8-bit shift register and latch driver

BU2114 / BU2114F

The BU2114 and BU2114F are CMOS ICs with low power consumption, and are equipped with an 8-bit shift register latch. Data in the shift register can be latched asynchronously. The outputs (O1 to O8) are open drain outputs (because there is no protection diode, a maximum voltage above V_{DD}, of up to 7V, can be applied), and one output can drive 36 mA. A total output of up to 150 mA can be driven (when using static operation).

●Applications

These are designed for a wide range of applications in microcomputer peripheral circuits, such as in industrial equipment, office telephones, audio visual equipment, and expansion input and output boards.

●Features

1) The CMOS configuration enables low power consumption.
2) Open drain output.
3) Latch to 8-bit shift register provided, enabling drive of up to 150mA. (I_{SINK} = 36mA)
4) Cascade connections possible.

●Absolute maximum ratings (unless otherwise noted, Ta = 25°C)

Parameter		Symbol	Limits	Unit
Applied voltage		V_{DD}	– 0.3 ~ + 7.0	V
Input voltage		V_{IN}	– 0.3 ~ V_{DD}0.3	V
Operating temperature		Topr	– 25 ~ + 75	°C
Storage temperature		Tstg	– 55 ~ + 150	°C
Input protection diode current		ID	± 20	mA
Power dissipation	BU2114	Pd	1100*1	mW
	BU2114F		400*2	

*1 Power dissipation is reduced by 8.8mW for each increase in Ta of 1°C over 25°C.

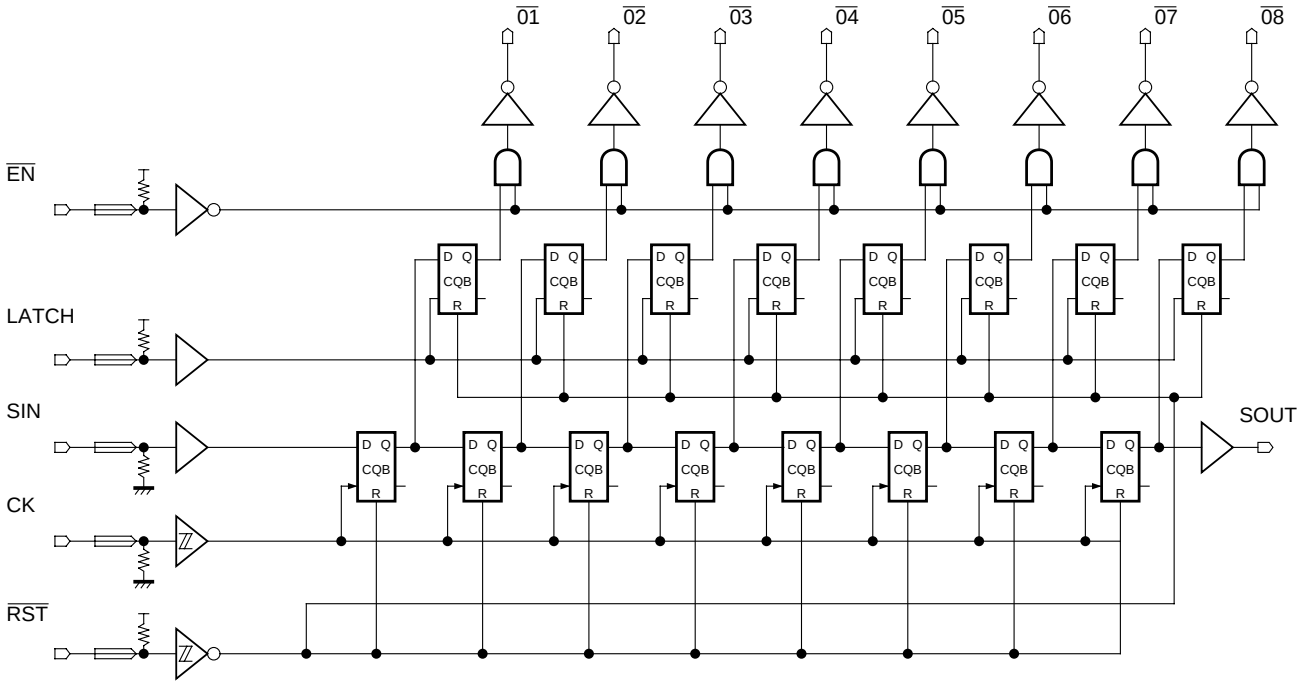
*2 Power dissipation is reduced by 3.2mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (unless otherwise noted, Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Recommend voltage	V_{DD}	4.5	5.0	5.5	V	
Input voltage	V_{IN}	0	—	V_{DD}	V	SIN, CK, LATCH, EN, RST
Output voltage	V_{OUT}	0	—	V_{DD}	V	SOUT

○Not designed for radiation resistance.

●Logic circuit diagram



●Pin assignments

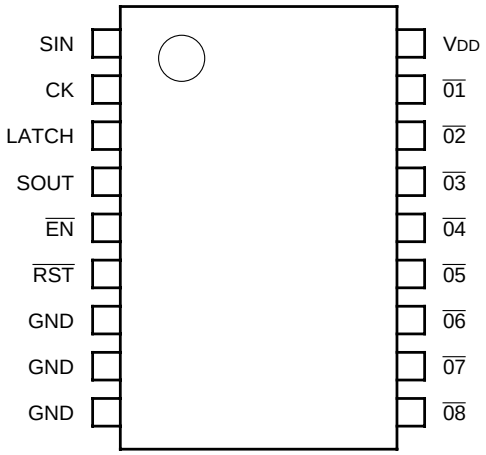


Fig.1

●Pin descriptions

Pin No.	Symbol	I / O	Function
1	SIN	I	Serial data input pin
2	CK	I	Shift clock for shift register
3	LATCH	I	Setting this pin to "L" holds the latch output. While it is "H", latch output changes simultaneously when the shift register output changes.
4	SOUT	O	This is the output for the final-stage shift register.
5	EN	I	This is the Enable pin for O1 to O8. When this pin is "L", the latch output appears as is. When the output is "H", however, output QN is "L", and when the latch output is "L", Qn becomes High-Z
6	RST	I	Resets the shift register and latch.
7	GND	—	0V power supply
8	GND	—	0V power supply
9	GND	—	0V power supply
10	O8	O	Latch output for 8th stage of shift register
11	O7	O	Latch output for 7th stage of shift register
12	O6	O	Latch output for 6th stage of shift register
13	O5	O	Latch output for 5th stage of shift register
14	O4	O	Latch output for 4th stage of shift register
15	O3	O	Latch output for 3rd stage of shift register
16	O2	O	Latch output for 2nd stage of shift register
17	O1	O	Latch output for 1st stage of shift register
18	V_{DD}	—	+ V_{DD} power supply

Note 1) O1 to O8 are open drain output, and when the shift register output is "H", the output level goes "L".

●Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{DD} = 5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input low level voltage	V_{IL}	0	—	1.5	V	SIN, LATCH, EN
Input high level voltage	V_{IH}	3.5	—	5.0	V	SIN, LATCH, EN
Output low level current	I_{SL}	—	—	6	mA	SOUT (VL = 0.4)
Output high level current	I_{SH}	—	—	– 6	mA	SOUT (VL = V_{DD} – 0.4)
Schmitt trigger "H" threshold value	V_P	2.31	—	3.28	V	CK, RST
Schmitt trigger "L" threshold value	V_N	1.5	—	2.58	V	CK, RST
Schmitt trigger hysteresis width	V_H	0.35	0.75	—	V	CK, RST
Output low level voltage	V_{OL} V_{OL}	— —	— —	0.15 0.4	V V	O1 ~ O8I_D = 12mA O1 ~ O8I_D = 36mA
Output leakage current	I_L	—	—	± 10	µA	—
Current dissipation	I_{DD}	—	1	100	µA	V_{DD} or GND
Pull-up resistance	R_{UP}	35	50	68	kΩ	—
Pull-down resistance	R_{DN}	35	50	68	kΩ	—

●Timing characteristics (unless otherwise noted, Ta = 25°C, V_{DD} = 5.0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock frequency	f	Input duty 50%			5	MHz
Clock pulse width	t_{cw}	—	100	—	—	ns
Latch pulse width	t_{rw}	—	100	—	—	ns
Data setup time	t_{su}	CK→SIN	100	—	—	ns
Data hold time	t_h	CK→SIN	100	—	—	ns
Clock latch time	t_{dtl}	—	100	—	—	ns

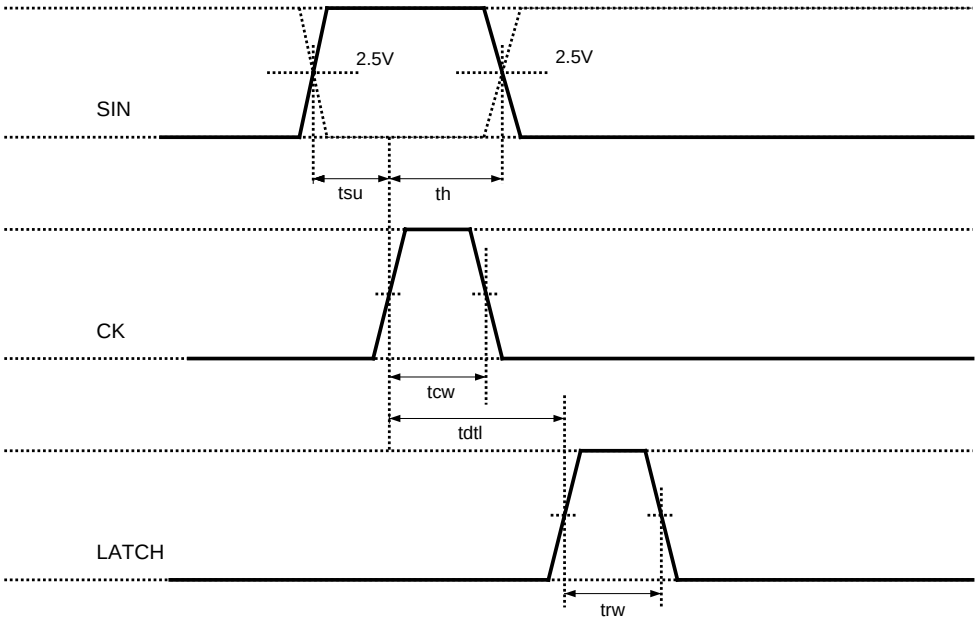
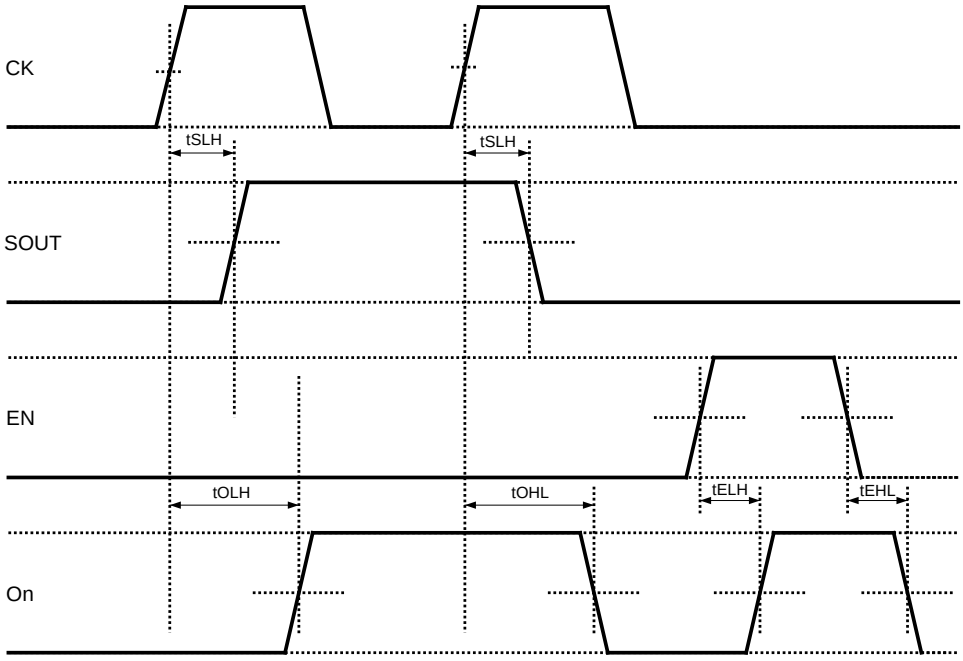


Fig.2 Timing conditions

●Switching characteristics (unless otherwise noted, Ta = 25°C, V_{DD} = 5.0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output "L - H" propagation time Input CK to output SOUT	t_{SLH}	V_{IH} = 5v V_{IL} = 0v	—	—	100	ns
Output "H - L" propagation time Input CK to output SOUT	t_{SPLH}		—	—	100	ns
Output "L - H" propagation time Input CK to output ON	t_{OLH}		—	—	200	ns
Output "H - L" propagation time Input CK to output ON	t_{OHL}		—	—	200	ns
Output "L - H" propagation time Input EN to output ON	t_{ELH}		—	—	100	ns
Output "H - L" propagation time Input EN to output ON	t_{EHL}		—	—	100	ns



Note) Measured with pull-up resistance of 1.0kΩ and load of 20pF applied to terminals O1 to O8.

Fig.3 Switching characteristic

●Timing chart

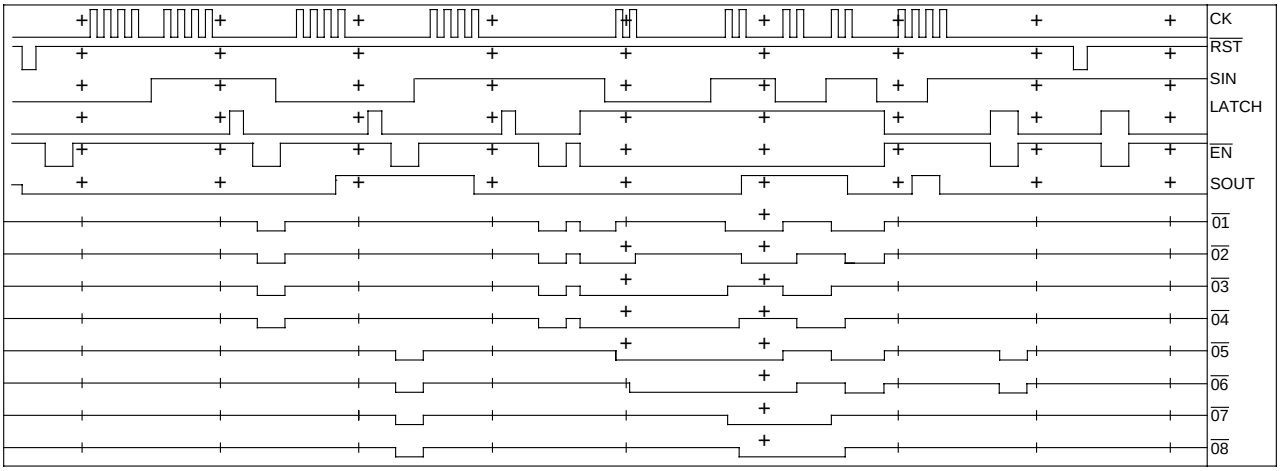


Fig.4

●Input / output circuits

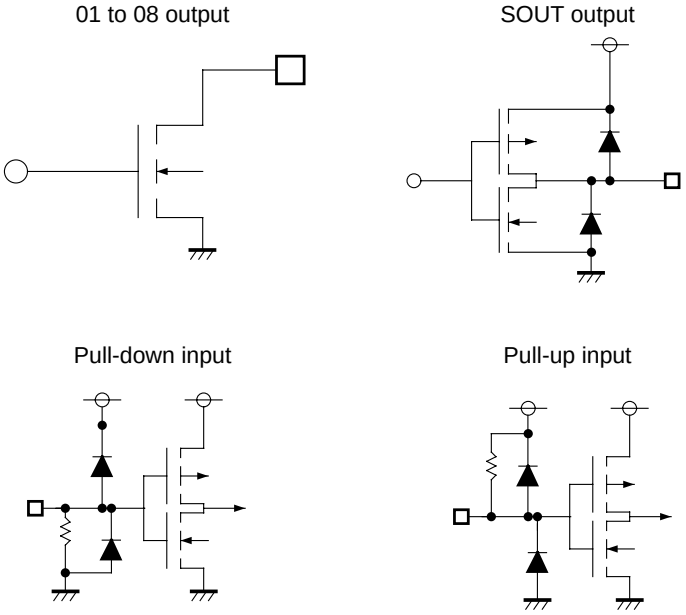


Fig.5

●Application example

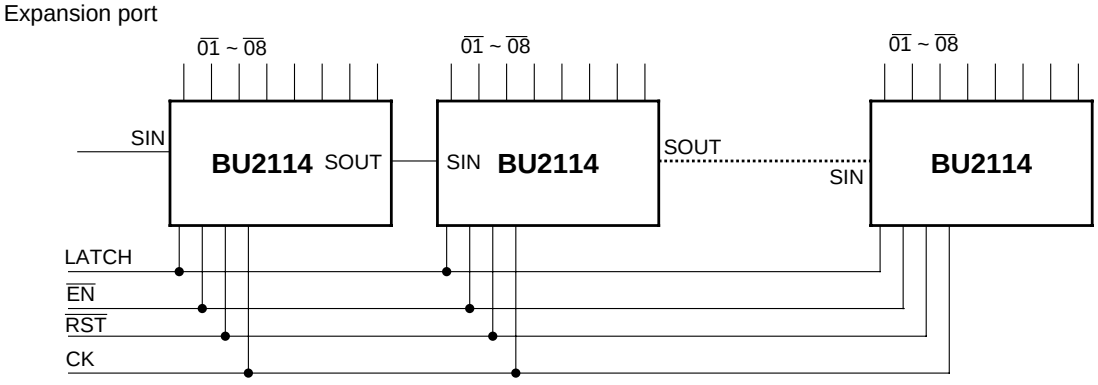
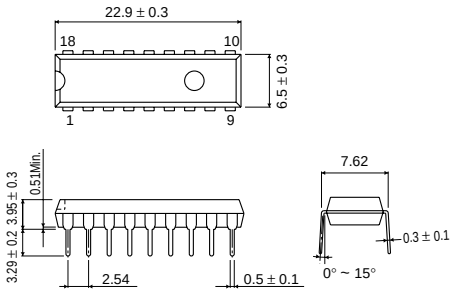


Fig.6

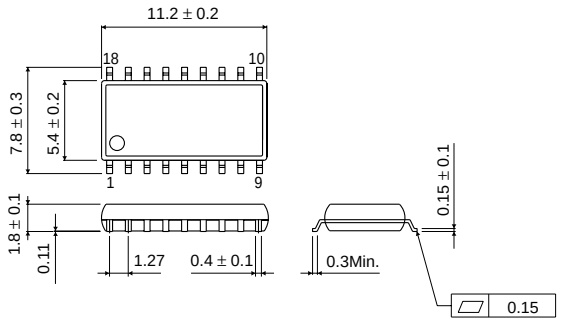
●External dimensions (Units: mm)

BU2114



DIP18

BU2114F



SOP18