

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U-MOSII)

2SK3442

Switching Regulator, DC-DC Converter and Motor Drive Applications

- Low drain-source ON resistance: $R_{DS(ON)} = 15 \text{ m}\Omega$ (typ.)
- High forward transfer admittance: $|Y_{fs}| = 28 \text{ S}$ (typ.)
- Low leakage current: $I_{DSS} = 100 \mu\text{A}$ ($V_{DS} = 100 \text{ V}$)
- Enhancement mode: $V_{th} = 2.0\sim 4.0 \text{ V}$ ($V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$)

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	100	V
Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)	V_{DGR}	100	V
Gate-source voltage	V_{GSS}	± 30	V
Drain current	DC (Note 1)	I_D	45
	Pulse (Note 1)	I_{DP}	180
Drain power dissipation ($T_c = 25^\circ\text{C}$)	P_D	125	W
Single pulse avalanche energy (Note 2)	E_{AS}	468	mJ
Avalanche current	I_{AR}	45	A
Repetitive avalanche energy (Note 3)	E_{AR}	12.5	mJ
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature range	T_{stg}	$-55\sim 150$	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

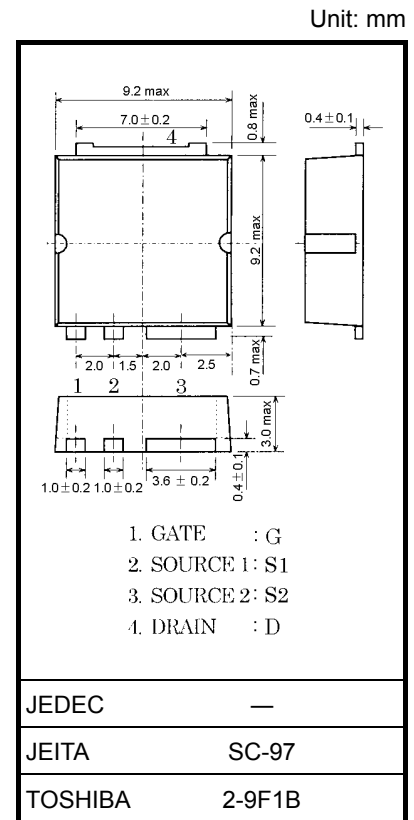
Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th(ch-c)}$	1.00	$^\circ\text{C/W}$

Note 1: Ensure that the channel temperature does not exceed 150°C .

Note 2: $V_{DD} = 25 \text{ V}$, $T_{ch} = 25^\circ\text{C}$ (initial), $L = 373 \mu\text{H}$, $R_G = 25 \Omega$, $I_{AR} = 45 \text{ A}$

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

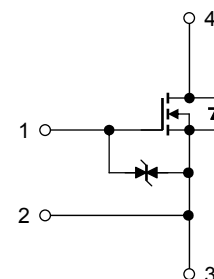
This transistor is an electrostatic-sensitive device. Please handle with caution.



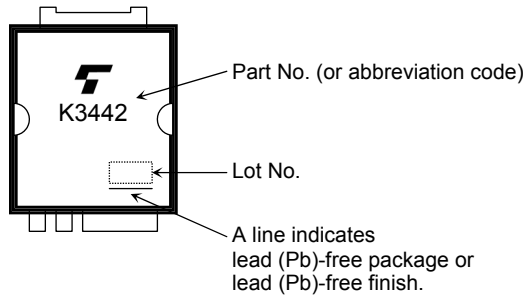
Weight: 0.74 g (typ.)

Notice:

Please use the S1 pin for gate input signal return. Make sure that the main current flows into the S2 pin.



Marking



Electrical Characteristics (Note 4) (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 25\text{ V}, V_{DS} = 0\text{ V}$	—	—	± 10	μA
Drain cut-off current		I_{DSS}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	100	—	—	V
Gate threshold voltage		V_{th}	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$	2.0	—	4.0	V
Drain-source ON resistance		$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 23\text{ A}$	—	15	20	$\text{m}\Omega$
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 23\text{ A}$	14	28	—	S
Input capacitance		C_{iss}	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	4100	—	pF
Reverse transfer capacitance		C_{rss}		—	340	—	
Output capacitance		C_{oss}		—	980	—	
Switching time	Rise time	t_r		—	15	—	ns
	Turn-on time	t_{on}		—	45	—	
	Fall time	t_f		—	20	—	
	Turn-off time	t_{off}		—	95	—	
Total gate charge (gate-source plus gate-drain)		Q_g	$V_{DD} \approx 80\text{ V}, V_{GS} = 10\text{ V}, I_D = 45\text{ A}$	—	85	—	nC
Gate-source charge		Q_{gs}		—	50	—	
Gate-drain ("miller") charge		Q_{gd}		—	35	—	

Note 4: Connect the S1 and S2 pins together, and ground them except during switching time measurement.

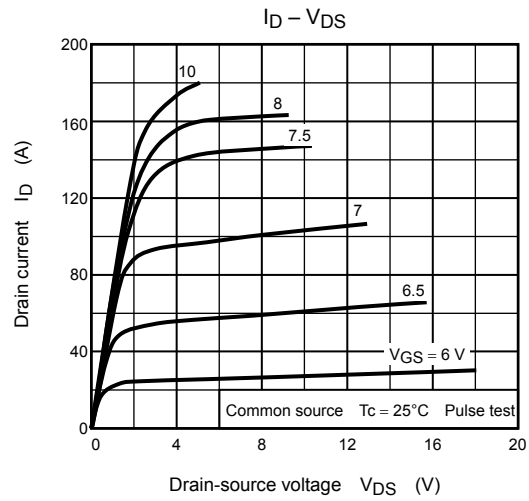
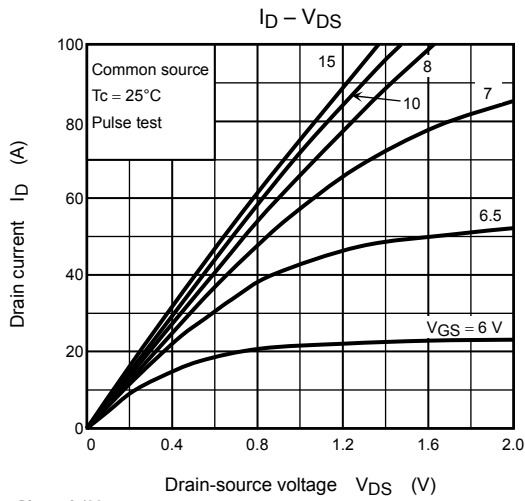
Source-Drain Ratings and Characteristics (Note 5) (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1, Note 5)	I_{DR1}	—	—	—	45	A
Pulse drain reverse current (Note 1, Note 5)	I_{DRP1}	—	—	—	180	A
Continuous drain reverse current (Note 1, Note 5)	I_{DR2}	—	—	—	1	A
Pulse drain reverse current (Note 1, Note 5)	I_{DRP2}	—	—	—	4	A
Forward voltage (diode)	V_{DS2F}	$I_{DR} = 45\text{ A}, V_{GS} = 0\text{ V}$	—	—	-1.5	V
Reverse recovery time	t_{rr}	$I_{DR} = 45\text{ A}, V_{GS} = 0\text{ V},$	—	160	—	ns
Reverse recovery charge	Q_{rr}	$dI_{DR}/dt = 50\text{ A}/\mu\text{s}$	—	512	—	nC

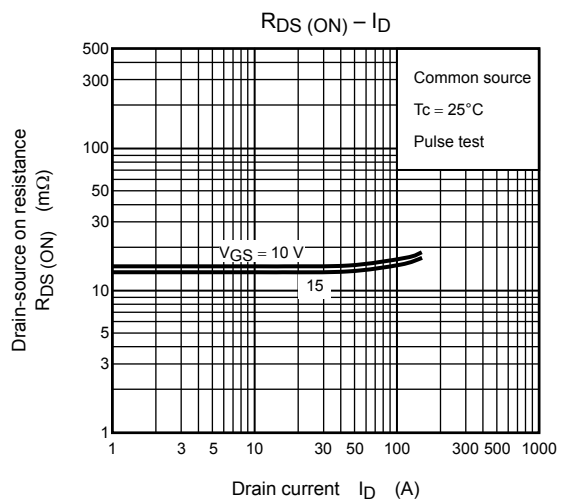
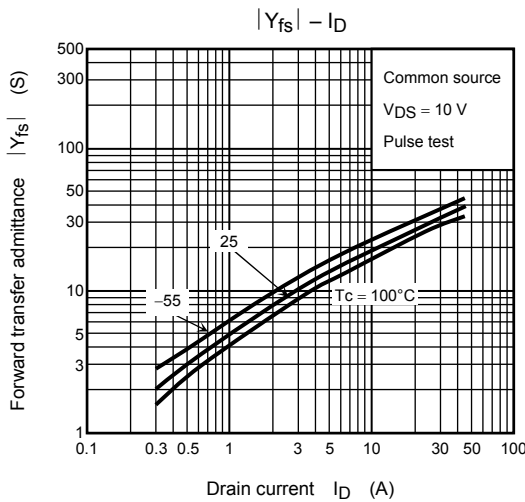
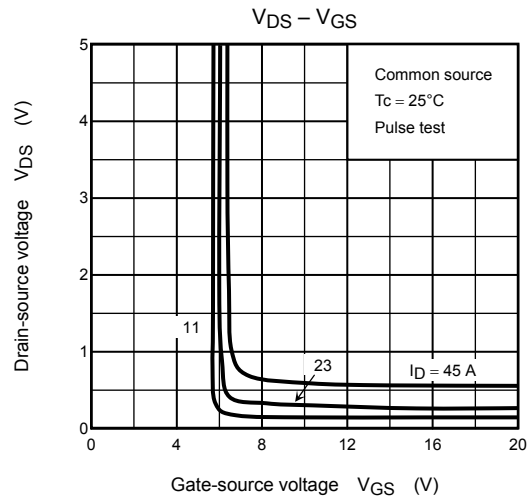
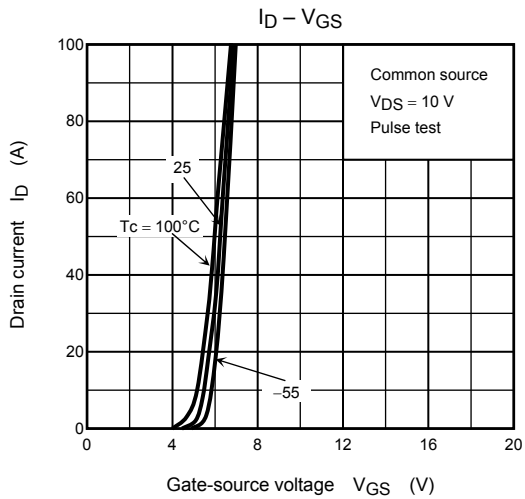
Note 5: I_{DR1}, I_{DRP1} : Current flowing between the drain and the S2 pin. Ensure that the S1 pin is left open.

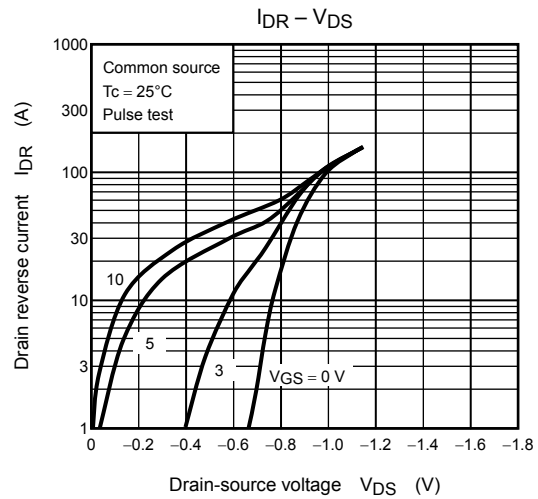
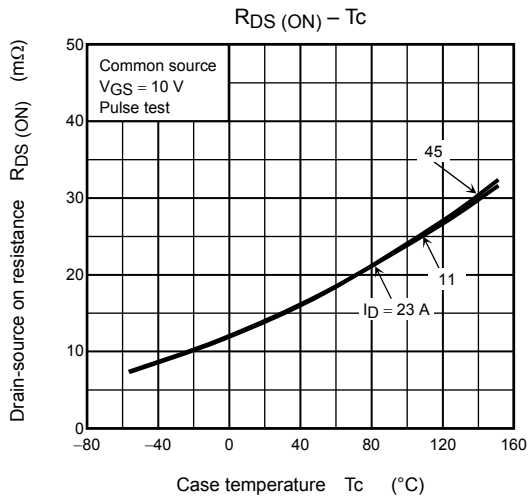
I_{DR2}, I_{DRP2} : Current flowing between the drain and the S1 pin. Ensure that the S2 pin is left open.

Unless otherwise specified, connect the S1 and S2 pins together, and ground them.

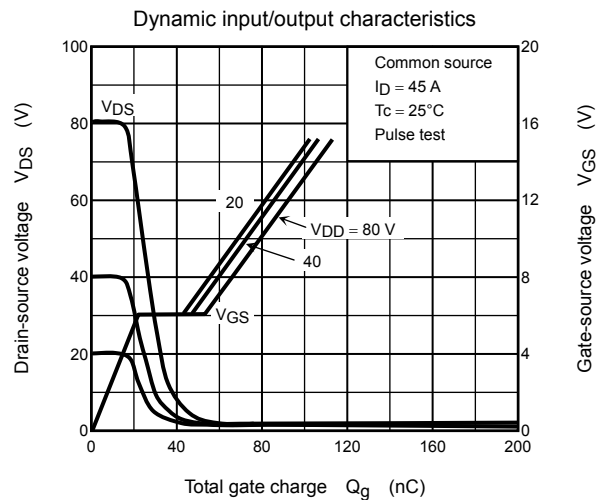
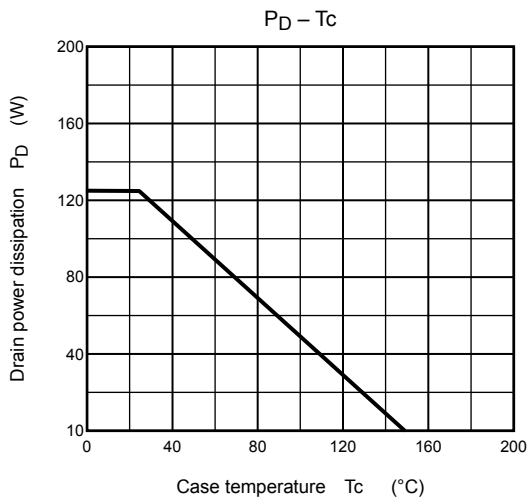
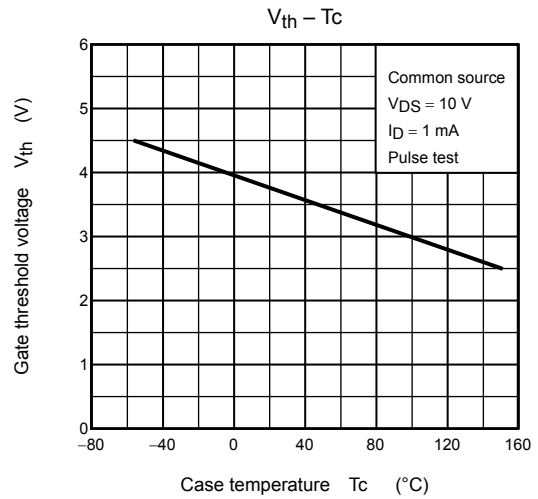
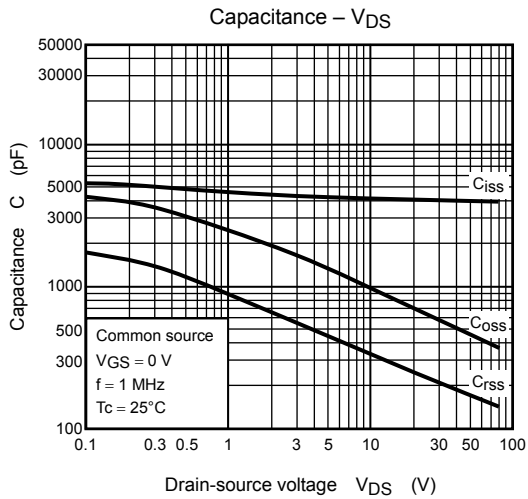


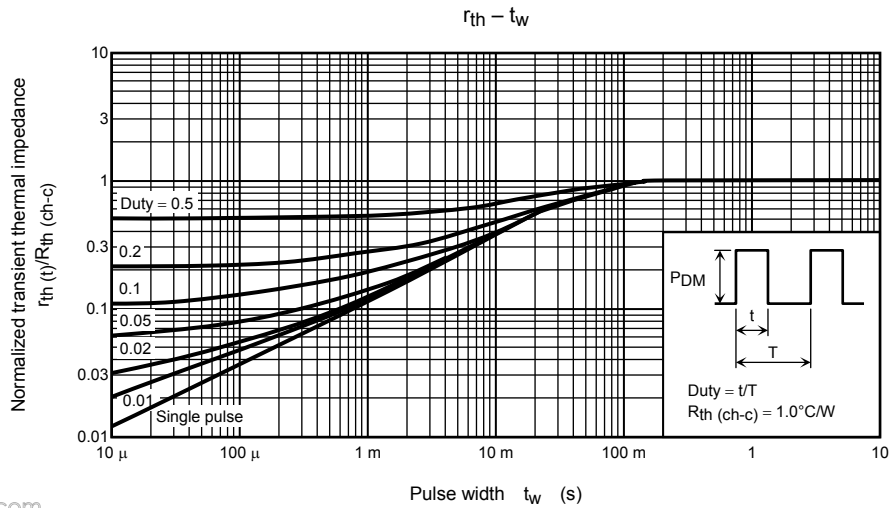
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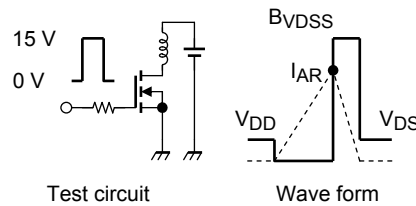
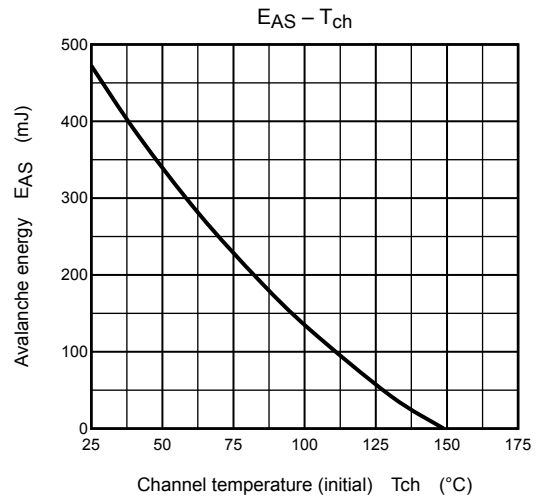
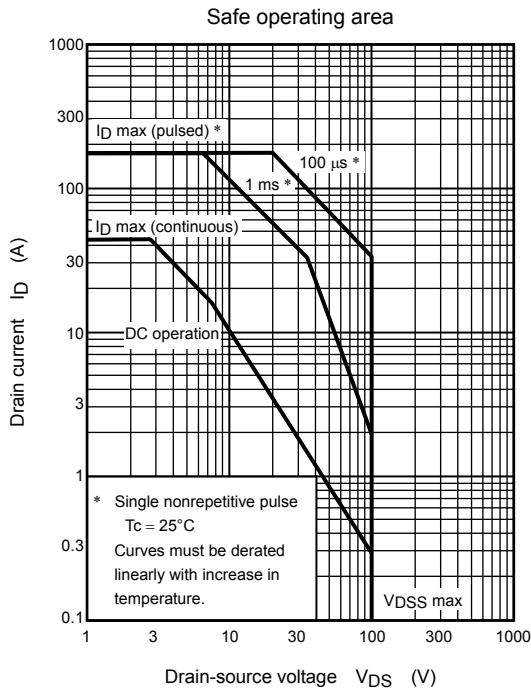


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$$R_G = 25 \Omega$$

$$V_{DD} = 25 V, L = 373 \mu H$$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AR}^2 \cdot \left(\frac{BVDSS}{BVDSS - V_{DD}} \right)$$

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