

# 2SK3136

Silicon N Channel MOS FET  
High Speed Power Switching

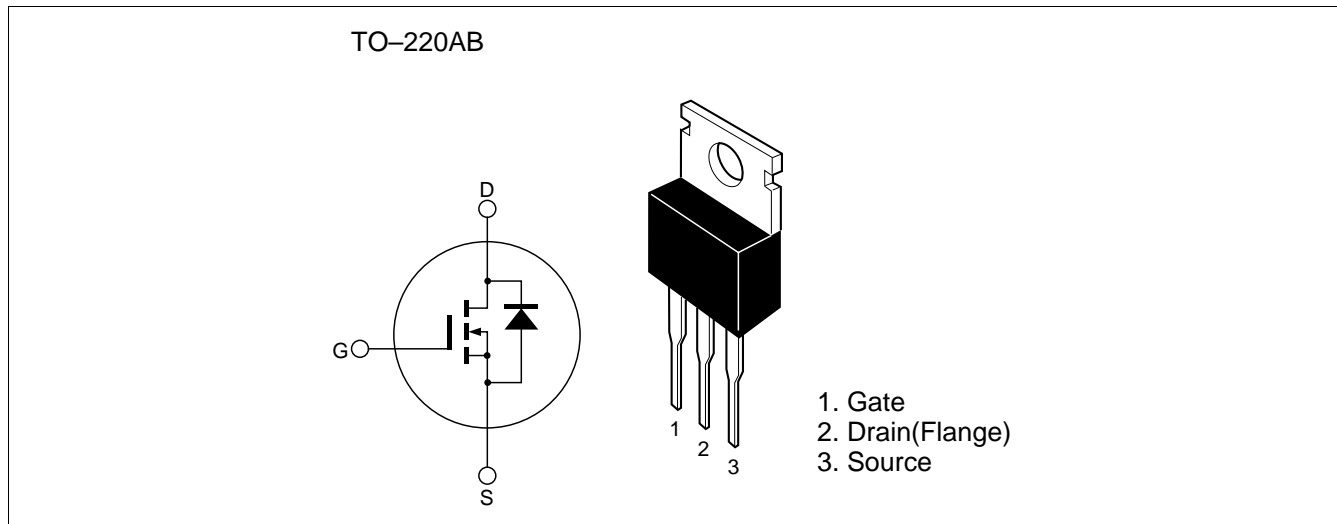
# HITACHI

ADE-208-696B (Z)  
3rd. Edition  
February 1999

## Features

- Low on-resistance  
 $R_{DS(on)} = 4.5 \text{ m}\Omega$  typ.
- Low drive current
- 4 V gate drive device can be driven from 5 V source

## Outline



**Absolute Maximum Ratings (Ta = 25°C)**

<b>Item</b>	<b>Symbol</b>	<b>Ratings</b>	<b>Unit</b>
Drain to source voltage	$V_{DSS}$	40	V
Gate to source voltage	$V_{GSS}$	±20	V
Drain current	$I_D$	75	A
Drain peak current	$I_{D(pulse)}$ <sup>Note 1</sup>	300	A
Body-drain diode reverse drain current	$I_{DR}$	75	A
Avalanche current	$I_{AP}$ <sup>Note 3</sup>	50	A
Avalanche energy	$E_{AR}$ <sup>Note 3</sup>	333	mJ
Channel dissipation	$P_{ch}$ <sup>Note 2</sup>	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

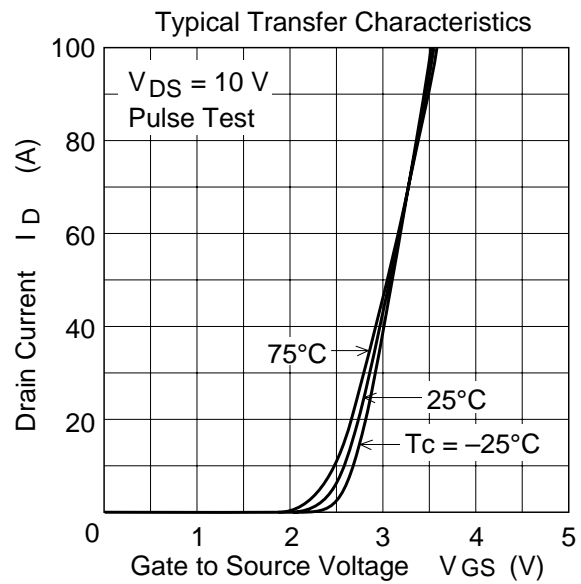
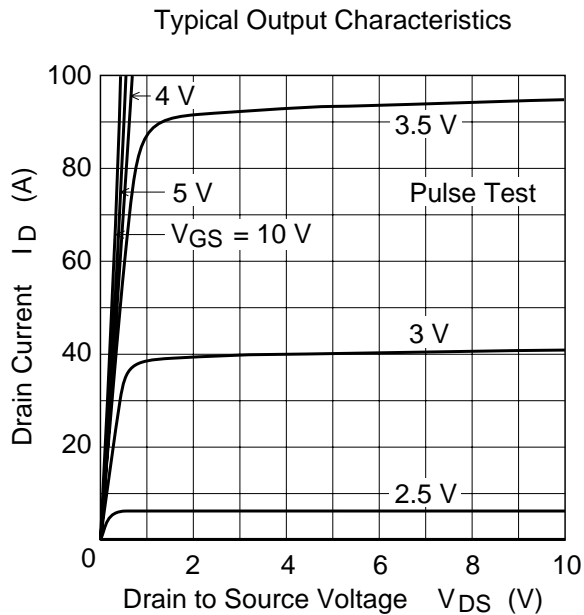
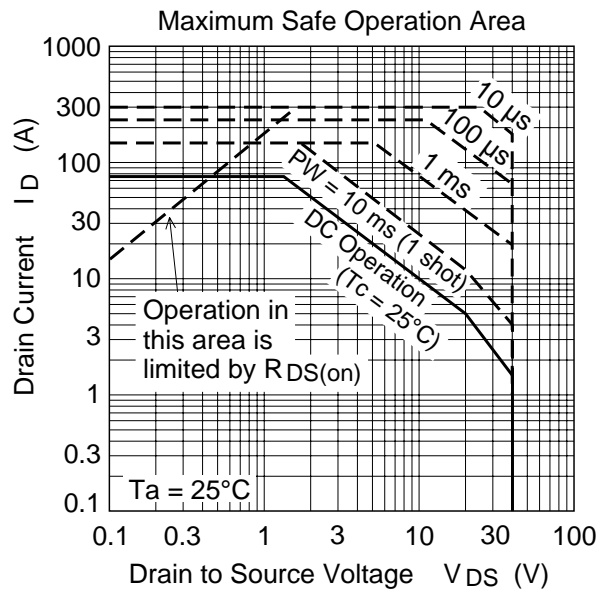
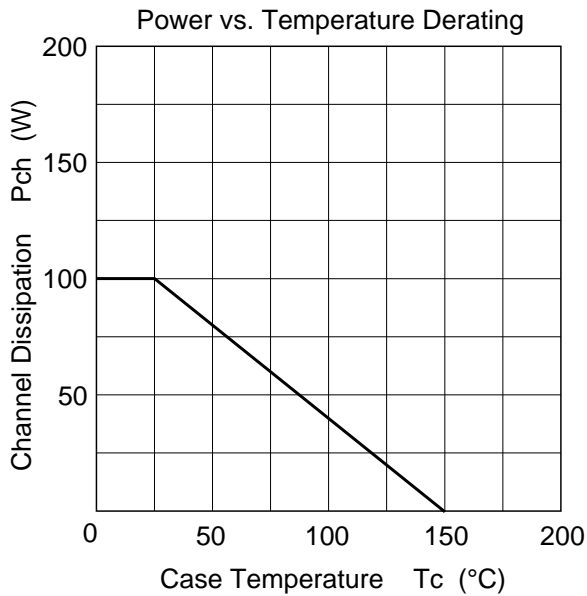
Note: 1.  $PW \leq 10 \mu s$ , duty cycle  $\leq 1\%$   
2. Value at  $T_c = 25^\circ C$   
3. Value at  $T_{ch} = 25^\circ C$ ,  $R_g \geq 50 \Omega$

## Electrical Characteristics (Ta = 25°C)

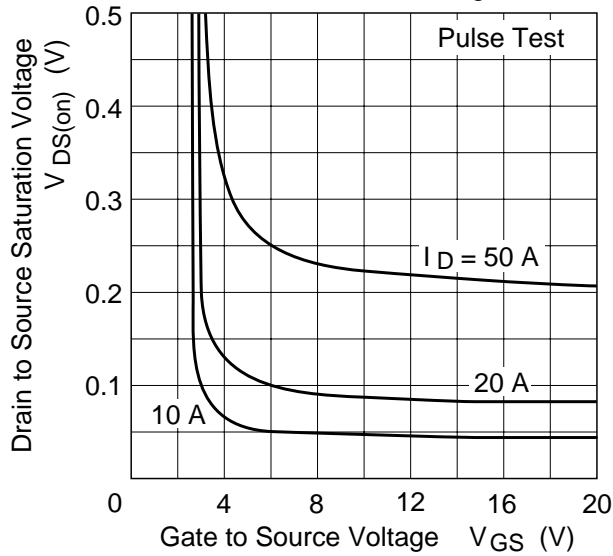
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	40	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 0.1$	$\mu\text{A}$	$V_{GS} = \pm 20 \text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	10	$\mu\text{A}$	$V_{DS} = 40 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$I_D = 1 \text{ mA}$ , $V_{DS} = 10 \text{ V}$ <sup>Note 1</sup>
Static drain to source on state resistance	$R_{DS(on)}$	—	4.5	5.8	m $\Omega$	$I_D = 40 \text{ A}$ , $V_{GS} = 10 \text{ V}$ <sup>Note 1</sup>
		—	6.5	10	m $\Omega$	$I_D = 40 \text{ A}$ , $V_{GS} = 4 \text{ V}$ <sup>Note 1</sup>
Forward transfer admittance	$ y_{fs} $	50	80	—	S	$I_D = 40 \text{ A}$ , $V_{DS} = 10 \text{ V}$ <sup>Note 1</sup>
Input capacitance	$C_{iss}$	—	6800	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	$C_{oss}$	—	1300	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	380	—	pF	$f = 1 \text{ MHz}$
Total gate charge	$Q_g$	—	130	—	nc	$V_{DD} = 25 \text{ V}$
Gate to source charge	$Q_{gs}$	—	25	—	nc	$V_{GS} = 10 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	30	—	nc	$I_D = 75 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	60	—	ns	$V_{GS} = 10 \text{ V}$ , $I_D = 40 \text{ A}$
Rise time	$t_r$	—	300	—	ns	$R_L = 0.75 \Omega$
Turn-off delay time	$t_{d(off)}$	—	550	—	ns	
Fall time	$t_f$	—	400	—	ns	
Body–drain diode forward voltage	$V_{DF}$	—	1.05	—	V	$I_F = 75 \text{ A}$ , $V_{GS} = 0$
Body–drain diode reverse recovery time	$t_{rr}$	—	90	—	ns	$I_F = 75 \text{ A}$ , $V_{GS} = 0$ $diF/dt = 50 \text{ A}/\mu\text{s}$

Note: 1. Pulse test

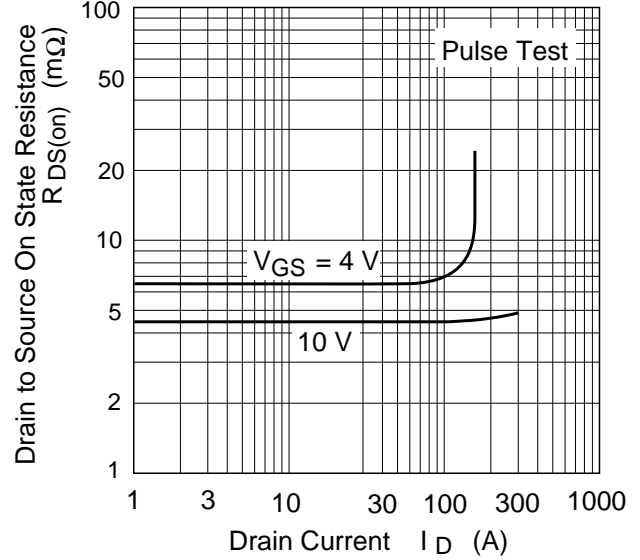
Main Characteristics



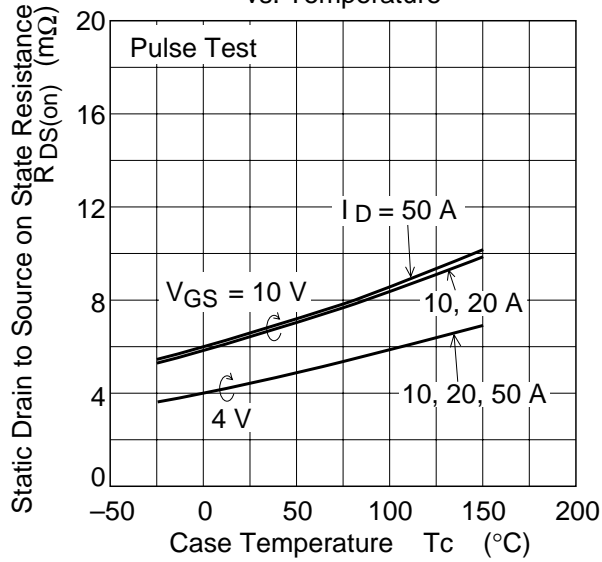
Drain to Source Saturation Voltage vs. Gate to Source Voltage



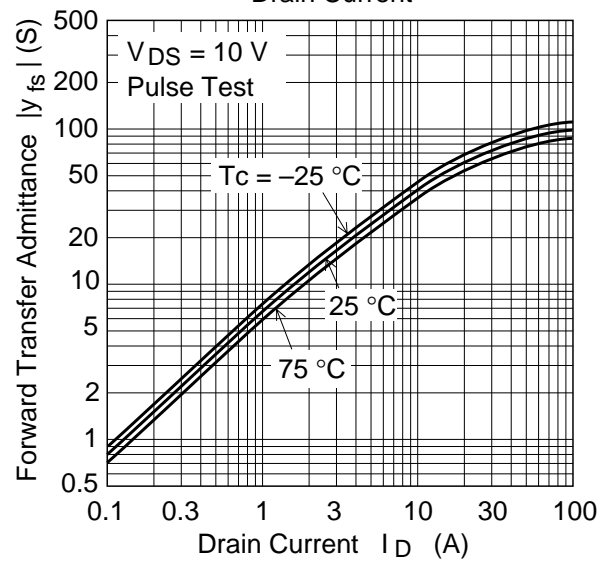
Static Drain to Source on State Resistance vs. Drain Current

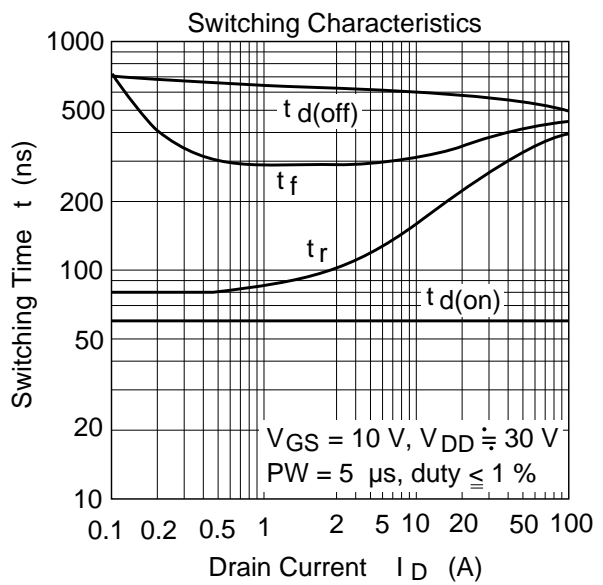
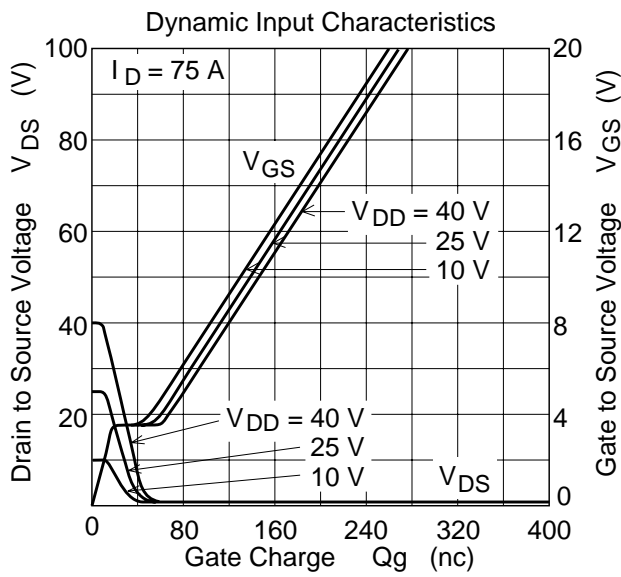
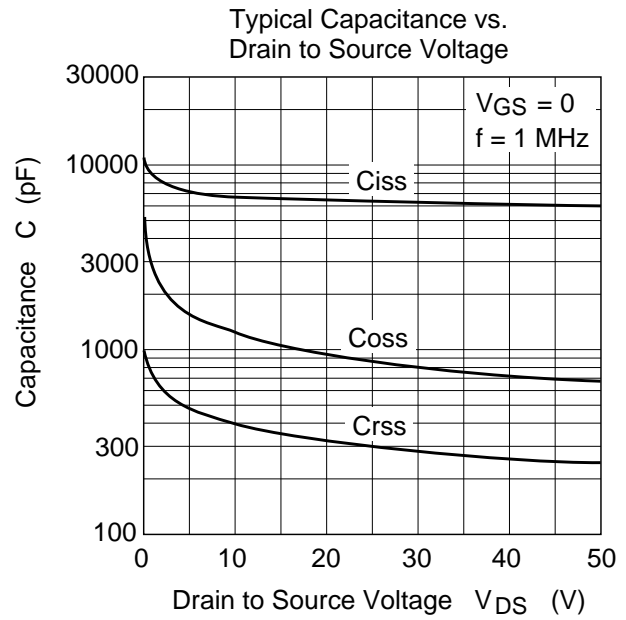
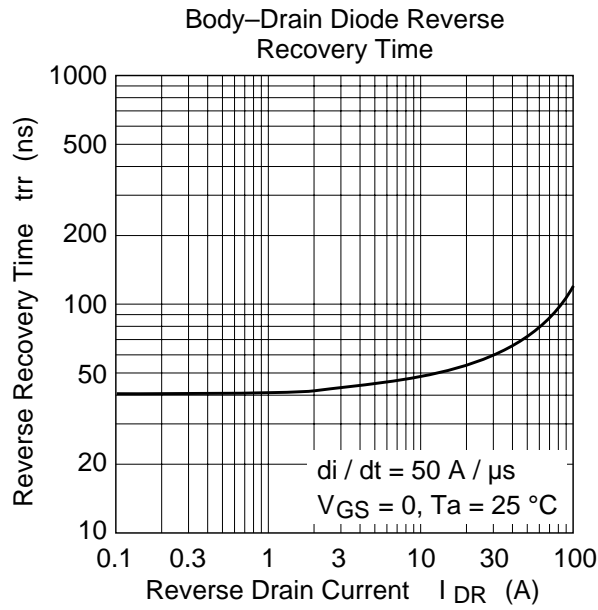


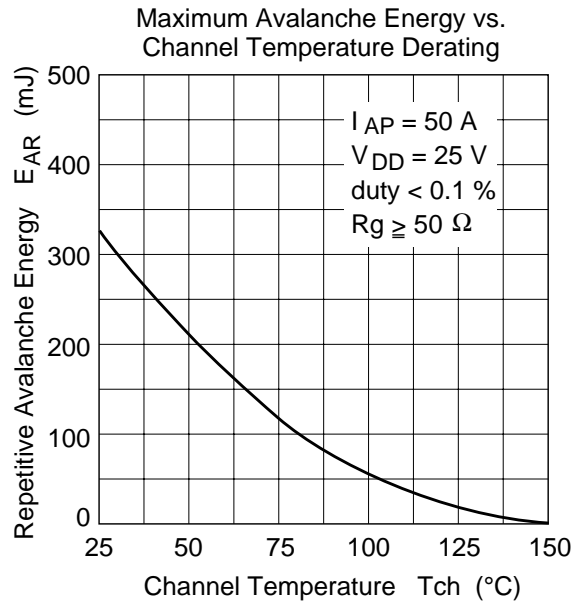
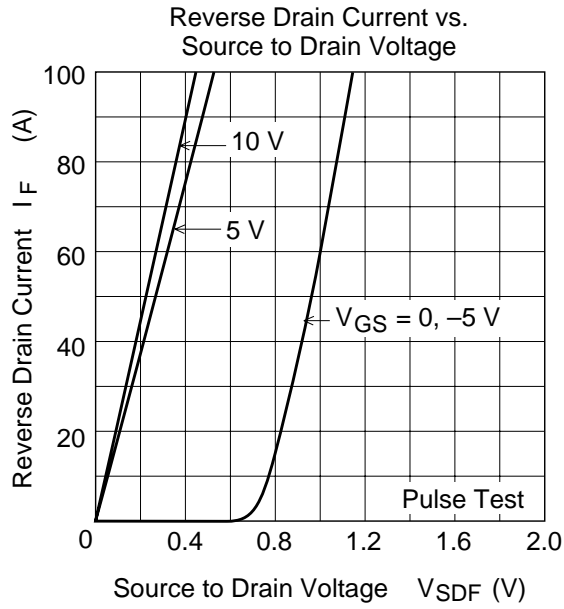
Static Drain to Source on State Resistance vs. Temperature



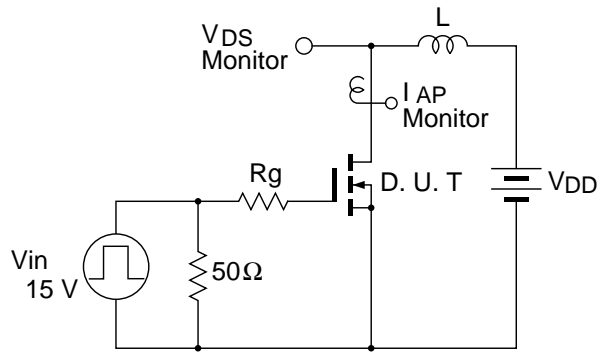
Forward Transfer Admittance vs. Drain Current





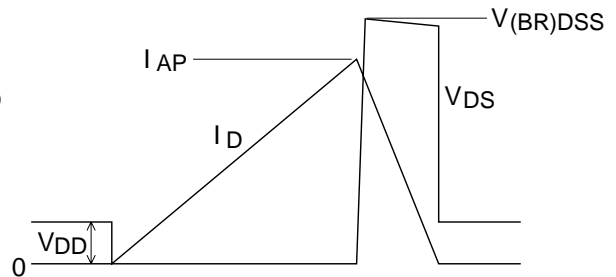


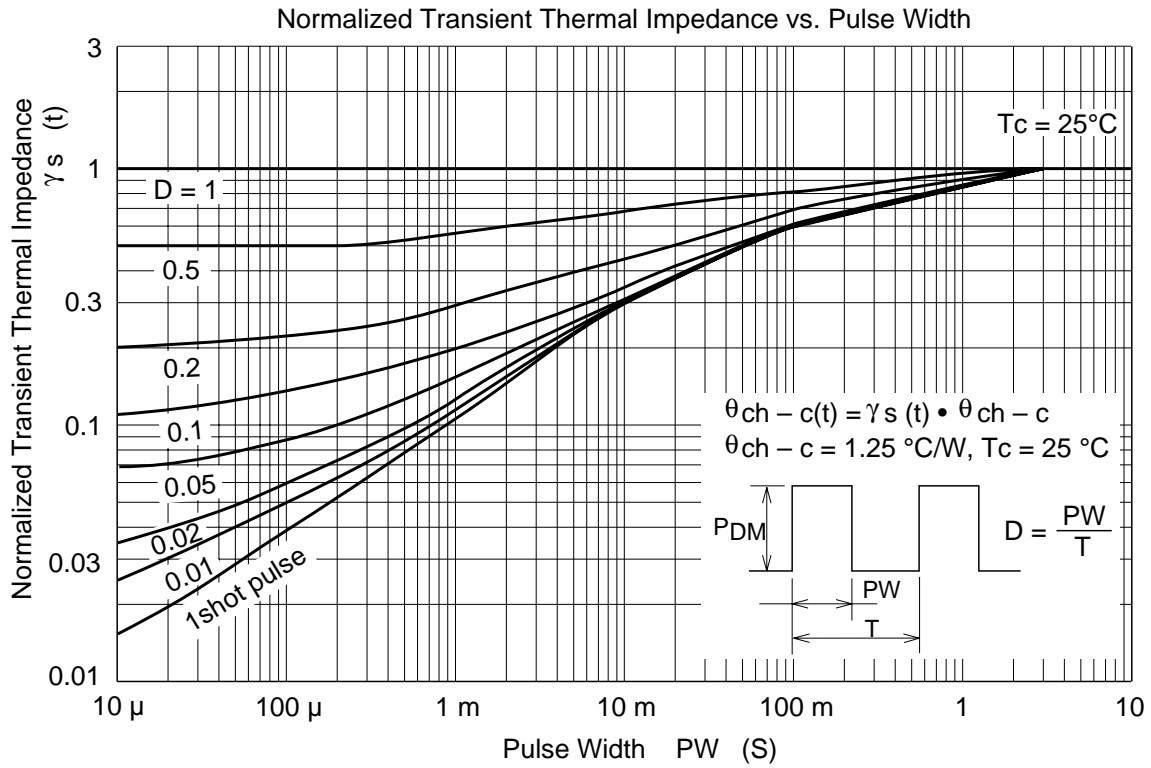
Avalanche Test Circuit



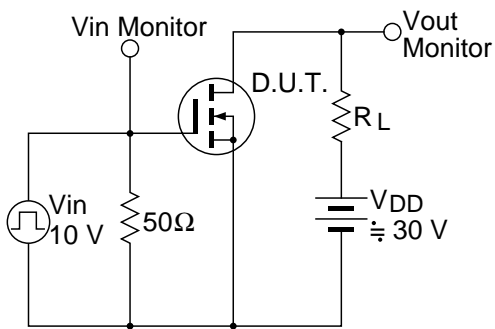
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

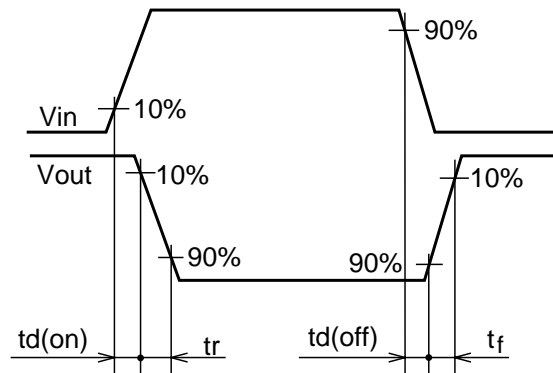




Switching Time Test Circuit



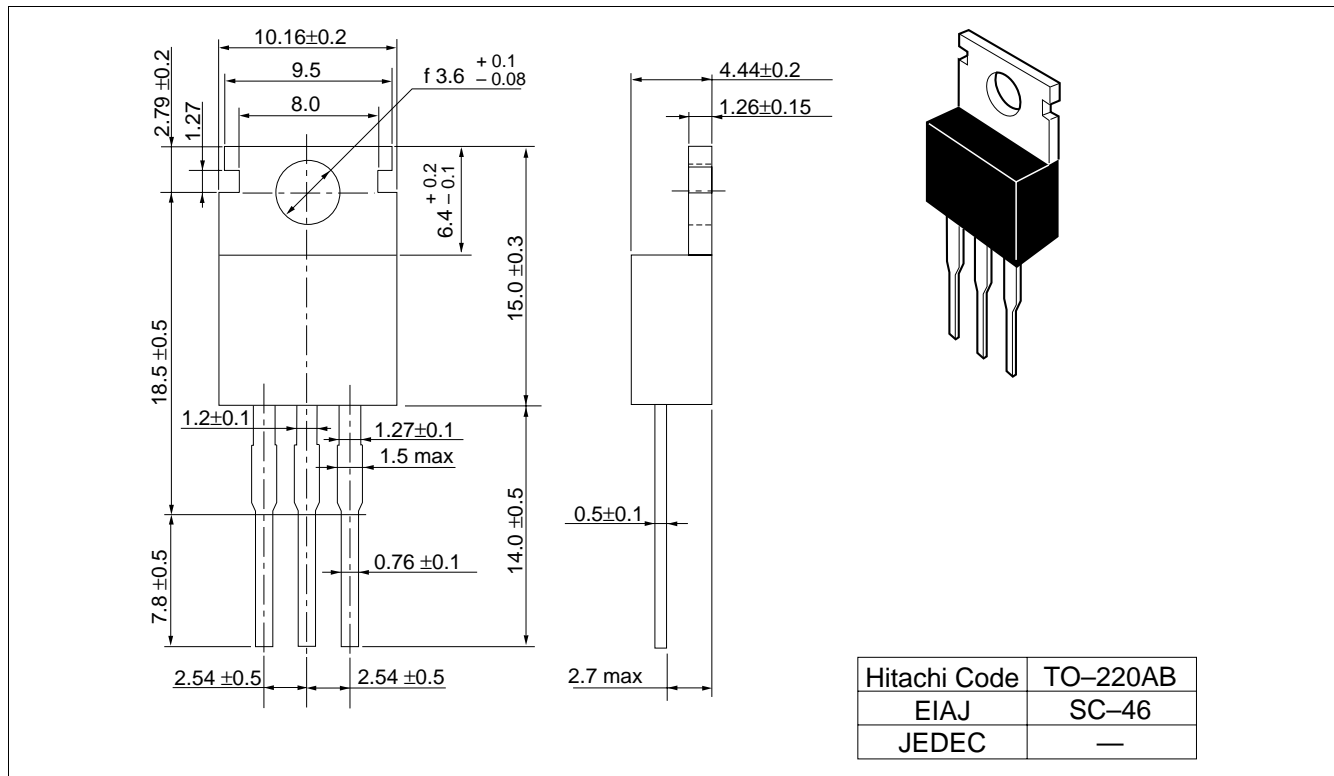
Waveform





## Package Dimensions

Unit: mm



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