

MOS FIELD EFFECT TRANSISTOR  
**2SK2510**

**SWITCHING  
N-CHANNEL POWER MOS FET  
INDUSTRIAL USE**

**DESCRIPTION**

The 2SK2510 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

**FEATURES**

- Super Low On-Resistance  
 $R_{DS(on)1} = 20\text{ m}\Omega$  ( $V_{GS} = 10\text{ V}$ ,  $I_D = 20\text{ A}$ )  
 $R_{DS(on)2} = 30\text{ m}\Omega$  ( $V_{GS} = 4\text{ V}$ ,  $I_D = 20\text{ A}$ )
- Low  $C_{iss}$   $C_{iss} = 1\ 600\text{ pF TYP.}$
- Built-in G-S Protection Diode

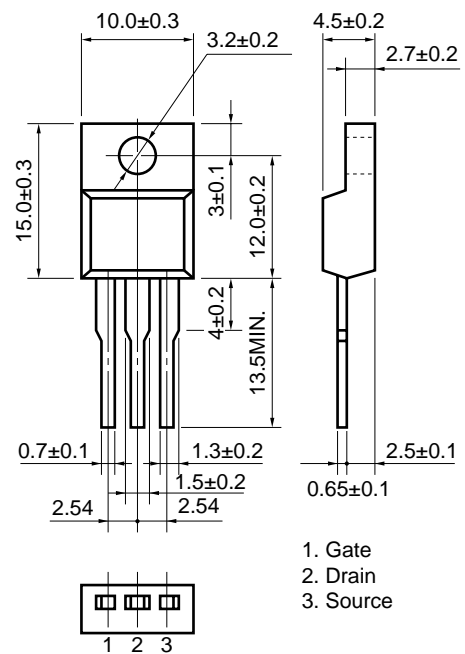
**ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$ )**

Drain to Source Voltage	$V_{bss}$	60	V
Gate to Source Voltage	$V_{gss}$	$\pm 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 40$	A
Drain Current (pulse)*	$I_{D(pulse)}$	$\pm 160$	A
Total Power Dissipation ( $T_c = 25\text{ }^\circ\text{C}$ )	$P_{T1}$	35	W
Total Power Dissipation ( $T_A = 25\text{ }^\circ\text{C}$ )	$P_{T2}$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

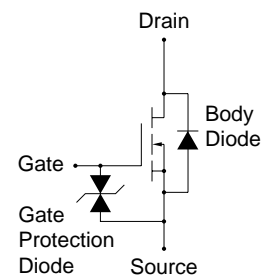
\*  $PW \leq 10\ \mu\text{s}$ , Duty Cycle  $\leq 1\ \%$

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

**PACKAGE DIMENSIONS  
(in millimeter)**



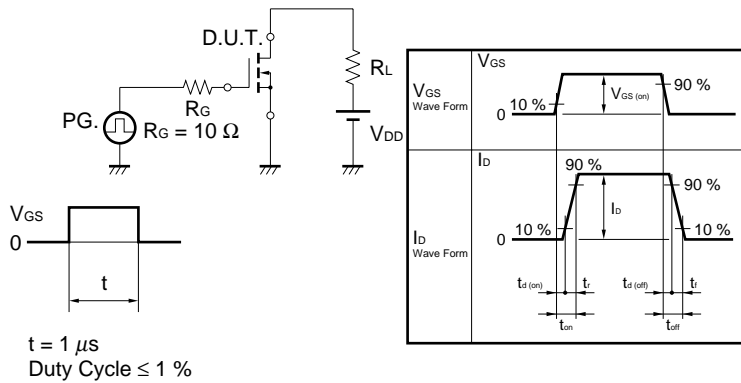
**MP-45F (ISOLATED TO-220)**



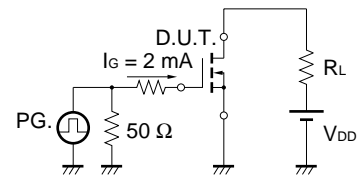
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-Resistance	R <sub>DS (on)1</sub>		16	20	mΩ	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A
Drain to Source On-Resistance	R <sub>DS (on)2</sub>		24	30	mΩ	V <sub>GS</sub> = 4 V, I <sub>D</sub> = 20 A
Gate to Source Cutoff Voltage	V <sub>GS (off)</sub>	1.0	1.5	2.0	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	13			S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 20 A
Drain Leakage Current	I <sub>DSS</sub>			10	μA	V <sub>DS</sub> = V <sub>DSS</sub> , V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>ISS</sub>		1 600		pF	V <sub>DS</sub> = 10 V
Output Capacitance	C <sub>OSS</sub>		780		pF	V <sub>GS</sub> = 0
Reverse Transfer Capacitance	C <sub>RSS</sub>		350		pF	f = 1 MHz
Turn-On Delay Time	t <sub>d (on)</sub>		35		ns	I <sub>D</sub> = 20 A
Rise Time	t <sub>r</sub>		380		ns	V <sub>GS (on)</sub> = 10 V
Turn-Off Delay Time	t <sub>d (off)</sub>		220		ns	V <sub>DD</sub> = 30 V
Fall Time	t <sub>f</sub>		300		ns	R <sub>G</sub> = 10 Ω
Total Gate Charge	Q <sub>G</sub>		69		nC	I <sub>D</sub> = 40 A
Gate to Source Charge	Q <sub>GS</sub>		5.0		nC	V <sub>DD</sub> = 48 V
Gate to Drain Charge	Q <sub>GD</sub>		26		nC	V <sub>GS</sub> = 10 V
Body Diode Forward Voltage	V <sub>F (S-D)</sub>		1.0		V	I <sub>F</sub> = 40 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		72		ns	I <sub>F</sub> = 40 A, V <sub>GS</sub> = 0
Reverse Recovery Charge	Q <sub>rr</sub>		130		nC	di/dt = 100 A/μs

**Test Circuit 1 Switching Time**

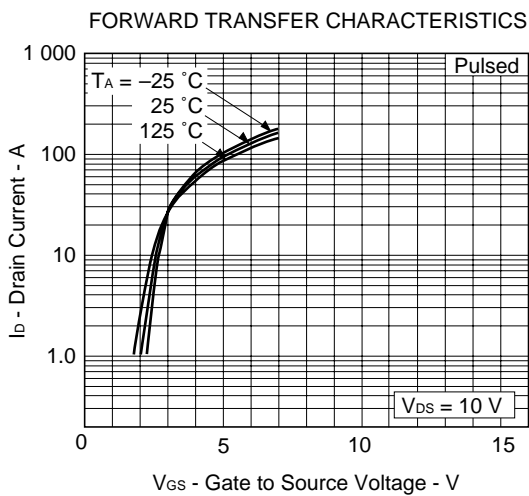
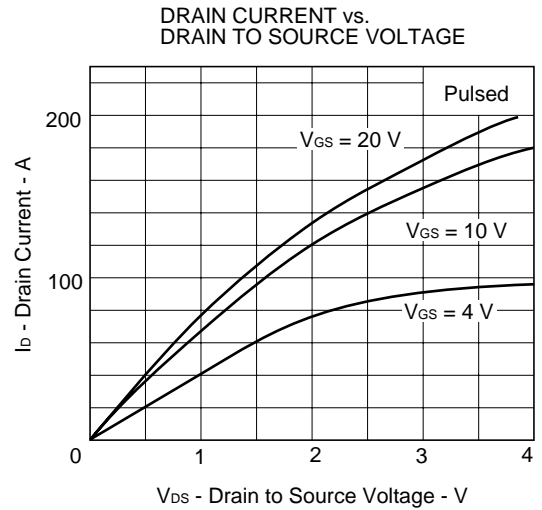
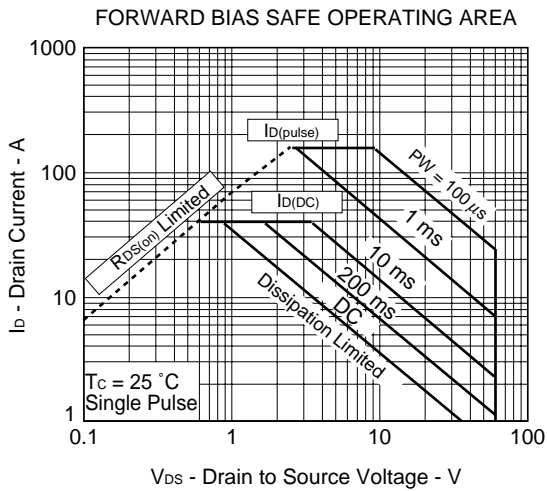
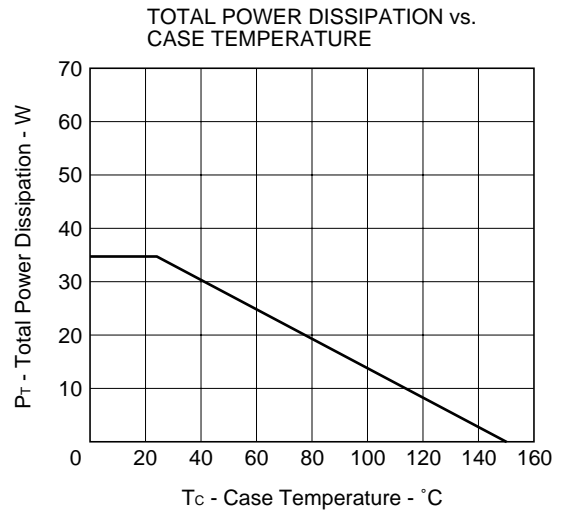
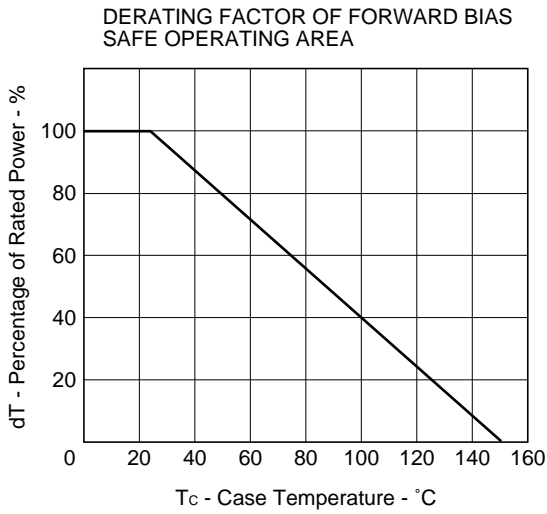


**Test Circuit 2 Gate Charge**

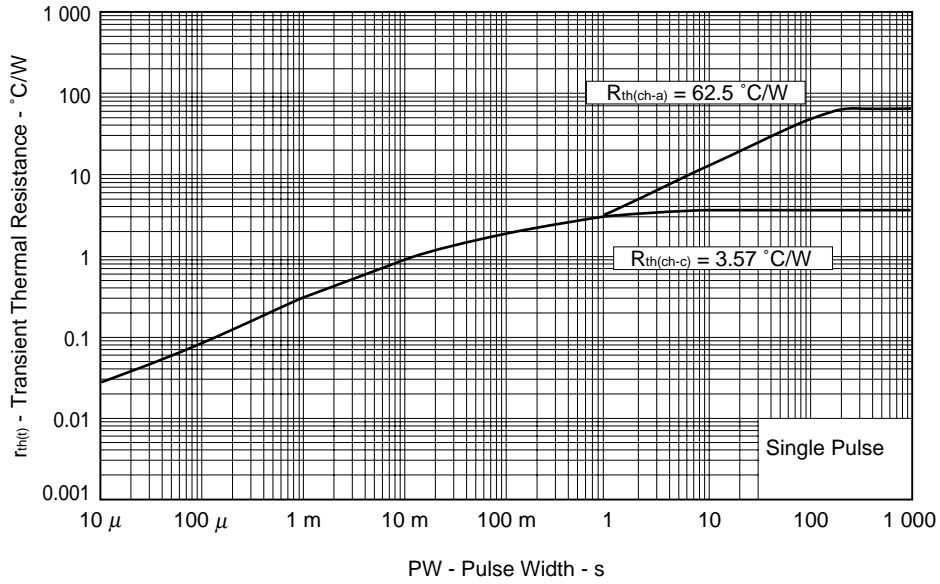


The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

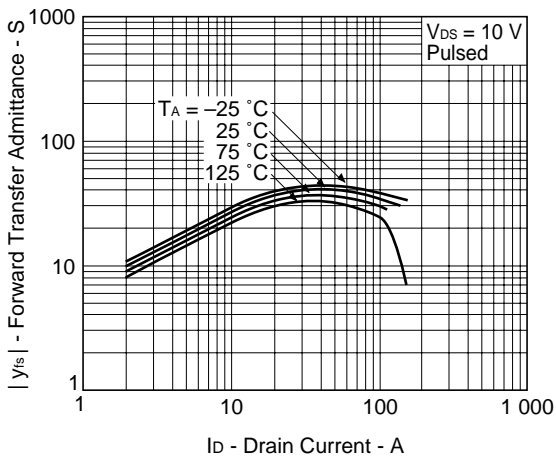
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)



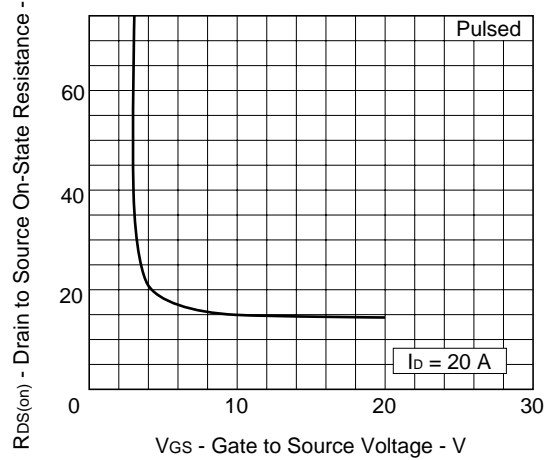
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



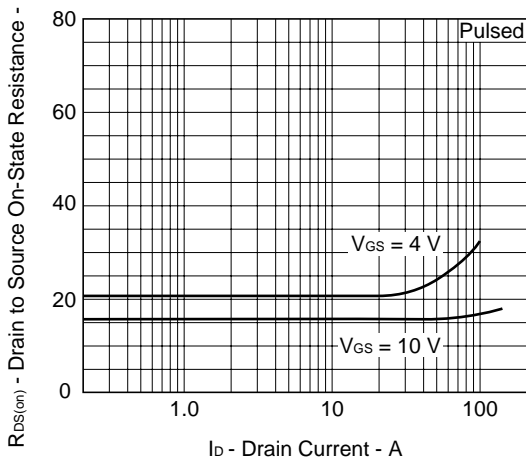
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



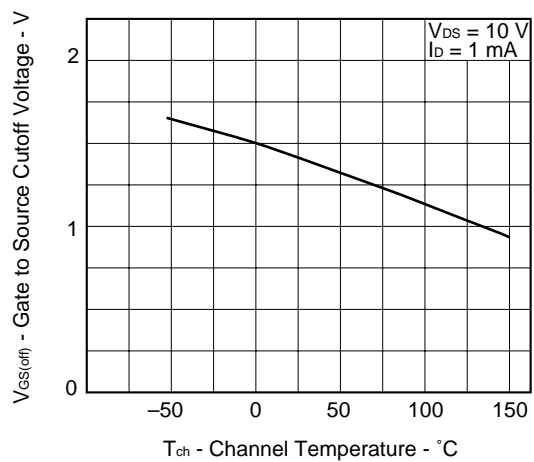
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

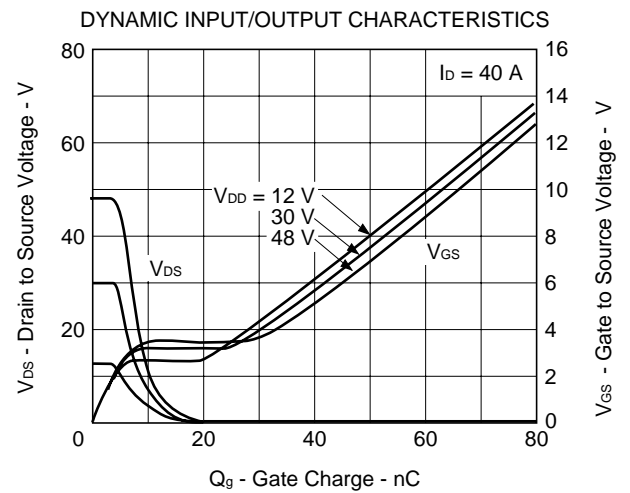
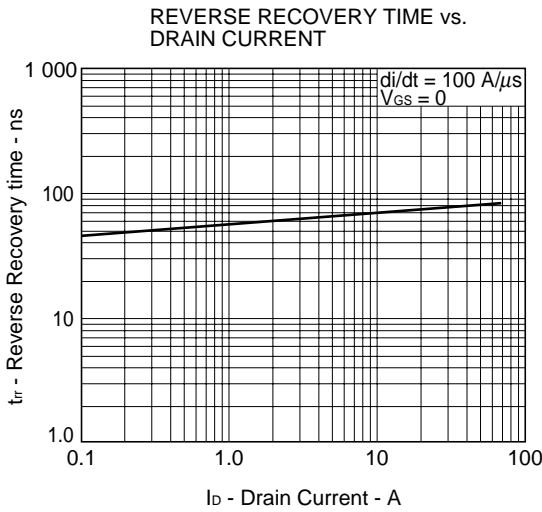
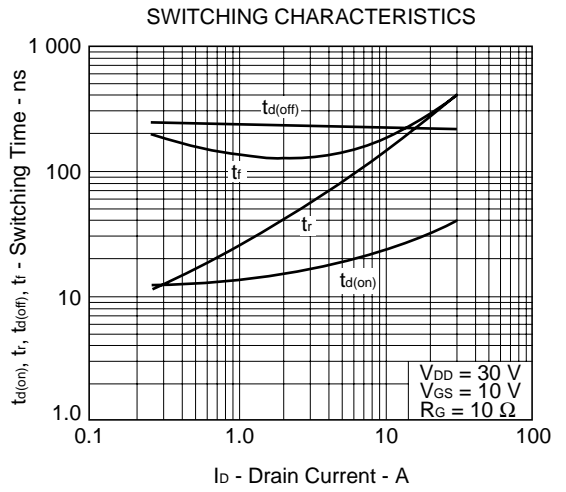
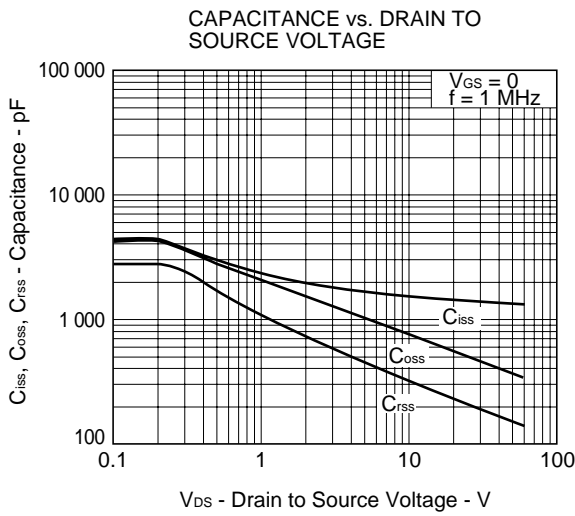
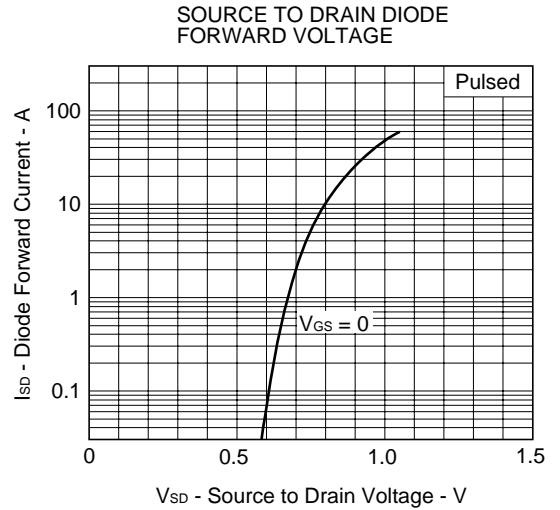
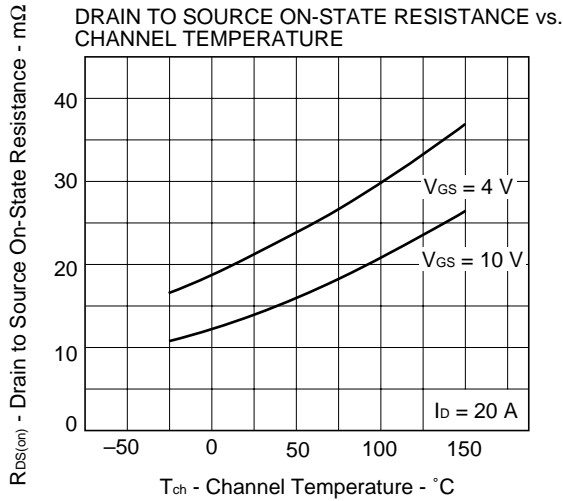


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





**REFERENCE**

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

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