

SL1496C SL1596C

DOUBLE-BALANCED MODULATOR/DEMODULATOR

The SL1596C and SL1496C are versatile monolithic integrated circuit double balanced modulators/demodulators, designed for use where the output voltage is the product of the signal input voltage and the switching carrier voltage. The SL1596C has an operating temperature range of -55°C to $+125^{\circ}\text{C}$, whilst that of the SL1496C is 0°C to $+70^{\circ}\text{C}$.

FEATURES

- Carrier Suppression
 - 65dB Typ.
 - @ 500 kHz
 - 50dB Typ.
 - @ 10 MHz
- Common Mode Rejection 85dB Typ.
- Gain and Signal Handling Both Adjustable
- Balanced Inputs and Outputs

APPLICATIONS

- DSB, DSBSC, AM Modulation
- Synchronous Detection
- FM Detection
- Phase Detection
- Telephone FDM Systems

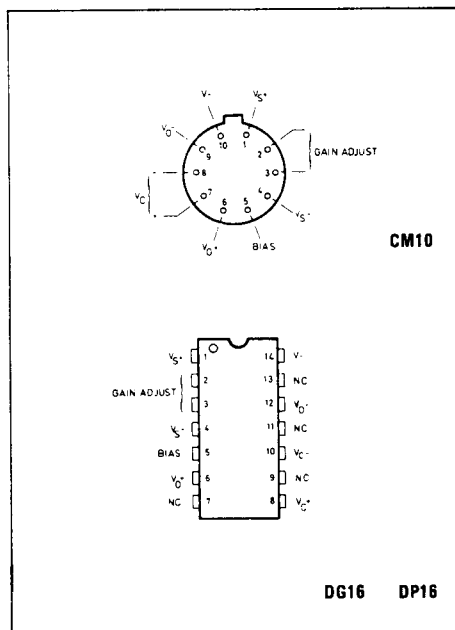
ORDERING CODES

SL1496C — CM, SL1496C — DG, SL1496C — DP
 SL1596C — CM, SL1596C — DG

ABSOLUTE MAXIMUM RATINGS

(Pin number reference to CM package)

Applied voltage*	30V
Differential input signal (V_7-V_8)	$\pm 5\text{V}$
Differential input signal (V_4-V_1)	$\pm (5+15R_E)\text{V}$
Bias current (I_S)	10mA
Operating temperature range	
SL1496C	0°C to $+70^{\circ}\text{C}$
SL1596C	-55°C to $+125^{\circ}\text{C}$



CM Package

Storage temperature range	-55°C to $+175^{\circ}\text{C}$
Junction temperature	$+175^{\circ}\text{C}$
Package dissipation (25°C)	680mW

DG Package

Storage temperature range	-55°C to $+175^{\circ}\text{C}$
Junction temperature	$+175^{\circ}\text{C}$
Package dissipation (25°C)	600mW

DP Package

Storage temperature range	-55°C to $+125^{\circ}\text{C}$
Junction temperature	$+125^{\circ}\text{C}$
Package dissipation (25°C)	500mW

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):—

 $V^+ = +12\text{V DC}$, $V^- = -8\text{V DC}$, $I_S = 1.0\text{ mA DC}$, $R_L = 3.9\text{ k}\Omega$, $R_G = 1.0\text{ k}\Omega$, $T_A = +25^\circ\text{C}$

All input and output characteristics single-ended, unless otherwise stated.

Characteristic*	SL1596			SL1496			Units
	Min	Typ	Max	Min	Typ	Max	
Carrier Feedthrough							$\mu\text{V(rms)}$
$V_C = 60\text{ mV(rms)}$ sinewave and offset adjusted to zero	—	40	—	—	40	—	mV(rms)
$f_C = 1.0\text{ kHz}$ $f_C = 10\text{ MHz}$	—	140	—	—	140	—	
$V_C = 300\text{ mVp-p}$ square wave offset adjusted to zero	—	0.04	0.2	—	0.04	0.4	dB
offset not adjusted	—	20	100	—	20	200	
Carrier Suppression							V/V
$f_S = 10\text{ kHz}$, 300 mV(rms) $f_C = 500\text{ kHz}$, 60 mV(rms) sinewave	50	65	—	40	65	—	$\text{k}\Omega$
$f_C = 10\text{ MHz}$, 60 mV(rms) sinewave	—	50	—	—	50	—	
Signal Gain	2.5	3.5	—	2.5	3.5	—	pF
$V_S = 100\text{ mV(rms)}$, $f = 1.0\text{ kHz}$, $ V_C = 0.5\text{ V DC}$							$\text{k}\Omega$
Single-Ended Input Impedance, Signal Port, $f = 5.0\text{ MHz}$	—	200	—	—	200	—	pF
Parallel Input Resistance	—	2.0	—	—	2.0	—	$\text{k}\Omega$
Parallel Input Capacitance	—	—	—	—	—	—	pF
Single-Ended Output Impedance, $f = 10\text{ MHz}$	—	40	—	—	40	—	pF
Parallel Output Resistance	—	5.0	—	—	5.0	—	μA
Parallel Output Capacitance	—	—	—	—	—	—	$\text{nA}/^\circ\text{C}$
Input Bias Current		12	25	—	12	30	μA
$\frac{I_1 + I_4}{2}$, $\frac{I_7 + I_8}{2}$							μA
Input Offset Current		0.7	5.0	—	0.7	7.0	$\text{nA}/^\circ\text{C}$
$(I_1 - I_4)$, $(I_7 - I_8)$	—	2.0	—	—	2.0	—	μA
Average Temperature Coefficient of Input Offset Current ($T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$)	—	14	50	—	14	80	$\text{nA}/^\circ\text{C}$
Output Offset Current	—	90	—	—	90	—	Vp-p
$(I_6 - I_9)$	—	—	—	—	—	—	dB
Average Temperature Coefficient of Output Offset Current ($T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$)	—	5.0	—	—	5.0	—	V DC
Common-Mode Input Swing, Signal Port, $f_S = 1.0\text{ kHz}$	—	85	—	—	-85	—	Vp-p
Common-Mode Gain, Signal Port, $f_S = 1.0\text{ kHz}$, $ V_C = 0.5\text{ V DC}$	—	8.0	—	—	8.0	—	mW
Common-Mode Quiescent Output Voltage (Pin 6 or Pin 9)	—	8.0	—	—	8.0	—	mW
Differential Output Voltage Swing Capability	—	2.0	3.0	—	2.0	4.0	mW
Power Supply Current	—	3.0	4.0	—	3.0	5.0	mW
$I_6 + I_9$ I_{10}	—	33	—	—	33	—	mW
DC Power Dissipation	—	—	—	—	—	—	

*Pin numbers are given for TO-5 package.

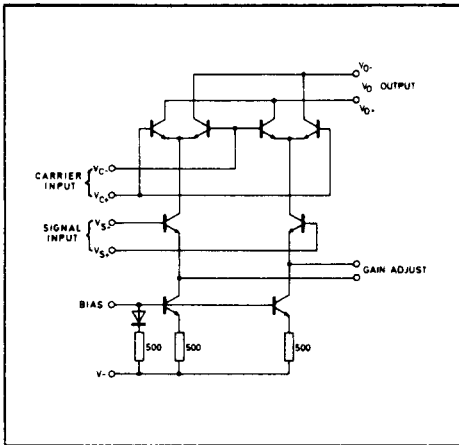


Fig. 2 Circuit diagram

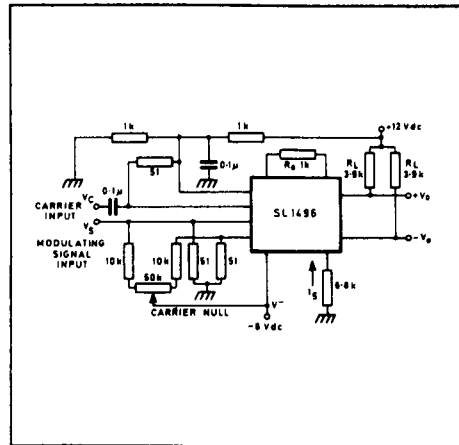


Fig. 3 Typical modulator circuit