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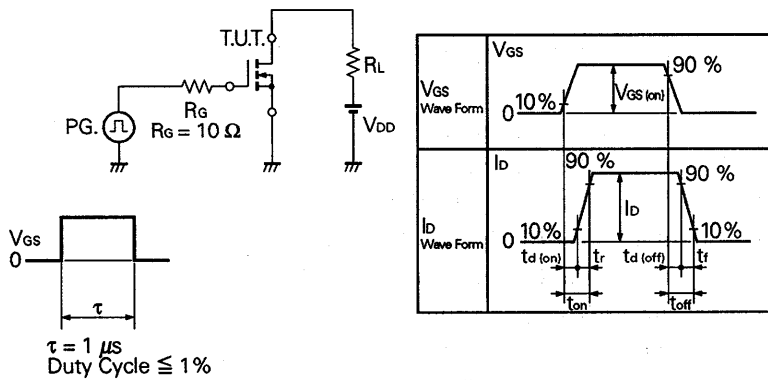
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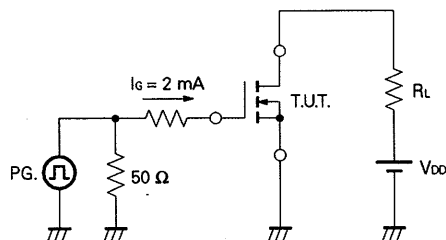
**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		35	45	mΩ	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 13 A
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		45	60	mΩ	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 13 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	1.0		2.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	12	25		S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 13 A
Drain Leakage Current	I <sub>DSS</sub>			10	μA	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		2 200		pF	V <sub>DS</sub> = 10 V
Output Capacitance	C <sub>oss</sub>		750		pF	V <sub>GS</sub> = 0
Reverse Transfer Capacitance	C <sub>rss</sub>		180		pF	f = 1 MHz
Turn-On Delay Time	t <sub>d(on)</sub>		30		ns	V <sub>GS(on)</sub> = 10 V
Rise Time	t <sub>r</sub>		240		ns	V <sub>DD</sub> = 30 V
Turn-Off Delay Time	t <sub>d(off)</sub>		200		ns	I <sub>D</sub> = 15 A, R <sub>G</sub> = 10 Ω
Fall Time	t <sub>f</sub>		140		ns	R <sub>L</sub> = 2.0 Ω
Total Gate Charge	Q <sub>G</sub>		50		nC	V <sub>GS</sub> = 10 V
Gate to Source Charge	Q <sub>GS</sub>		10		nC	I <sub>D</sub> = 30 A
Gate to Drain Charge	Q <sub>GD</sub>		10		nC	V <sub>DD</sub> = 48 V
Diode Forward Voltage	V <sub>SD</sub>		1.1		V	I <sub>SD</sub> = 25 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		130		ns	I <sub>F</sub> = 30 A, V <sub>GS</sub> = 0
Reverse Recovery Charge	Q <sub>rr</sub>		220		nC	di/dt = 50 A/μs

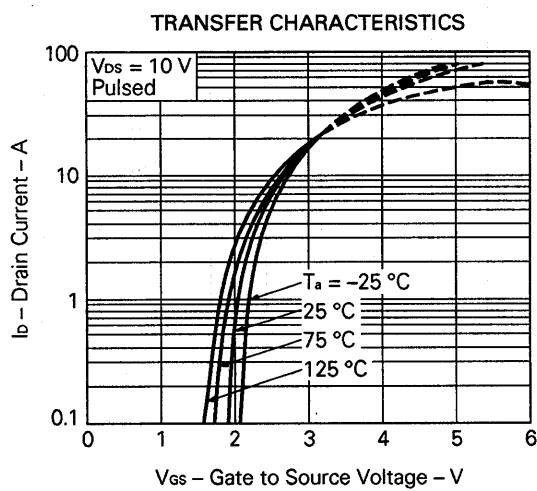
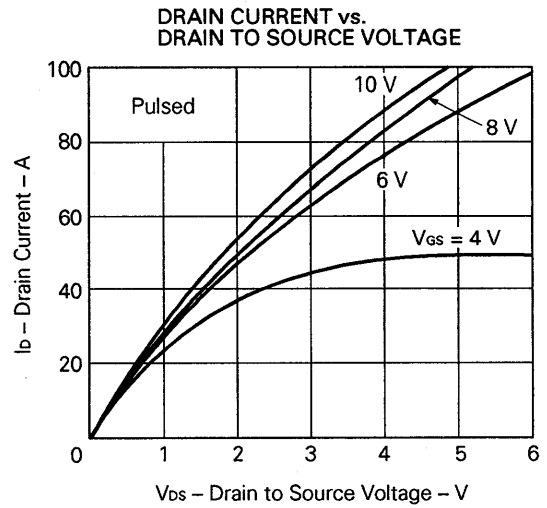
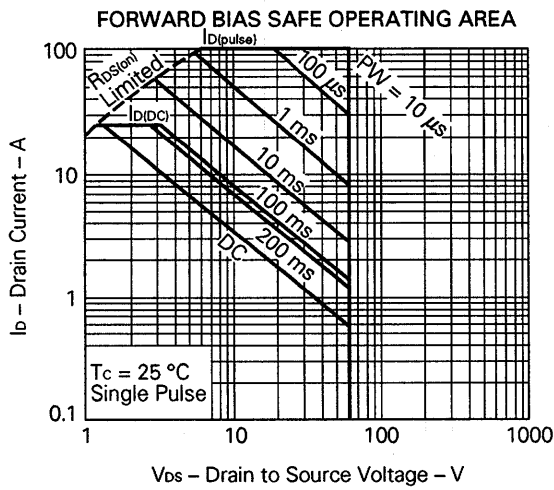
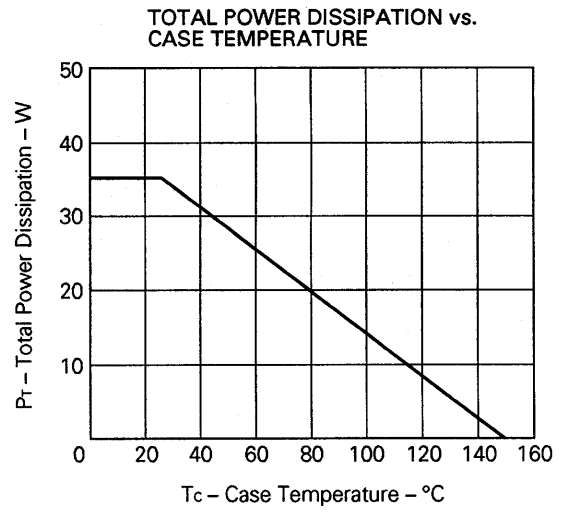
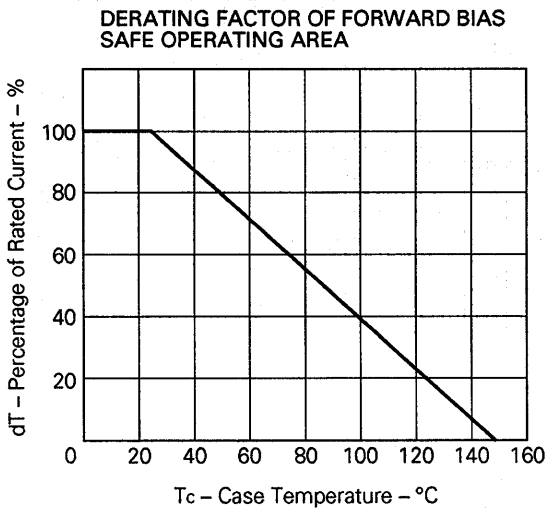
**Test Circuit 1: Switching Time**

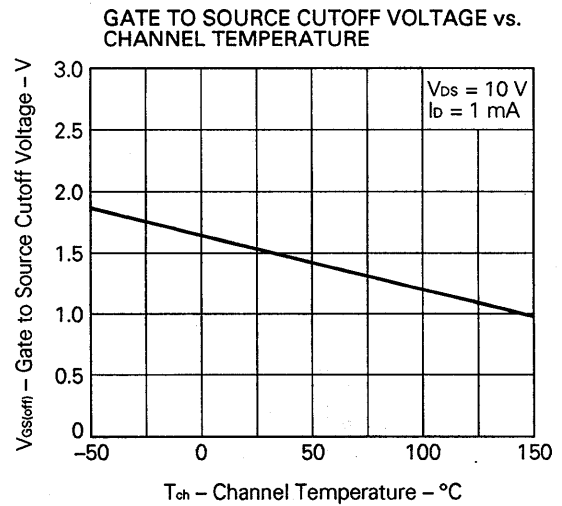
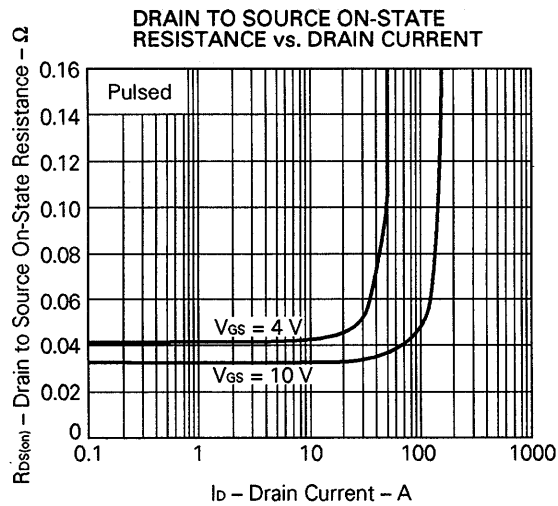
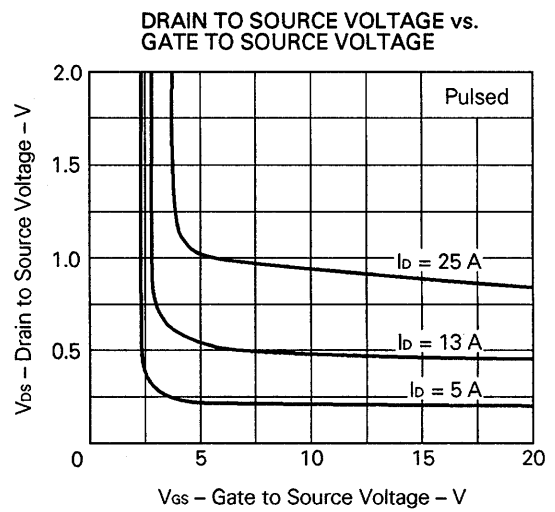
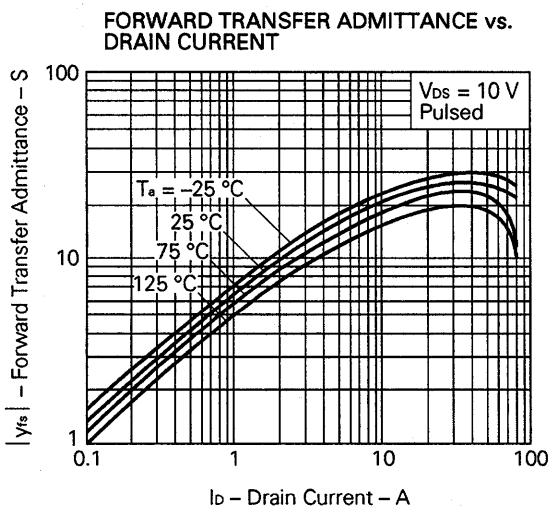
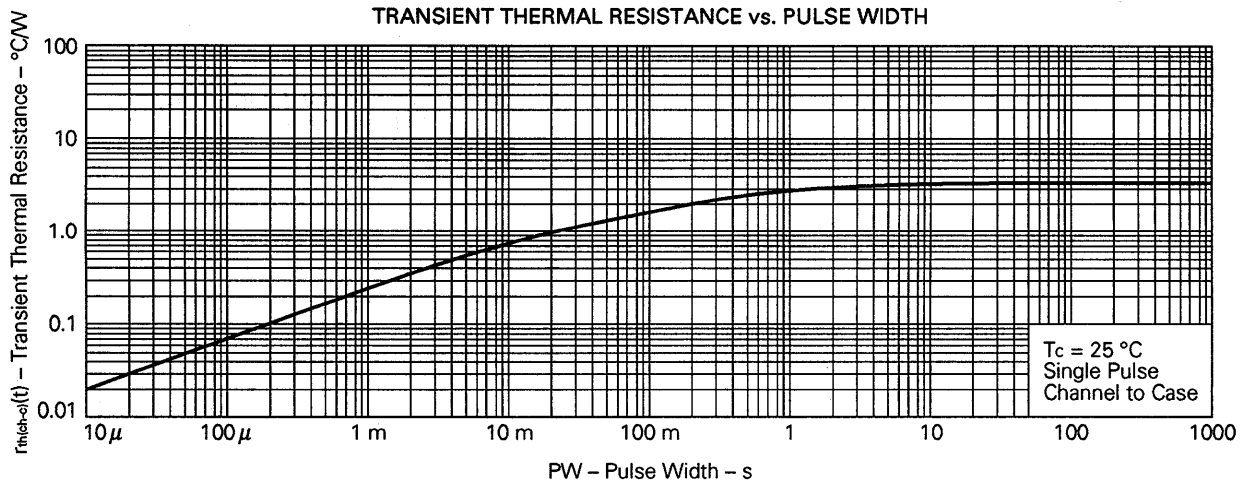


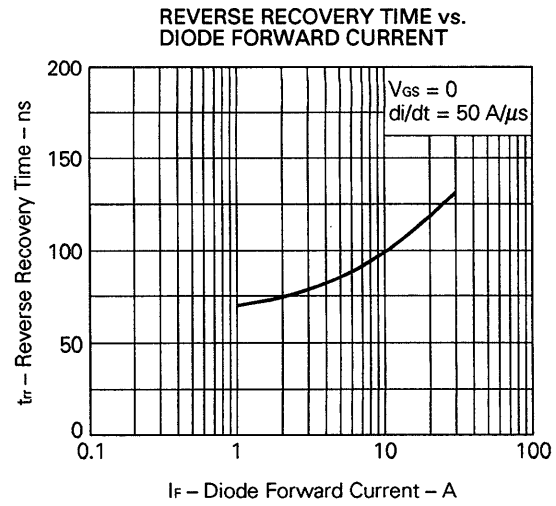
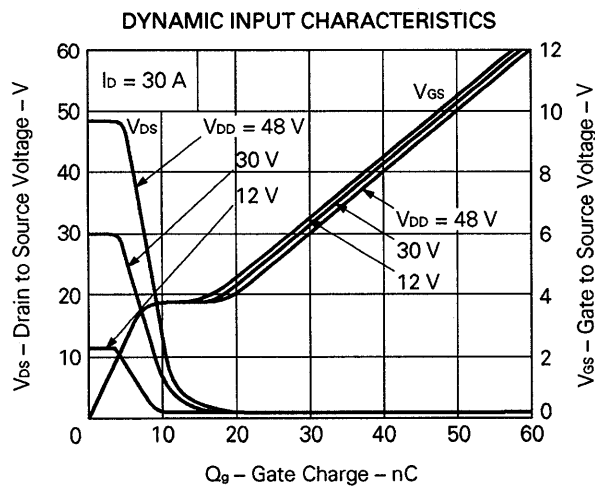
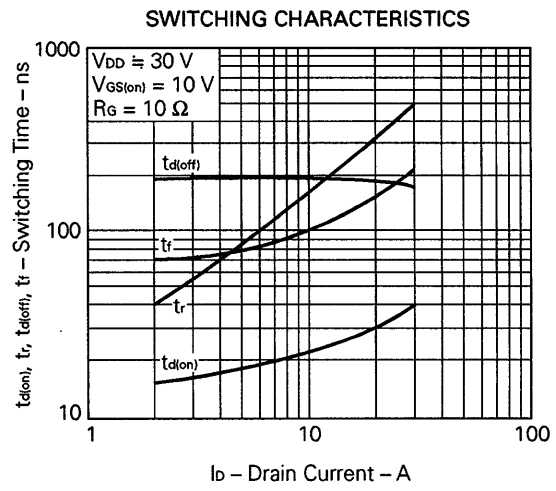
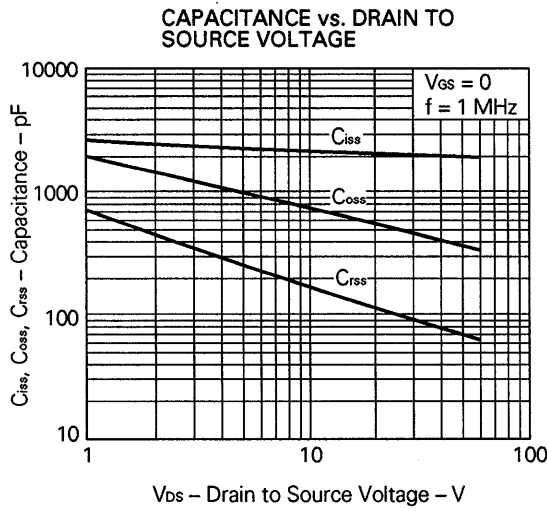
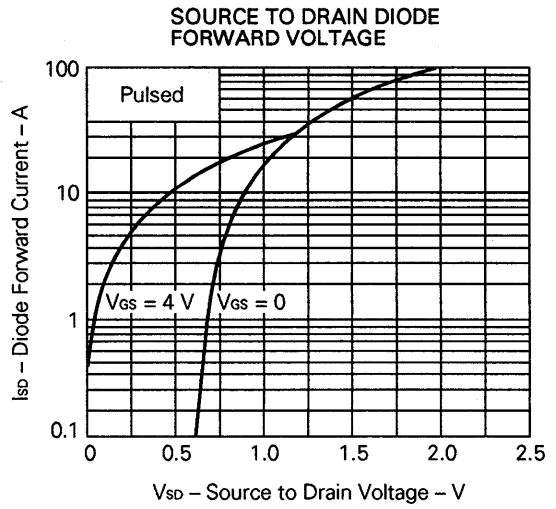
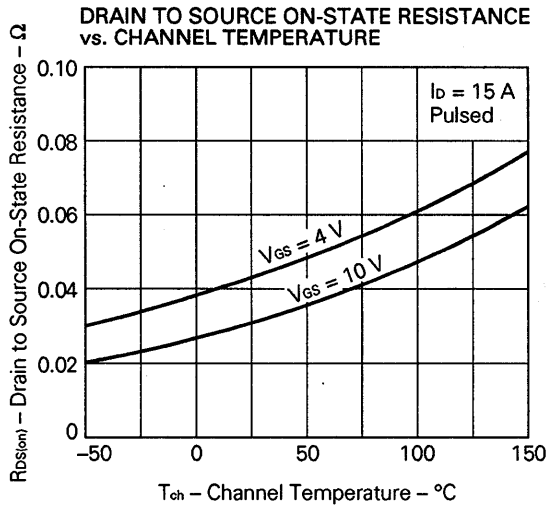
**Test Circuit 2: Gate Charge**



TYPICAL CHARACTERISTICS ( $T_a = 25\text{ }^\circ\text{C}$ )







**Reference**

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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