

Presetable Up/Down Counter

High-Voltage Silicon-Gate CMOS

The SL4029B consists of a four-stage binary or BCD-decade up/down counter with provisions for look-ahead carry in both counting modes. The inputs consists of a single CLOCK, CARRY IN,(CLOCK ENABLE), BINARY/DECADE, UP/DOWN, PRESET ENABLE, and four individual JAM signals. Q1, Q2, Q3, Q4 and a CARRY OUT signal are provided as outputs.

A high PRESET ENABLE signal allows information on the JAM INPUTS to preset the counter to any state asynchronously with the clock. A low on each JAM line, when the PRESET-ENABLE signal is high, resets the counter to its zero count. The counter is advanced one count at the positive transition of the clock when the CARRY IN and PRESET ENABLE signals are low. Advancement is inhibited when the CARRY IN or PRESET ENABLE signals are high. The CARRY OUT signal is normally high and goes low when the counter reaches its maximum count in the UP mode or the minimum count in the DOWN mode provided the CARRY IN signal is low. The CARRY IN signal in the low state can thus be considered a CLOCK ENABLE. The CARRY IN terminal must be connected to GND when not in use.

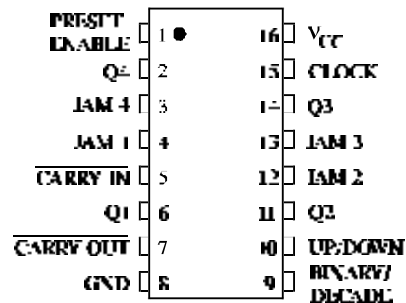
Binary counting is accomplished when the BINARY/DECADE input is high; the counter counts in the decade mode when the BINARY/DECADE input is low. The counter counts up when the UP/DOWN input is high, and down when the UP/DOWN input is low.

Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

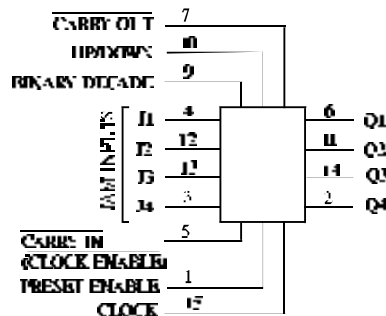
- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 - 1.0 V min @ 5.0 V supply
 - 2.0 V min @ 10.0 V supply
 - 2.5 V min @ 15.0 V supply



PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 16=V_{CC}
 PIN 8=GND

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V _{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±10	mA
P _D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750	mW
		500	
P _D	Power Dissipation per Output Transistor	100	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

SL4029B

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} = 0.5 V or V _{CC} - 0.5V V _{OUT} = 1.0 V or V _{CC} - 1.0 V V _{OUT} = 1.5 V or V _{CC} - 1.5V	5.0	3.5	3.5	3.5	V
			10	7	7	7	
			15	11	11	11	
V _{IL}	Maximum Low-Level Input Voltage	V _{OUT} = 0.5 V or V _{CC} - 0.5V V _{OUT} = 1.0 V or V _{CC} - 1.0 V V _{OUT} = 1.5 V or V _{CC} - 1.5V	5.0	1.5	1.5	1.5	V
			10	3	3	3	
			15	4	4	4	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =GND or V _{CC}	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =GND or V _{CC}	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
I _{IN}	Maximum Input Leakage Current	V _{IN} = GND or V _{CC}	18	±0.1	±0.1	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = GND or V _{CC}	5.0	5	5	150	μA
			10	10	10	300	
			15	20	20	600	
			20	100	100	3000	
I _{OL}	Minimum Output Low (Sink) Current	V _{IN} = GND or V _{CC} U _{OL} =0.4 V U _{OL} =0.5 V U _{OL} =1.5 V	5.0	0.64	0.51	0.36	mA
			10	1.6	1.3	0.9	
			15	4.2	3.4	2.4	
I _{OH}	Minimum Output High (Source) Current	V _{IN} = GND or V _{CC} U _{OH} =2.5 V U _{OH} =4.6 V U _{OH} =9.5 V U _{OH} =13.5 V	5.0	-2	-1.6	-1.15	mA
			5.0	-0.64	-0.51	-0.36	
			10	-1.6	-1.3	-0.9	
			15	-4.2	-3.4	-2.4	



AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, $R_L=200\text{k}\Omega$, Input $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			≥-55°C	25°C	≤125°C	
t _{max}	Maximum Clock Frequency (Figure 1)	5.0	2	2	1	MHz
		10	4	4	2	
		15	5.5	5.5	2.75	
t _{PHL} , t _{PLH}	Maximum Propagation Delay, Clock to Q (Figure 1)	5.0	500	500	1000	ns
		10	240	240	480	
		15	180	180	360	
t _{PHL} , t _{PLH}	Maximum Propagation Delay, Clock to Carry Output (Figure 1)	5.0	560	560	1120	ns
		10	260	260	520	
		15	190	190	380	
t _{PHL} , t _{PLH}	Maximum Propagation Delay, Preset Enable to Q (Figure 1)	5.0	470	470	940	ns
		10	200	200	400	
		15	160	160	320	
t _{PHL} , t _{PLH}	Maximum Propagation Delay, Preset Enable to Carry Output (Figure 1)	5.0	640	640	1280	ns
		10	290	290	580	
		15	210	210	420	
t _{PHL} , t _{PLH}	Maximum Propagation Delay, Carry Input to Carry Output (Figure 1)	5.0	340	340	680	ns
		10	140	140	280	
		15	100	100	200	
t _{THL} , t _{TLH}	Maximum Output Transition Time, Any Output (Figure 1)	5.0	200	200	400	ns
		10	100	100	200	
		15	80	80	160	
C _{IN}	Maximum Input Capacitance	-		7.5		pF

FUNCTION TABLE

CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC (B/D)	H	BINARY COUNT
	L	DECADE COUNT
UP/DOWN (U/D)	H	UP COUNT
	L	DOWN COUNT
PRESET ENABLE (PE)	H	JAM IN
	L	NO JAM
CARRY IN (CI) (CLOCK ENABLE)	H	NO COUNTER ADVANCE AT POS. CLOCK TRANSITION
	L	ADVANCE COUNTER AT POS. CLOCK TRANSITION

SL4029B

TIMING REQUIREMENTS ($C_L=50\text{pF}$, $R_L=200\text{ k}\Omega$, Input $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			≥-55°C	25°C	≤125°C	
t _w	Minimum Pulse Width, Clock (Figure 1)	5.0	180	180	360	ns
		10	90	90	180	
		15	60	60	120	
t _w	Minimum Pulse Width, Preset Enable (Figure 1)	5.0	130	130	260	ns
		10	70	70	140	
		15	50	50	100	
t _{su} *	Minimum Setup Time, Clock to B/D or U/D (Figure 1)	5.0	340	340	680	ns
		10	140	140	280	
		15	100	100	200	
t _{rem} *	Minimum Removal Time, Preset Enable (Figure 1)	5.0	200	200	400	ns
		10	110	110	220	
		15	80	80	160	
t _h **	Minimum Hold Time, Clock to Carry In (Figure 2)	5.0	50	50	100	ns
		10	30	30	60	
		15	25	25	50	
t _{su}	Minimum Setup Time, Carry In to Clock (Figure 1)	5.0	200	200	400	ns
		10	70	70	140	
		15	60	60	120	
t _r , t _f **	Maximum Input Rise and Fall Times, Clock (Figure 2)	5.0	15	15	30	μs
		10	15	15	30	
		15	15	15	30	

* From Up/Down, Binary/Decode, Carry In, or Preset Enable Control Inputs to Clock Edge.

** From Carry In to Clock Edge

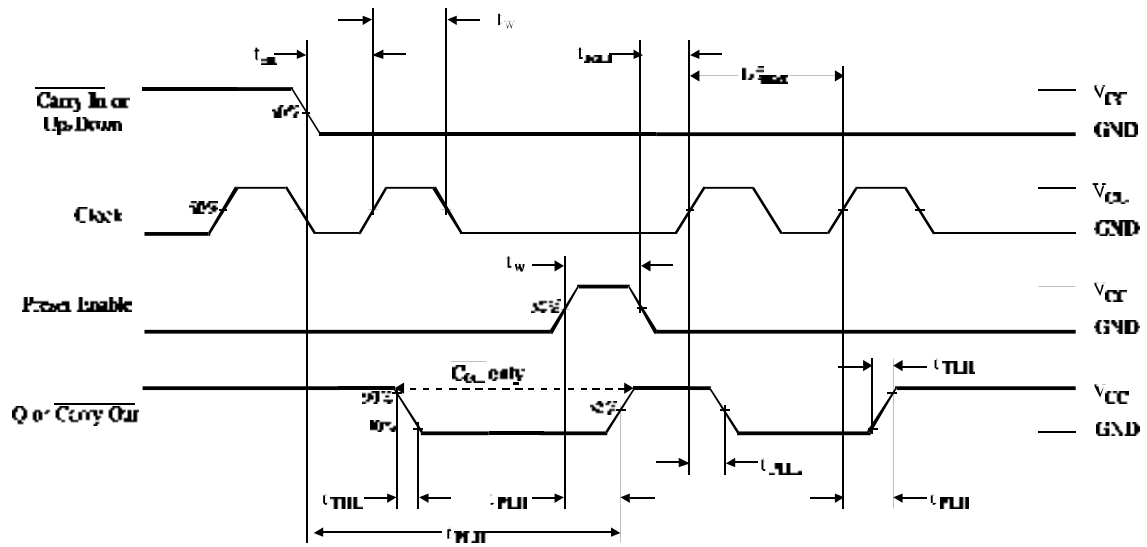


Figure 1. Switching Waveforms

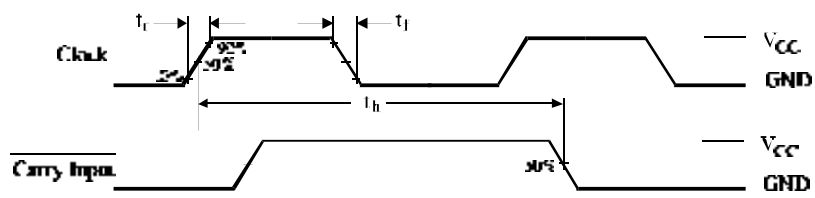
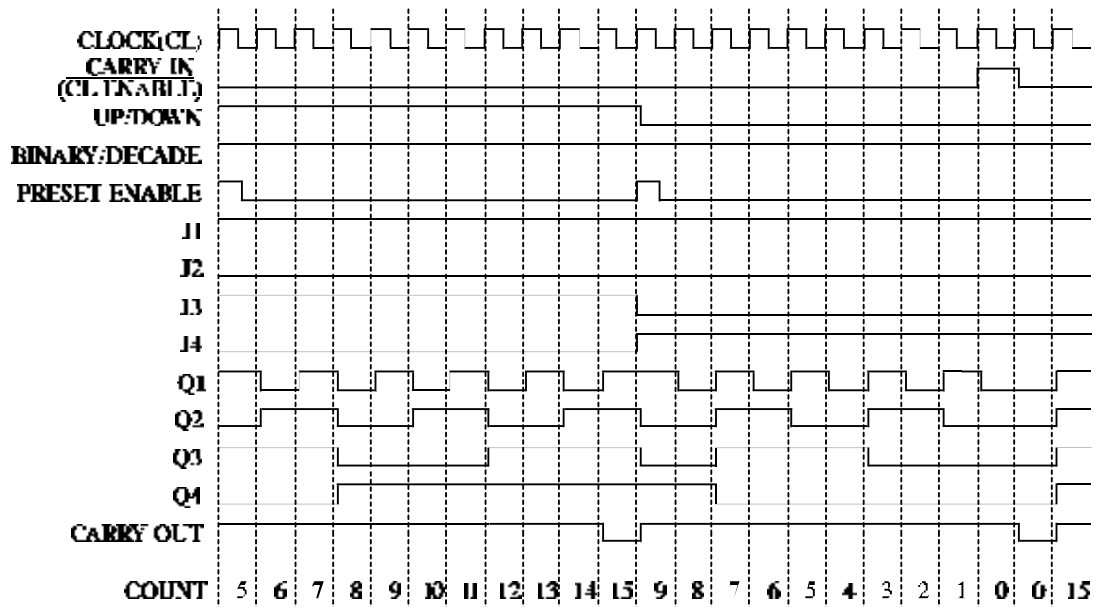
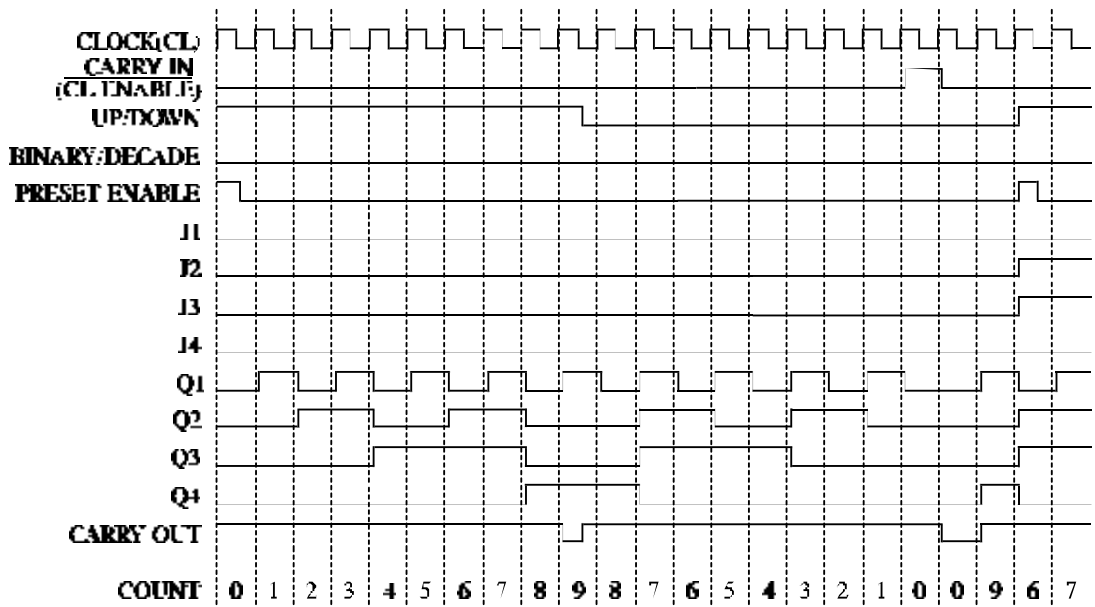


Figure 2. Switching Waveforms

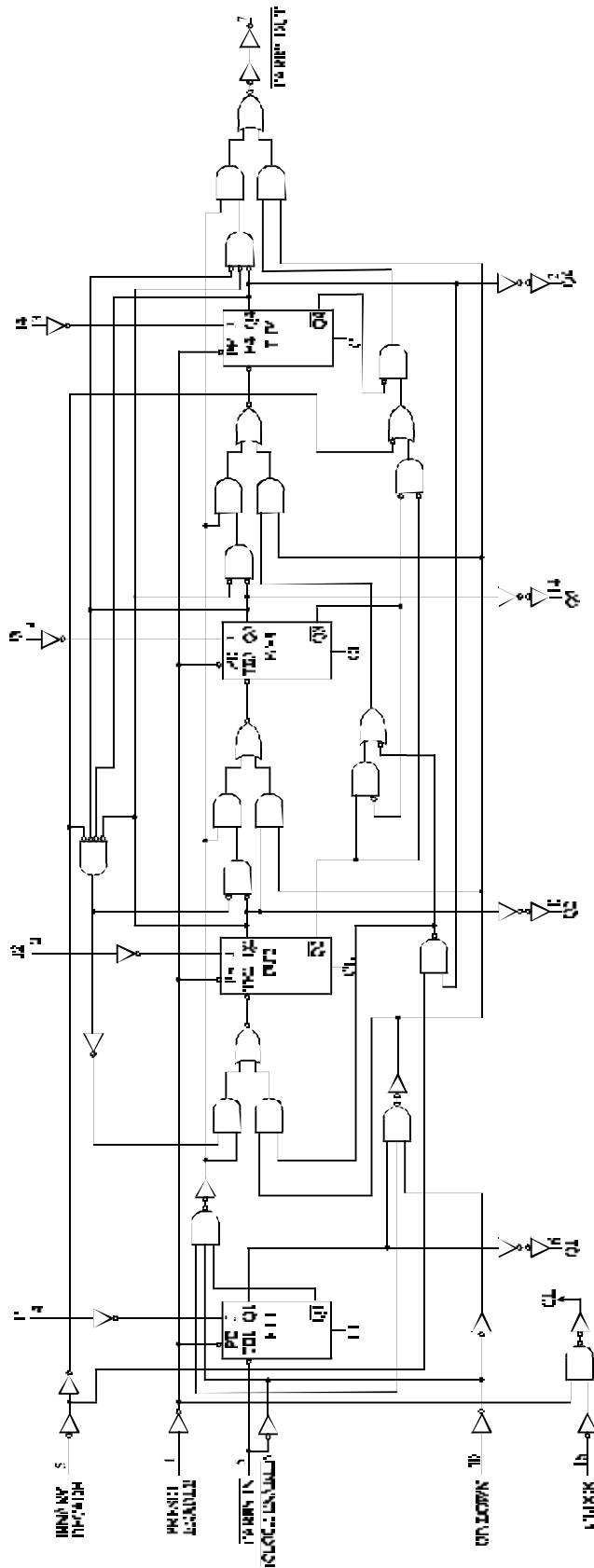
TIMING DIAGRAM; binary mode; J1=HIGH; J2=LOW; BIN/DEC=HIGH



TIMING DIAGRAM; decade mode; J1=LOW; J4=LOW; BIN/DEC=LOW



EXPANDED LOGIC DIAGRAM



TRUTH TABLE

CLOCK	TE	PE	J	K	Q	\bar{Q}
X	X	L	L	L	L	H
	L	H	X	X	Q	\bar{Q}
X	X	L	H	H	H	L
	H	H	X	X	Q	\bar{Q} NC
	X	H	X	X	Q	\bar{Q} NC

