Preliminary Information [1] *(See Last Page)*

Single & Dual Programmable Buck Regulators with Integrated MOSFETs and Digital Control

FEATURES & APPLICATIONS

Features

- **Single/Dual Step-Down DC-DC Outputs**
  - **Integrated power MOSFET switches**
  - **1A/2A/4A output current with built in current limit**
  - **Input voltage range: +4.5V to +16V**
  - **+0.8V to +5.0V output voltage (+/-2.5% accuracy)**
  - **Automatic PFM mode for light load efficiency**
  - **180^0 phase interleave (SMB207/A/208/A)**
  - **Integrated frequency compensation**
  - **Input undervoltage lockout (UVLO)**
- **Integrated Power Control and Programmability**
  - **I^2C Digital or Pin Control**
  - **Coarse and Fine Output Voltage Setting**
    - **16-level "Coarse" nominal setpoint**
      - **+0.8V to +1.8V @ 100mV/step**
      - **+2.5/2.3/3.0/3.3/5.0V**
    - **8-level "Fine" Margining (20XA only)**
      - **+1.14% to +7.95% (vs. coarse setting)**
  - **PWM frequency: 500kHz or 1MHz**
  - **Output up/down sequence (SMB207/A/208/A)**
  - **Digital output softstart/stop**
  - **Output UV monitoring with PGOOD/RESET output**
  - **Independent output enable pins (SMB207/A/208/A)**

Applications

- **Digital LCD/Plasma TV**
- **Digital Set-Top Box/PVR/DVR**
- **Datacom/Telecom Equipment**

INTRODUCTION

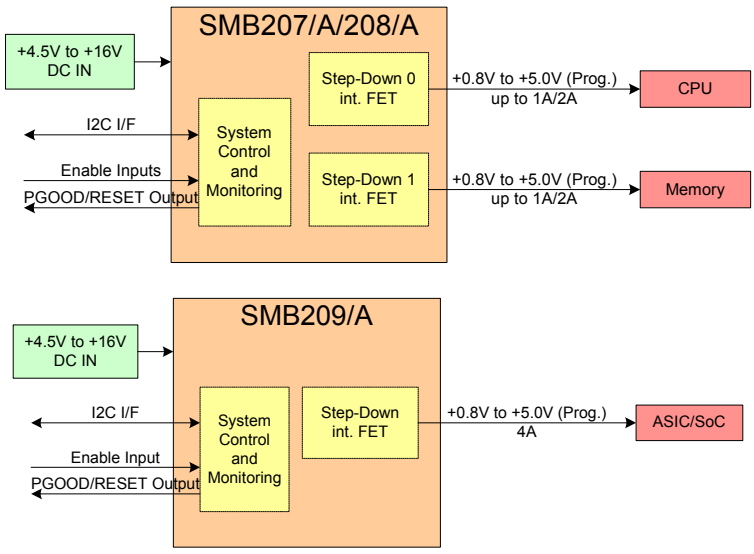
The SMB20X/20XA are a highly integrated and flexible Single/Dual-output DC-DC regulator designed for use in a wide variety of applications. High integration reduces system cost, component count and development time while the built-in non-volatile digital programmability allows system designers to custom tailor the device to suit almost any application.

The SMB20X/20XA include single/dual DC-DC step-down regulators with integrated high-side MOSFET switches for up to 1A/2A/4A continuous output current. Programmable output voltages as low as +0.8V support the latest VLSI digital cores. Minimum external components result in a very compact solution size for space constrained applications.

Also sophisticated power control/monitoring functions required by many systems are built-in and accessible via digital I^2C interface. These include digitally programmable output voltage setpoint, power-up/down softstart and sequencing, independent enable/disable, output UV monitoring with Power Good/Reset output. Additionally on the SMB20XA fine resolution voltage margining is provided to allow for sophisticated system optimization.

The integration of features and built-in flexibility of the SMB20X/20XA allow the system designer to create a "platform solution" that can be easily modified without hardware changes. The SMB20X/20XA are well suited to applications with an input range of +4.5 to +16V. The operating temperature range is -40^oC to $+85^oC$ and the available package is a 3mm X 3mm 20-pad QFN.

Figure 1 - SIMPLIFIED APPLICATION



GENERAL DESCRIPTION

Digital Interface/Non-Volatile Programming

The built-in serial digital I2C/SMBus compatible port and built-in non-volatile programming bring several benefits to power supply design with the SMB20X/20XA. Many external components are eliminated that would otherwise be used to set configuration and parametric values. Additionally the digital interface allows for quick and easy development and debug without hardware changes. Finally, after the non-volatile power-up configuration the serial port can used to re-program the SMB20X/20XA by host software after the system is running. For quick programming development and debug use Summit's prebuilt evaluation kit including a PC-based graphical user interface (GUI).

Single/Dual PWM DC-DC Regulators

The SMB20X/20XA contain one/two integrated PWM DC-DC step-down (buck) regulator(s). In the SMB207A/208/A both regulators are identical and share the same features and functions. The input voltage range is +4.5V to +16V to support a wide variety of system applications. The outputs support a full 1A/2A/4A continuous output current with built-in cycle-by-cycle current limit. The output voltage range is similarly flexible over +0.8V and +5.0V and fully programmable in non-volatile (static) or volatile (dynamic, on-the-fly) via the serial digital interface. The nominal "coarse" voltage programming provides flexibility for various types of loads without hardware changes. In the SMB20XA the "fine" programming provides "margining" capability for sophisticated system validation and optimization

Built-in high-side MOSFETs work in conjunction with external Schottky diode rectifiers in constant frequency PWM-mode at high load currents or high efficiency pulse skipping PFM-mode at light loads. Switching frequency is programmable (500kHz/1000kHz) to trade off efficiency and component size. Each output (SMB207A/208/A) switches 180^{o} out of phase with the other to reduce input ripple current, switching noise and input capacitance requirement. Bootstrapped high-side drive improves efficiency and extends operating voltage range. Frequency compensation is fully integrated to further reduce component count and cost.

Power Control/Management Functions

The SMB20X/20XA integrate several power management functions that are typically otherwise performed by external circuits. These include output sequencing with programmable timing, hardware or software-based output enable/disable, and programmable softstart timing. Also the output voltages are monitored with a programmable PGOOD/RESET output (PGOOD asserts immediately, RESET delays 125ms). Software Enable bits and hardware Enable pins work together to provide flexible power up/down and manual/auto sequencing

The SMB20X/20XA also support digitally programmable output voltage. The non-volatile setting determines the power-up/static value but it can be re-programmed by software via the serial interface. The settings are +0.8V to +1.8V with 100mV step plus +2.5/2.3/3.0/3.3/5.0V settings. This can support dynamic voltage/clock CPU cores or low power memory modes.

Figure 2 - TYPICAL APPLICATION SMB207A/208/A

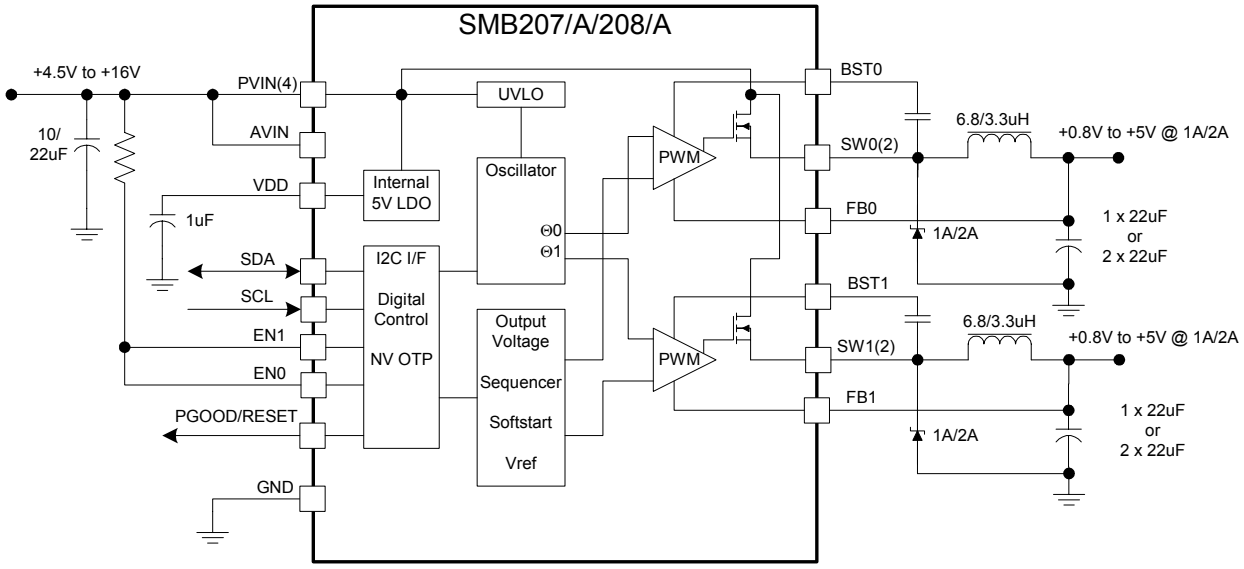
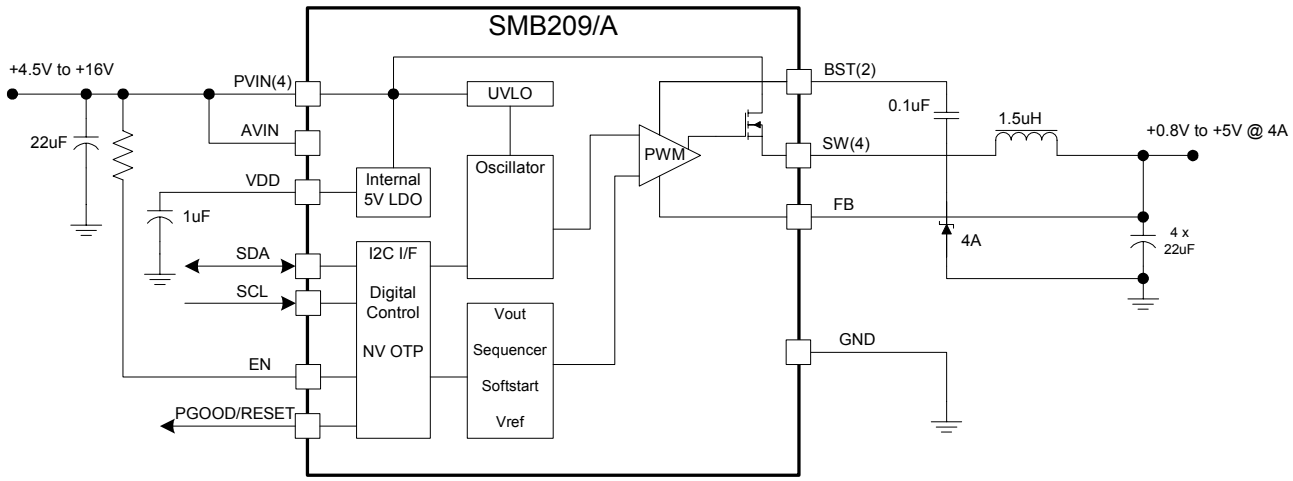


Figure 3 - TYPICAL APPLICATION SMB209



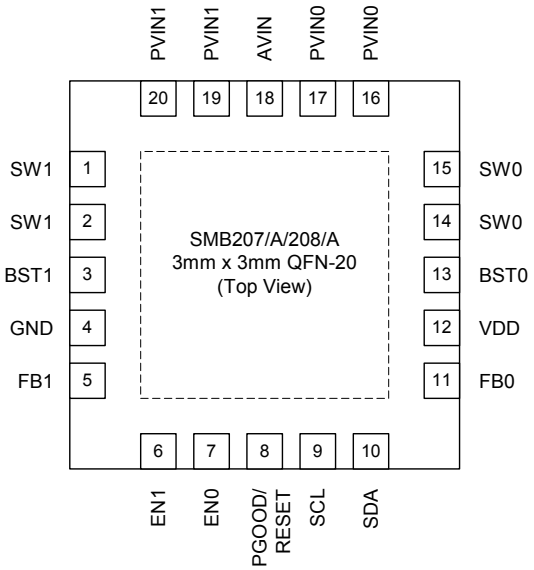
PIN DESCRIPTION (SMB207A/208/A)

SMB207/A/208/A Pin #	Pin Name	Pin Type	Pin Description
16,17,19,20	PVIN(4)	Power	Power Input - Connect to +4.5V to +16V source. Bypass with 10uf (SMB207/A) or 22uF (SMB208/A) typical MLCC
18	AVIN	Power	Analog Power Input - Connect to +4.5V to +16V source (same as PVIN)
12	VDD	Power	Internal VDD - +5V internal supply. Bypass with 1uF typical MLCC
4	GND	Ground	Analog Ground – Connect to PCB isolated ground
9	SCL	Input	I^2C Clock
10	SDA	Input/Output	I^2C Data
7,6	EN(0/1)	Input	Enable0/1 – Enables output, high true
14,15,1,2	SW0/1 (4)	Output	Switch Node 0/1 – Connect to output inductors
13,3	BST0/1	Input	Bootstrap Input – Connect to 0.1uF capacitor to switch node
11,5	FB0/1	Input	Feedback Input 0/1 – Connect to output sense node
8	PGOOD/ RESET	Output	PowerGood/RESET Output – Output UV monitor signal (high true, open drain)

PIN DESCRIPTION (SMB209/A)

SMB209/A Pin #	Pin Name	Pin Type	Pin Description
16,17,19,20	PVIN(4)	Power	Power Input - Connect to +4.5V to +16V source. Bypass with 22uF typical MLCC
18	AVIN	Power	Analog Power Input - Connect to +4.5V to +16V source (same as PVIN)
12	VDD	Power	Internal VDD - +5V internal supply. Bypass with 1uF typical MLCC
4	GND	Ground	Analog Ground – Connect to PCB isolated ground
9	SCL	Input	I^2C Clock
10	SDA	Input/Output	I^2C Data
7	EN	Input	Enable – Enables output, high true
14,15,1,2	SW	Output	Switch Node – Connect to output inductor
13	BST	Input	Bootstrap Input – Connect to 0.1uF capacitor to switch node
11	FB	Input	Feedback Input – Connect to output sense node
8	PGOOD/ RESET	Output	PowerGood/RESET Output – Output UV monitor signal (high true, open drain)
3,5,6	NC	NC	Not Connected

Figure 4 - PACKAGE AND PINOUT



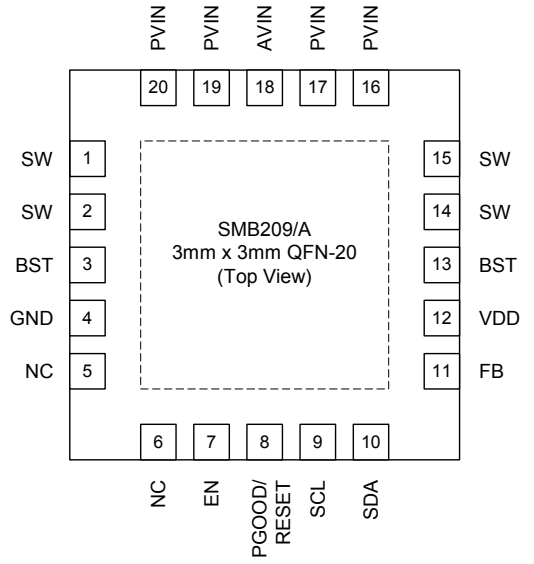


Figure 5 - TYPICAL OUTPUT TIMING DIAGRAM

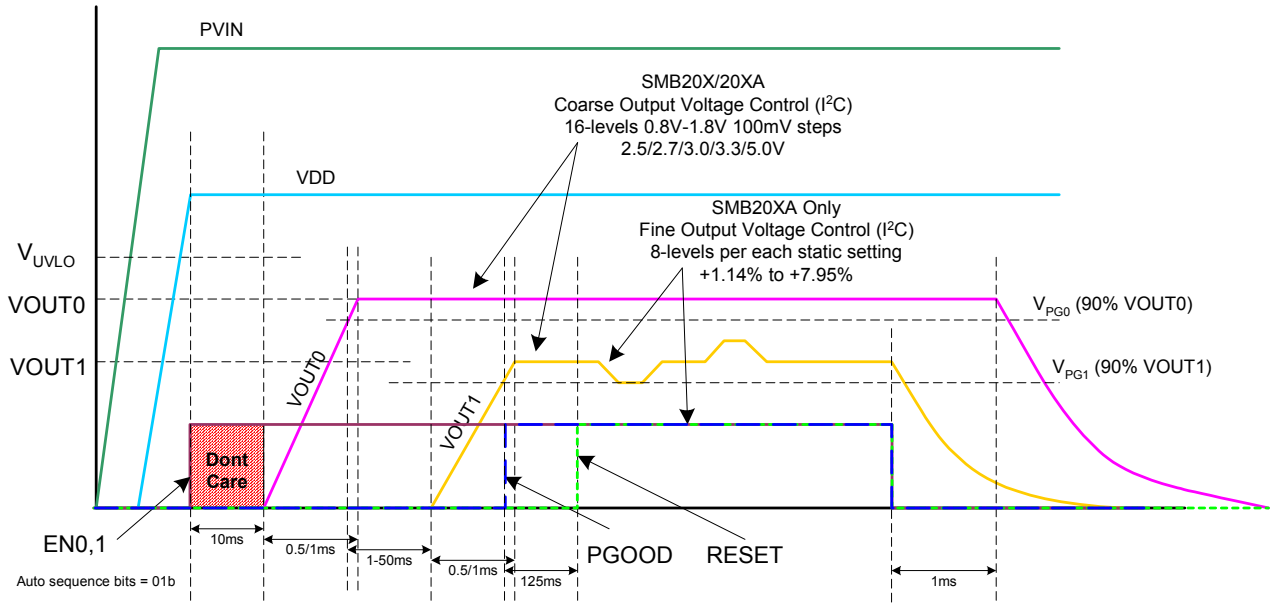
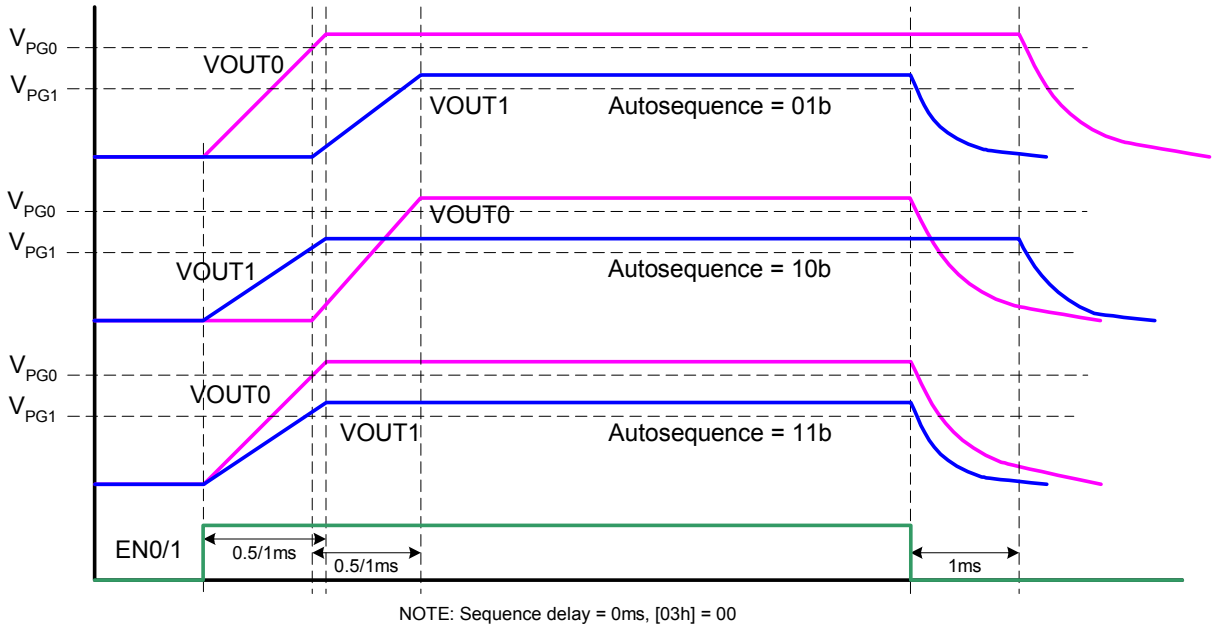


Figure 6 - TYPICAL OUTPUT SEQUENCE DIAGRAM (SMB207/A/208/A)



NOTE: Sequence delay = 0ms, [03h] = 00

OUTPUT STATE/SEQUENCE LOGIC TABLES

Output States (SMB207/A/208/A)

EN0 Pin	EN1 Pin	CH0 enable bit	CH1 enable bit	Chip State	Output behavior	
					CH0	CH1
Low	Low	X	X	Shutdown	Disabled	Disabled
Low	High	X	0	Standby	Disabled	Disabled
High	Low	0	X	Standby	Disabled	Disabled
Low	High	X	1	Active	Disabled	Enabled
High	Low	1	X	Active	Enabled	Disabled
High	High	0	0	Standby	Disabled	Disabled
High	High	0	1	Active	Disabled	Enabled
High	High	1	0	Active	Enabled	Disabled
High	High	1	1	Active	Enabled	Enabled

Output States (SMB209/A)

EN Pin	Enable bit	Chip State	Output behavior
Low	X	Shutdown	Disabled
High	0	Standby	Disabled
High	1	Active	Enabled

NOTE: "X" denotes a "Don't Care" state

Output Sequencing (SMB207/A/208/A)

Auto Sequence Bits [02h bits3:2]		Output behavior*
0	0	CH0/CH1 respond independently to enable pins/bits, no auto-sequence
0	1	CH1 is dependent on CH0 state. CH1 always turns on after and turns off before CH0 (based on PGOOD signals)**
1	0	CH0 is dependent on CH1 state. CH0 always turns on after and turns off before CH1 (based on PGOOD signals)**
1	1	CH0 and CH1 turn on and off together**

**Power down timing is not specifically controlled and is dependent on load current and output capacitance - slew rate is not guaranteed. Assumes input UVLO is cleared. If auto-sequence bit are other than 00b then fault conditions (OC, OT etc.) may shutdown both outputs.*

***Assumes EN pins and enable bits are in the intended states per the Output State Table.*

POWERGOOD/RESET OUTPUT LOGIC TABLE

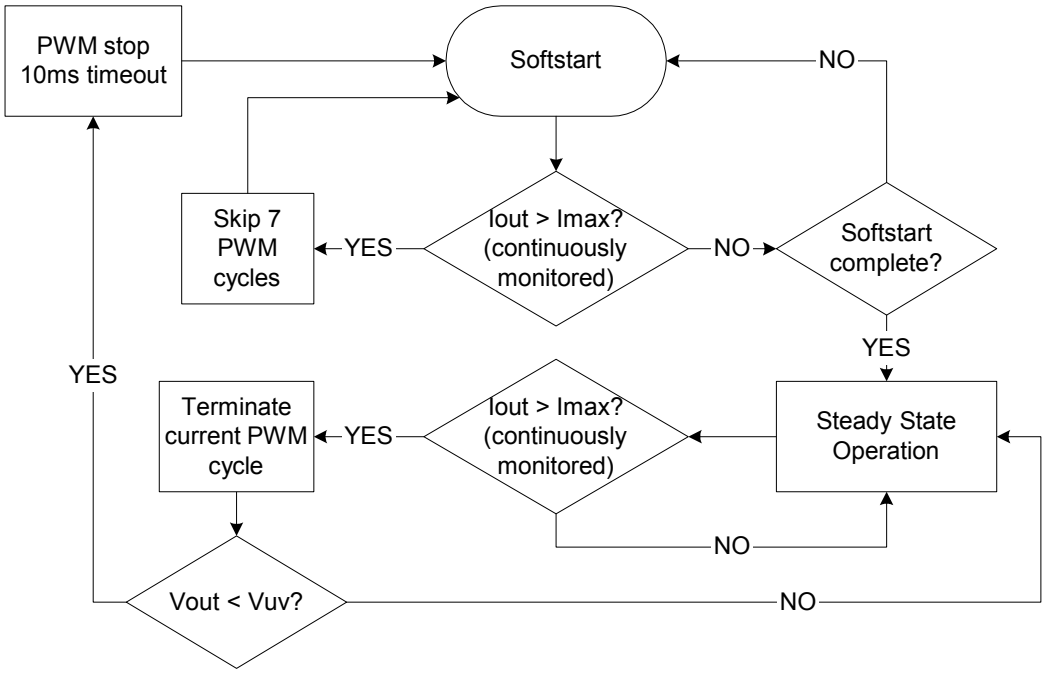
SMB207/A/208/A

PGOOD/RESET Assignment [02h bits7:6]	VOUT0	VOUT1	PGOOD/RESET Output
00	VOUT0 < V_{PG0}	VOUT1 < V_{PG1}	Low
00	VOUT0 < V_{PG0}	VOUT1 > V_{PG1}	Low
00	VOUT0 > V_{PG0}	VOUT1 < V_{PG1}	Low
00	VOUT0 > V_{PG0}	VOUT1 > V_{PG1}	High
01	Don't Care	VOUT1 < V_{PG1}	Low
01	Don't Care	VOUT1 > V_{PG1}	High
10	VOUT0 < V_{PG0}	Don't Care	Low
10	VOUT0 > V_{PG0}	Don't Care	High
11	Don't Care	Don't Care	High

SMB209/A

PGOOD/RESET Assignment [02h bits7:6]	VOUT	PGOOD/RESET Output
10	VOUT < V_{PG}	Low
10	VOUT > V_{PG}	High
11	Don't Care	High

Figure 7 - OVERCURRENT BEHAVIOR (PER OUTPUT)



ABSOLUTE MAXIMUM RATINGS

Storage Temperature..... -65°C to +150°C
Junction Temperature..... -55°C to +150°C
Lead Solder Temperature (10s)..... 300°C
Terminal Voltage with Respect to GND:
PVIN, AVIN, SW, EN0/1 ..... +18V
BST .....PVIN+6.5V
All Others ..... +6.5V
Output Short Circuit Current (Any single pin) 3A
ESD Rating per JEDEC (HBM)..... 2000V
Latch-Up testing per JEDEC..... ±100mA

Note - The device is not guaranteed to function outside its operating rating. Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions outside those listed in the operational sections of the specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability. Devices are ESD sensitive. Handling precautions are recommended.

RECOMMENDED OPERATING CONDITIONS

Ambient Temperature Range ..... -40°C to +85°C
Junction Temperature Range .....-40°C to +125°C
PVIN, AVIN .....+4.5V to +16V
Package Thermal Resistance (θ_{JA})
20 Pad 3mm x 3mm QFN ..... 47°C/W
Moisture Classification ...Level 3 (MSL 3) per J-STD- 020

RELIABILITY CHARACTERISTICS
Data Retention .....20 Years

ELECTRICAL OPERATING CHARACTERISTICS

PVIN = +12V, VDD = +5V, $T_A = T_J$ = -40°C to +85°C unless otherwise noted. Typical values are +25°C, Note 1

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main Supply						
V_{IN}	Main input supply voltage (PVIN)		4.5		16	V
V_{DD}	Internal LDO supply voltage (VDD)	V_{IN}>5.5V (Note 2)	4.75		5.25	V
I_{IN}	Input supply current (PVIN)	Outputs enabled, no load		3	10	mA
$I_{IN-STBY}$	Standby supply current	EN pins high, Output enable bits disabled, I^2C active		0.5	1	mA
$I_{IN-SHDN}$	Shutdown supply current	EN pins low		1	5	uA
I_{DD}	Internal LDO Output Current	VDD>4.5V, Note 2	25			mA
V_{UVLO}	Input Undervoltage lockout (VDD monitored)	VDD Rising	3.75	4.0	4.25	V
		VDD Falling (relative to VDD Rising)		-10		%
T_{SHDN}	Thermal shutdown threshold	Temp rising		140	150	°C
T_{HYST}	Thermal shutdown hysteresis			20		°C

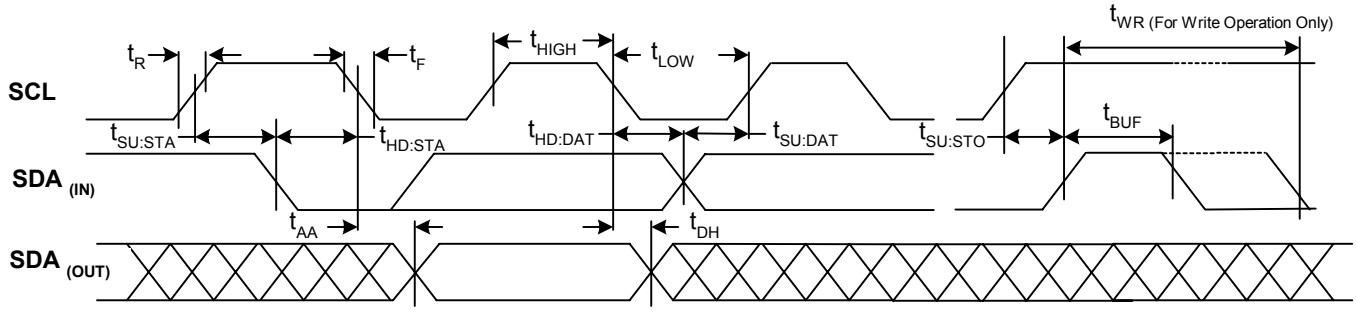
Note 1: Parametric tolerances are only guaranteed for factory-programmed settings. Changing configuration settings from that reflected in the customer specific CSIR code will result in inaccuracies exceeding those specified above.
Note 2: Internal LDO disabled for PVIN < 5.5V and VDD externally connected to PVIN (see Applications Schematic)
Note 3: Dynamic output voltage slew is set by softstart/stop programming. Output UV/OV detectors are blanked during output slew.

ELECTRICAL OPERATING CHARACTERISTICS (CONTINUED)

PVIN = +12V, VDD = +5V, $T_A = T_J$ = -40°C to +85°C unless otherwise noted. Typical values are at +25°C, Note 1						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Step-down regulators (CH0,1)						
V_{OUT}	Coarse Output Voltage	Programmable 0.8V-1.8V (100mV steps) and 2.5/2.3/3.0/3.3/5.0V (4-bits)	-2.5		+2.5	%
SRV_{OUT}	Dynamic Output Voltage Slew Rate (Note 3)	V_{FB} slew from completion of I^2C write (0.8V-1.8V only)		128		us/step
DV_{OUTF}	Fine Output Voltage Offset SMB20XA ONLY	Programmable +1.14% to 7.95% relative to static output voltage (3-bits)	0		+7.95	%
ΔV_{LINE}	Line regulation	$\Delta V_{OUT}/\Delta V_{IN}$ (10V > V_{IN} > 14V)		1	3	mV/V
ΔV_{LOAD}	Load regulation	$\Delta V_{OUT}/\Delta I_{OUT}$ (0.1A > I_{OUT} > 2A)		4	15	mV/A
I_{FB}	Feedback pin current			1		uA
F_{SW}	PWM Switching frequency (SMB207A/208/A)	Programmable 500/1000kHz (1-bit)	-15		15	%
Θ	Phase interleave slots	CH1 vs. CH2		180		deg
R_{DSH}	High side FET switch resistance	SMB207A/208/A		250	400	mΩ
		SMB209/A		125	200	mΩ
R_{DSL}	Low side FET switch resistance			10		Ω
I_{LIM}	Switch Current Limit	SMB207/A		1.5	2	A
		SMB208/A		3	4	A
		SMB209/A		6	8	A
T_{HO}	Startup holdoff time			10		ms
T_{SS}	Softstart/stop and dynamic voltage slew	Programmable 0.5/1.0ms (1 bit)	-20		+20	%
T_{SEQ}	Sequence delay	Programmable 1.5-50ms (2 bits)	-20		+20	%
$V_{PG0,1}$	Output PGOOD/RESET threshold	$V_{OUT0,1}$ rising Relative to nominal coarse setting	85	90	95	%
T_{BPG}	PGOOD/RESET blanking time	After last step of V_{FB} during dynamic output voltage (Note 3)		192		us
T_{UVPG}	Output PGOOD/RESET glitch filter	V_{OUT} falling		32		us
T_{RST}	RESET Output Delay	V_{OUT} rising	100	125	200	ms
V_{UV}	Output undervoltage threshold	% of V_{OUT}, V_{OUT} falling	60	70	80	%
$V_{HYST-UV}$	UV threshold hysteresis	% of V_{OUT}, V_{OUT} rising		3		%
T_{UVGF}	Output UV glitch filter	V_{OUT} falling		32		us
Logic Inputs/Outputs (EN0/1, SDA/SCL, PGOOD)						
V_{IH}	Input high voltage		1.4			V
V_{IL}	Input low				0.6	V
V_{OL}	Open drain outputs	I_{SINK} = 3mA		0.3		V

I²C/SMBus SERIAL INTERFACE ELECTRICAL SPECIFICATIONS

PVIN = +12V, VDD = +5V, T_A = 0°C to +85°C unless otherwise noted. Typical values are +25°C, Note 1						
Symbol	**Parameter**	**Conditions**	**400kHz**			
			Min	**Typ**	**Max**	**Units**
f_{SCL}	SCL clock frequency		0		400	kHz
T_{LOW}	Clock low period		1.3			µs
T_{HIGH}	Clock high period		0.6			µs
t_{BUF}	Bus free time between a STOP and a START condition	Before new transmission - Note 10	1.3			µs
$t_{SU:STA}$	Start condition setup time		0.6			µs
$t_{HD:STA}$	Start condition hold time		0.6			µs
$t_{SU:STO}$	Stop condition setup time		0.6			µs
t_R	SCL and SDA rise time		20 + 0.1C_b		300	ns
t_F	SCL and SDA fall time		20 + 0.1C_b		300	ns
$t_{SU:DAT}$	Data in setup time		100			ns
$t_{HD:DAT}$	Data in hold time		0		0.9	µs
t_N	Noise filter SCL and SDA	Noise suppression		100		ns



APPLICATIONS INFORMATION

DEVICE OPERATION

POWER SUPPLY (PVIN, AVIN, VDD, GND)

The SMB20X can be powered from an input voltage of between 4.5-16 volts applied to the PVIN pins, AVIN and ground. An internal LDO (VDD) is used to supply 5 volts for the gate drive of the internal N-channel MOSFET. If the target application has an input supply range of 4.5-5.5 volts VDD can be connected to the input supply along with the PVIN pins and AVIN. Once the voltage applied to PVIN is above 4.0V (UVLO) and an ENx pin is taken high, the channel assigned to the ENx pin will begin switching providing the SMB20x is programmed for pin control (see "POWER-ON/OFF CONTROL" sections). Please note that the ENx pins serve dual functions both enabling/disabling channels and serving to place the SMB208x when high and placing the SMB20x in shutdown or Standby modes (see "OUTPUT STATE/SEQUENCE LOGIC TABLES" section).

POWER-ON/OFF CONTROL (EN0, EN1, I^2C Control)

The output(s) on the SMB20x can be turned on/off in a number of different ways:

The ENx pins can be pulled high (to VDD) and once power is applied, the channels will turn on according to one of the following user assigned (programmed) sequences:

1. Channels turn on according to ENx pin(s)
2. Channel 0 followed by Channel 1
3. Channel 1 followed by Channel 0
4. Channel 0 and Channel 1 Start Together

The SMB20x also employs I^2C control of the outputs, requiring only that the ENx pins be pulled high in order to facilitate this control. Using I^2C control allows all the above sequence combinations.

Finally, taking EN0 low places the part in low current shutdown mode.

SWx Pin(s)

The internal N-channel MOSFET(s)' source connection appears at the SWx nodes where the external inductor, Bootstrap capacitor and Schottky diode are all connected. The internal MOSFET gate is driven by the VDD supply working in conjunction with the Bootstrap capacitor to allow the MOSFET gate to be driven to VIN plus 5 volts. The MOSFET current is internally limited and the switching cycle is terminated when the current limit threshold is exceeded. An internal low current, low-side, N-channel MOSFET is provided for keeping the Bootstrap capacitor charged when there is no or minimal load on the output. This MOSFET is not to be used in place of the external Schottky as it will not support high currents.

Connections to the inductor, Schottky and Bootstrap capacitor must be as short as possible and the trace width maximized to the inductor and Schottky paths. Minimum trace width should be at least 0.050" (

FB

Each channel has a unique FB (Feedback) pin where the output voltage is internally connected to the inverting input of the internal transconductance amplifier. The SMB208x family requires no external resistive divider from the output to the FB node for output voltages between 0.8V to 5.0V. Further, the SMB208x family requires no external compensation components as the compensation is optimized internal to the part.

PGOOD/RESET

This open drain pin indicates that all channels assigned to this pin are functional and within the user-programmed values plus or minus the amount for under and overvoltage.

Each output can have a PGOOD/RESET associated with it or one can choose not to have this function associated with one or all channels.

The RESET pin is low when the channel is off or out of spec for voltage or an overcurrent and will go high when the channels(s) are within spec after a delay of 125mS. The PGOOD function acts as the RESET with the exception that is has no delay once all channels is within spec.

BOOTSTRAP

This pin connects to a high quality, low-ESR ceramic capacitor of 0.1uF to power the internal gate drive to VIN plus VDD (5V nominal). The BST capacitor is initially charged to 5V when the part is turned on and the output is off. When the output is turned on, the capacitor voltage is refreshed each time the internal MOSFET is turned off via the external Schottky when it is forward biased. When there is little or no load, the SMB20x refreshes the Bootstrap capacitor as required.

OVERTEMPERATURE

The SMB20x family contains an overtemperature shutdown circuit that shuts down all channels when the die temperature exceeds 140°C (nominal). Operation may resume when the internal die temperature falls to below 120°C (nominal).

APPLICATIONS INFORMATION

PROGRAMMABLE DEVICE PARAMETERS

OUTPUT VOLTAGE(S)

Output voltages for all channels are user programmable from 0.8V to 5.0V according to the below:

0.8V to 1.8V in 0.1V increments followed by;

2.3V, 2.5V, 3.0V, 3.3V, 5.0V

For any setting, a fine adjust is available whereby the user can fine tune the output voltage in steps of +1.14% of nominal up to +7.95% of nominal.

OPERATING FREQUENCY SELECTION

The SMB208x switch frequency is user programmable to operate at 500kHz or 1MHz. This setting must not be changed when the outputs are enabled. First, disable the output and then select the frequency.

SOFT START

Two soft start ramp times are available, effecting both channels. With a selection of 0.5mS or 1.0mS, choose the value that best suits the application keeping in mind that these softstart periods apply to the programmed output voltage and will cause higher turn-on slew rates when higher output voltages are programmed.

POWER-ON SEQUENCING SLOTS

Power on sequencing with multiple channels is user programmable as shown below:

1. Ch 0 > Ch 1
2. Ch 1 > Ch 0
3. Ch 0 & Ch 2 turn on are coincident
4. Disabled. This mean the channels will not turn on until the associated ENx pin is pulled high.

POWER-ON SEQUENCING DELAY(S)

Four sequence on time delays are available:

1.5mS, 12.5mS, 25mS, 50mS

These is the delay time between the first channel reaching 90% of nominal to the time the second channel begins turning on (Figure xx). This same delay time applies to turn off but the channel sequence position is reversed (Figure xx).

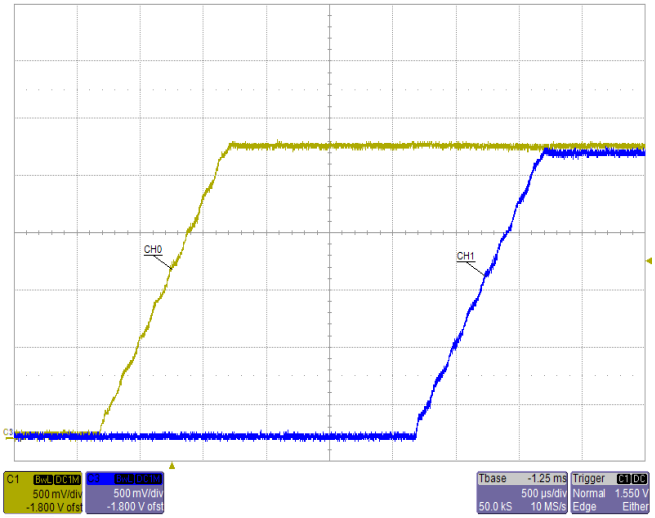


Figure 8: Ch 0 to Ch1 Sequence on with 1.5mS delay 500us/div, 500mV/div

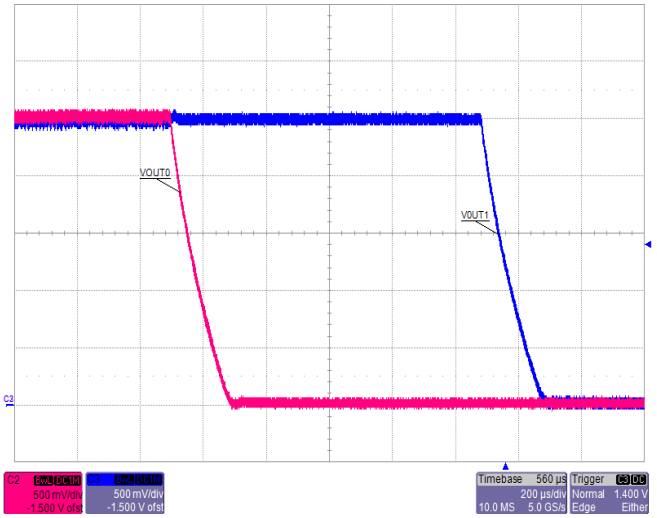


Figure 9: Ch 1 to Ch0 Sequence off with 1.5mS delay 500us/div, 500mV/div

APPLICATIONS INFORMATION

EXTERNAL COMPONENT SELECTION

OUTPUT L & C

The inductor and filter capacitor is chosen according to system requirements. These include the minimum to maximum input voltage, nominal output voltage, maximum output current and maximum allowable output ripple. For these criteria we use Equations 1-3 to determine the optimal value of L and C. The chosen output capacitor's ESR will impact the system ripple and therefore must be taken into account. For this, we use Equation 3 to determine the maximum allowable ESR.

Eq 1. $L \geq \frac{V_{OUT}(1-\sigma)}{1.4 f_{SW} I_{OUT}}$ Where σ is the duty cycle $\frac{V_{OUT}}{V_{IN}}$

Eq 2. $ESR_{COUT} \leq \frac{V_{P-P}}{I_{L(P-P)}}$

Eq 3. $C \geq \frac{I_{LP-P}}{8 f_{SW} V_{P-P}}$

A practical example involves the below system requirements:

V_{IN} = 12V

V_{OUT} = 1.8V

$I_{OUT(Max)}$ = 1.5A, use 50% of this amount to guarantee the inductor current is in CCM for most loads.

P-P Ripple (Max) = 50mV

First, solve for the minimum inductor value:

$$L \geq \frac{1.8 \cdot \left(1 - \frac{1.8}{12}\right)}{1.4 \cdot 5 \cdot 10^5 \cdot 10.75} \geq 2.9 \cdot 10^{-6} : \text{Use } 3.3\text{uH}$$

Now find the inductor ripple current:

$$I_{LP-P} = \frac{V_{OUT}(1-\sigma)}{L \cdot f_{SW}} = \frac{1.8 \cdot 0.85}{3.3 \cdot 10^5 \cdot 5 \cdot 10^5} = 0.093A$$

Next solve for the maximum allowable ESR for the output capacitor followed by the minimum capacitor value required to meet the output ripple spec with given the ripple current flowing through the inductor.

$$ESR_{COUT} \leq \frac{0.05}{2.1} \leq 24m\Omega$$

$$C \geq \frac{0.093}{8 \cdot 5 \cdot 10^5 \cdot 0.05} \geq 4.65 \cdot 10^{-7}$$

The calculated value of capacitance is much less than the minimum recommended for stable loop operation of the SMB20x (22uF), so choose 2 - 22uF capacitors with each having a maximum ESR at 500kHz of 48milliohms (0.048/2 = 0.024) or less.

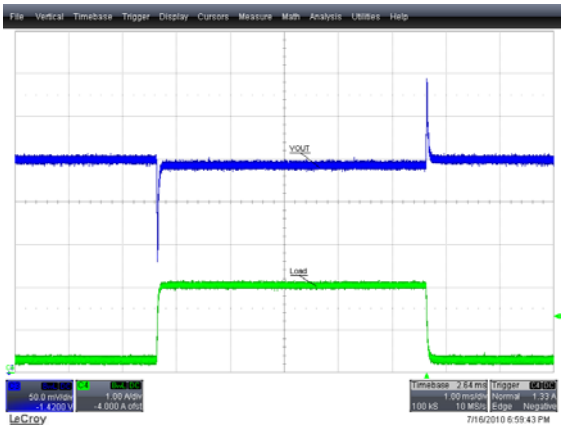


Figure 10: Transient load response: 5VIN, 1.5VOUT 0.2A-2A current Step

50mV/div, 1A/div, 1ms/div

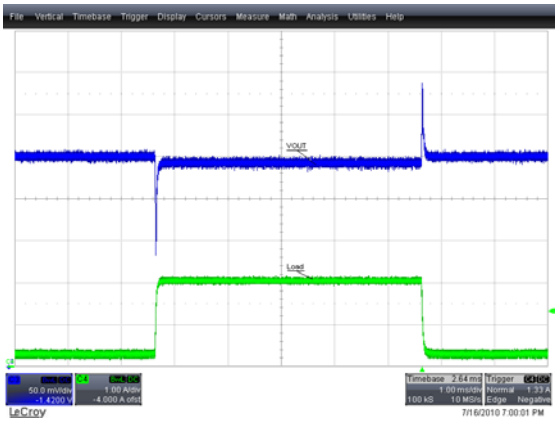


Figure 11: Transient load response: 5VIN, 1.5VOUT 0.2A-2A current Step

50mV/div, 1A/div, 1ms/div

APPLICATIONS INFORMATION

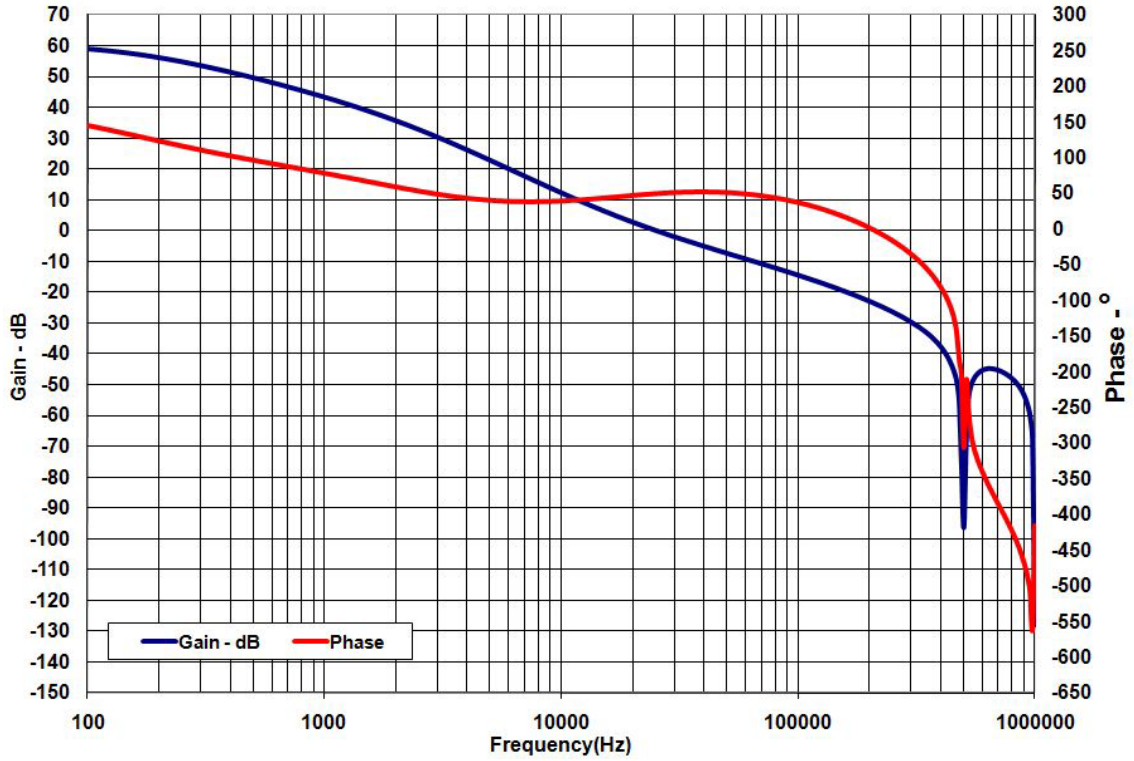


Figure 12: Bode plot of SMB208 circuit displayed in Figure 17 with full load

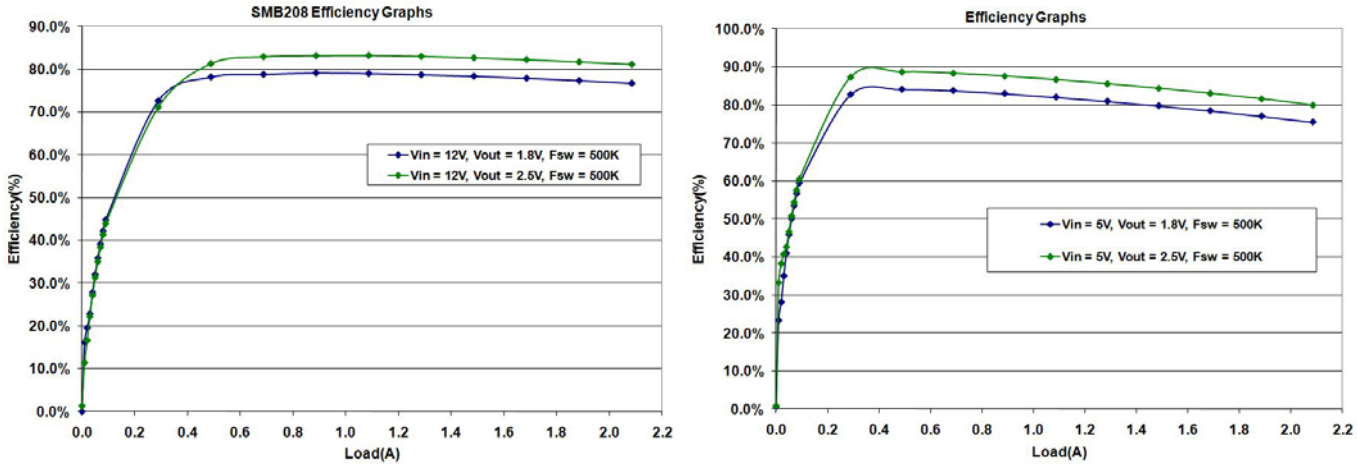


Figure 13 & 14: SMB208 Efficiency with 12V and 5V inputs

APPLICATIONS INFORMATION

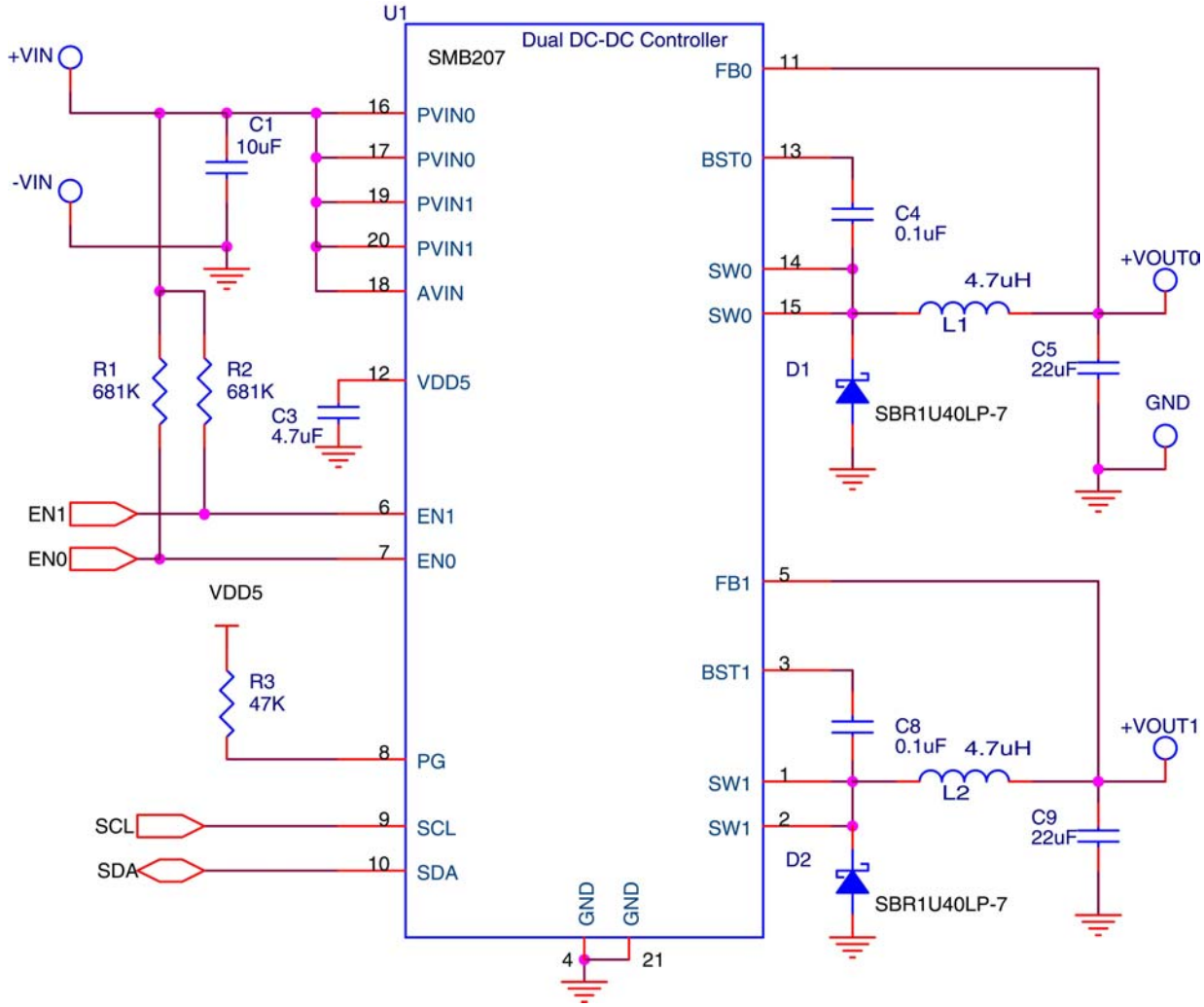
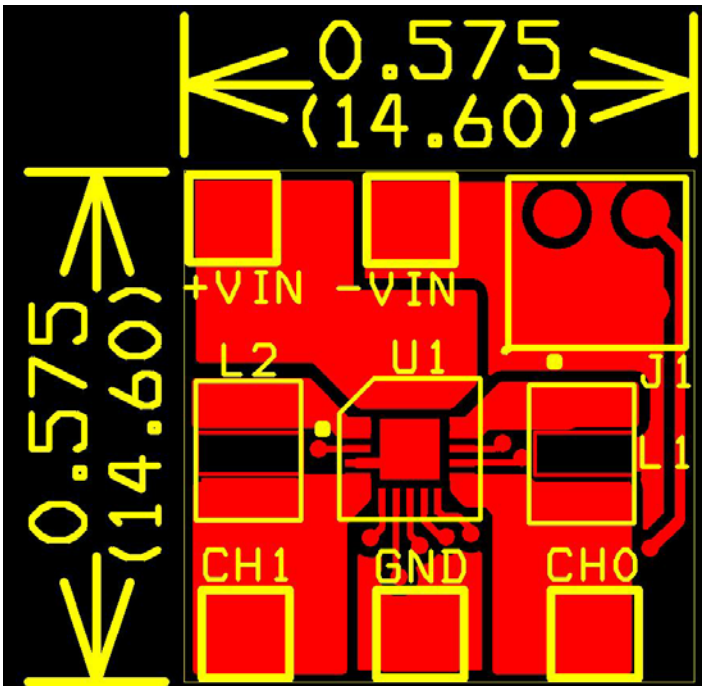


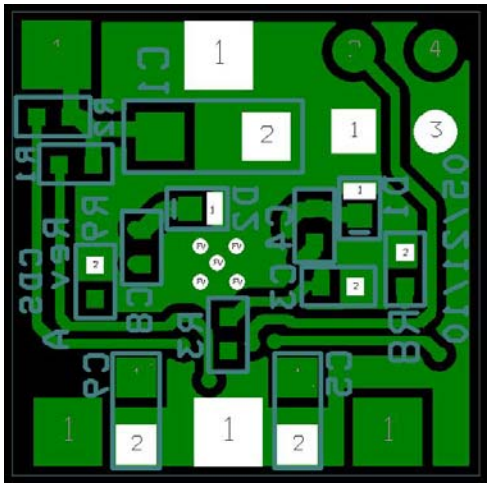
Figure 15: SMB207 Detailedl Schematic

SMB207 Bill of Materials

Item#	Quantity	Description	Ref Des	Manufacturer	Manufacturer P/N
1	1	10UF 25V CERAMIC X5R 1206	C1	Panasonic	ECJ-3YB1E106K
2	1	CAP CER 4.7UF 6.3V X5R 0402	C3	Panasonic	ECJ-0EB0J475M
3	2	0.1uF 16V 10% X7R 0402	C4, C8	EPCOS Inc	B37921C9104K60
4	2	CAP CER 22UF 10V X5R 0805	C5, C9	Panasonic	ECJ-2FB1A226M
5	2	Schottky diode, 3 pin, common anode	D1, D2	Diode Inc	SBR1U40LP-7
6	2	4.7uH Inductor 1.3A 20% 1210 SMD	L1, L2	Taiyo Yuden	BRL3225T4R7M
7	2	RES 681K OHM 1/16W 1% 0402	R1, R2	Any	
8	1	RES 47K OHM 1/16W 5% 0402	R3	Any	
9	1	DC-DC Controller	U1	Summit Micro	SMB207

APPLICATIONS INFORMATION





Top Layer

Bottom Layer

Figure 17: Typical SMB207 layout displaying placement of critical components and trace routing

APPLICATIONS INFORMATION

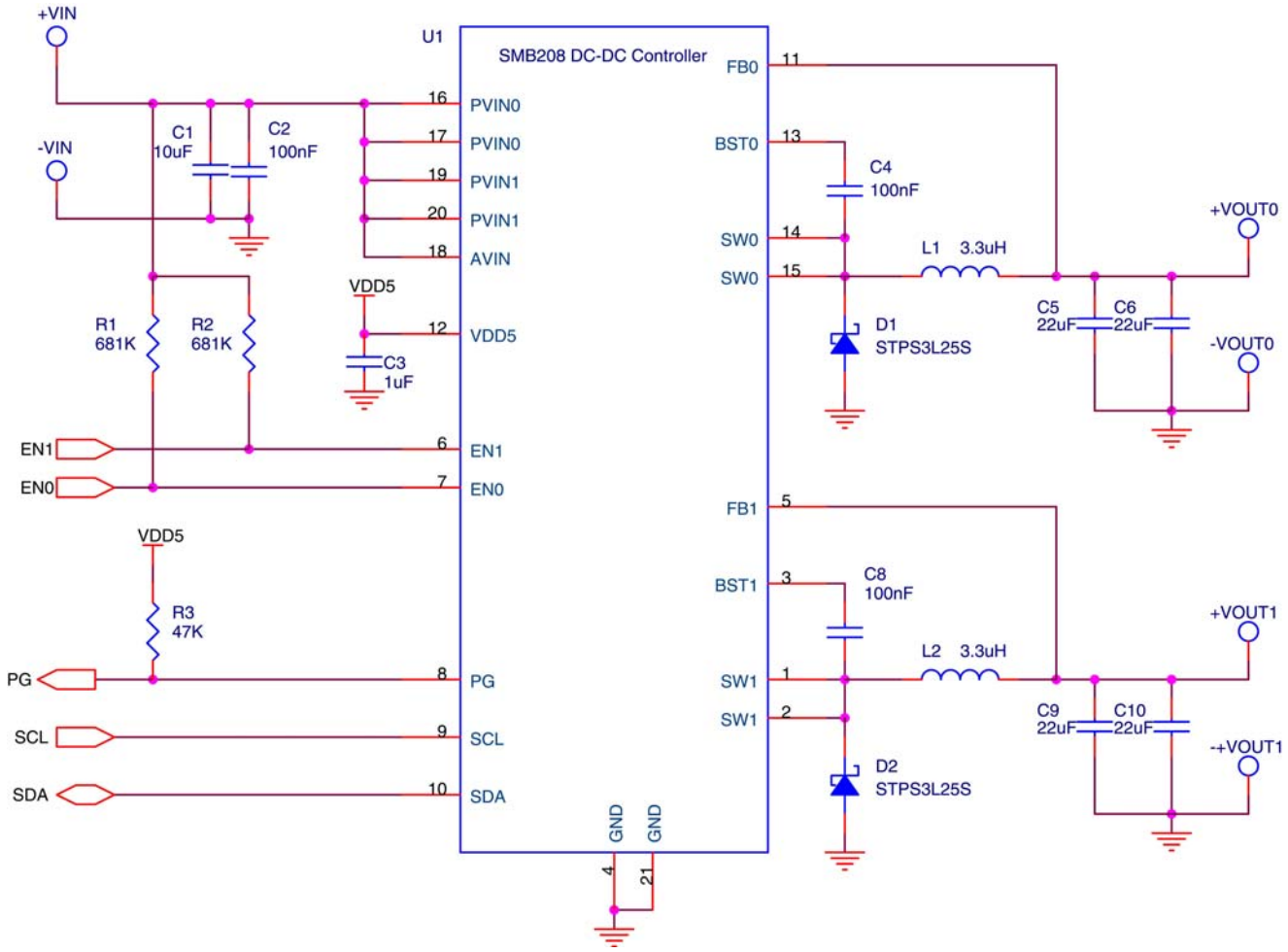
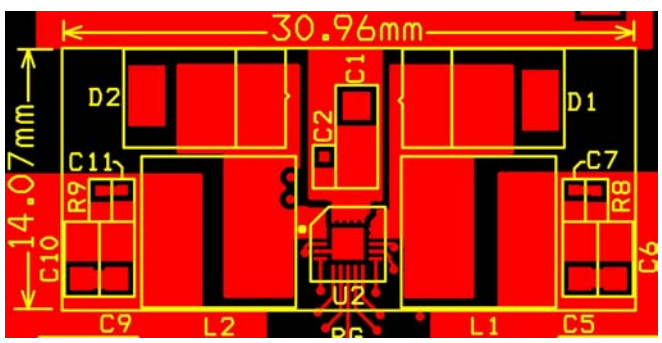


Figure 17: SMB208 Detailed Schematic

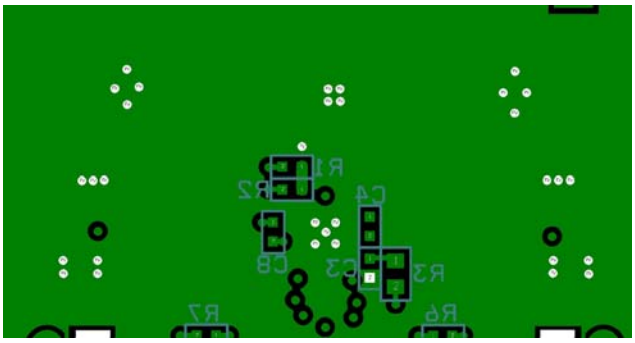
SMB208 Bill of Materials

Item Number	Qty	Description	Ref Des	Manufacturer	Manufacturer P/N
1	1	10UF 25V CERAMIC X5R 1206	C1	Panasonic	ECJ-3YB1E106K
2	1	CAP CER 4.7UF 6.3V X5R 0402	C3	Panasonic	ECJ-0EB0J475M
3	2	0.1uF 16V 10% X7R 0402	C4 C8	EPCOS Inc	B37921C9104K60
4	2	CAP CER 22UF 10V X5R 0805	C5 C9	Panasonic	ECJ-2FB1A226M
5	2	Schottky diode, 3 pin, common anode	D1, D2	Diode Inc	SBR1U40LP-7
6	2	4.7uH Inductor 1.3A 20% 1210	L1, L2	Taiyo Yuden	BRL3225T4R7M
7	2	RES 681K OHM 1/16W 1% 0402	R1, R2	Any	
8	1	RES 47K OHM 1/16W 5% 0402	R3	Any	
11	1	DC-DC Controller	U1	Summit Micro	SMB208

APPLICATIONS INFORMATION

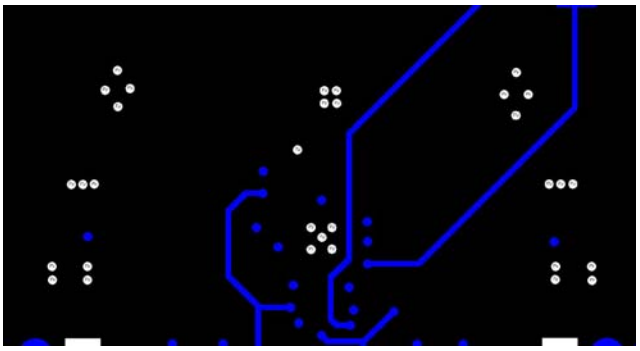


Top Layer



Bottom Layer

Inner Layer 1



Inner Layer 2

Figure 18: SMB208 typical bottom layer layout displaying placement of critical components and trace routing

APPLICATIONS INFORMATION

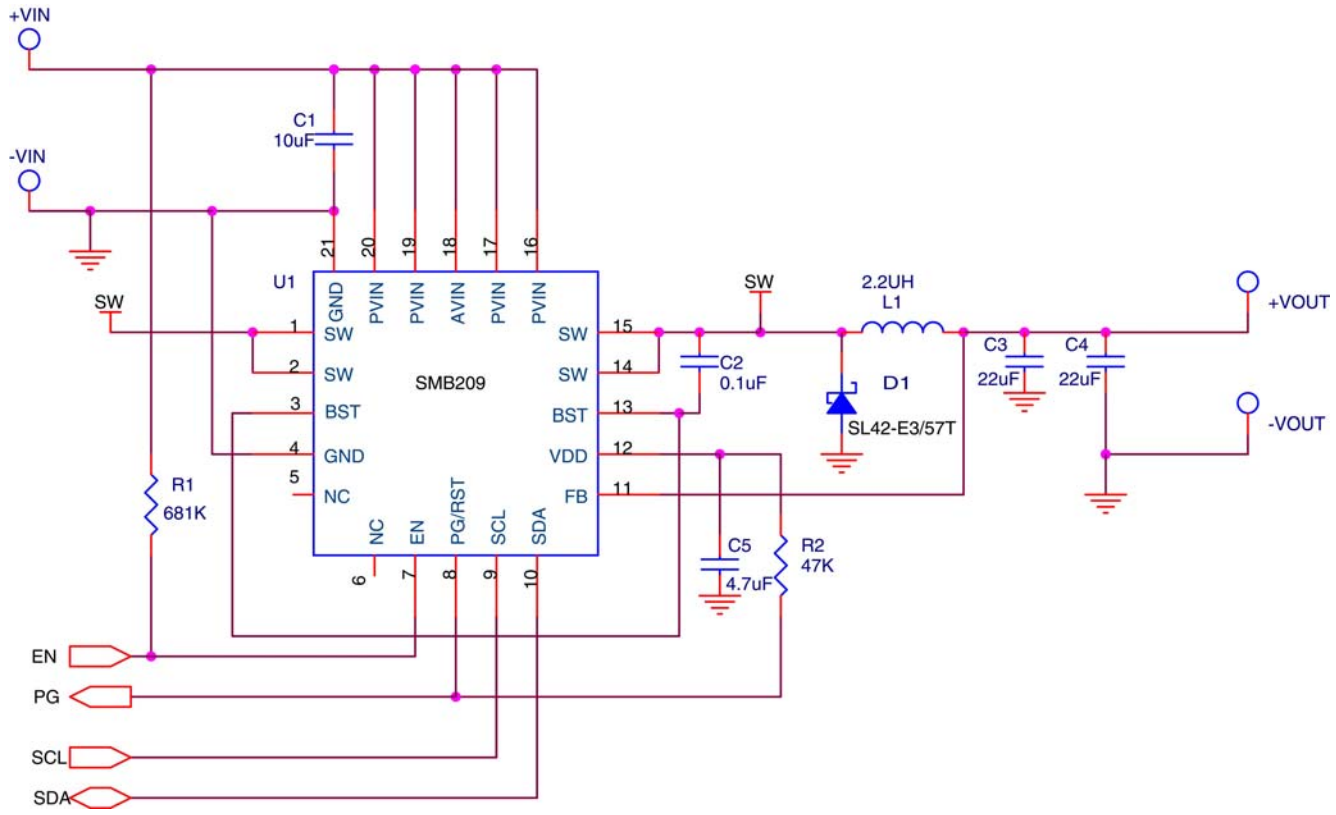
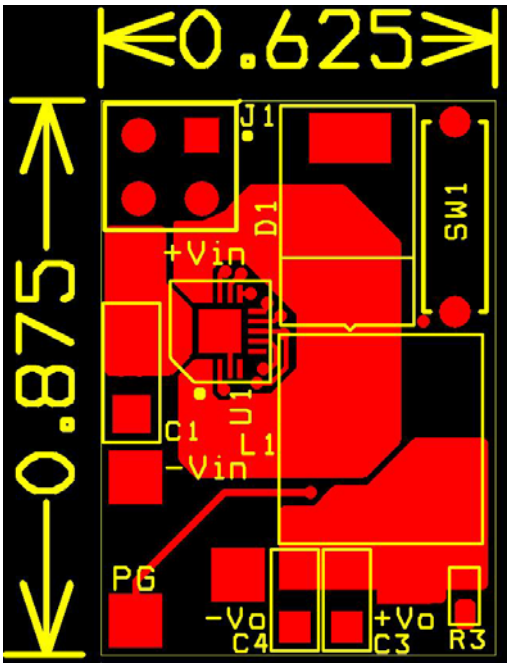


Figure 19: SMB209 Detailed Schematic

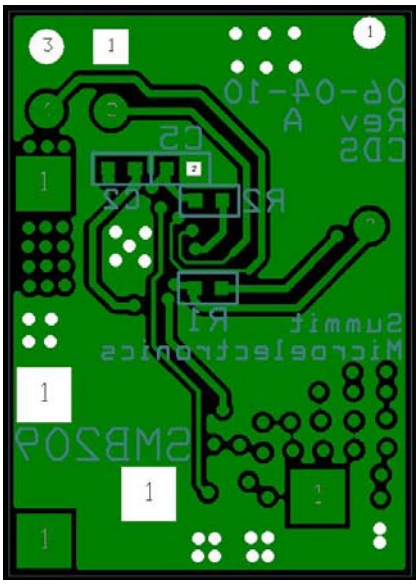
SMB209 Bill of Materials

Item Number	Qty	Description	Ref Des	Manufacturer	Manufacturer P/N
1	1	10UF 25V CERAMIC X5R 1206	C1	Panasonic	ECJ-3YB1E106K
2	1	0.1uF 16V X7R 0402	C2	Murata	GCM155R71C104KA55D
3	2	CAP CER 22UF 6.3V 20% X5R 0805	C3, C4	Murata	GRM21BR60J226ME39L
4	1	CAP CER 4.7UF 6.3V X5R 0402	C5	Panasonic	ECJ-0EB0J475M
5	1	DIODE SCHOTTKY 40V 1A SMA	D1	Vishay	SL42-E3/57T
6	1	2.2UH 4.02A SMD INDUCTOR POWER	L1	Wurth Electronics	7447789002
7	1	RES 681K OHM 1/16W 1% 0402 SMD	R1	Any	
8	1	RES 10K OHM 1/16W 5% 0402 SMD	R2	Any	
10	1	DC-DC Controller	U1	Summit Micro	SMB209

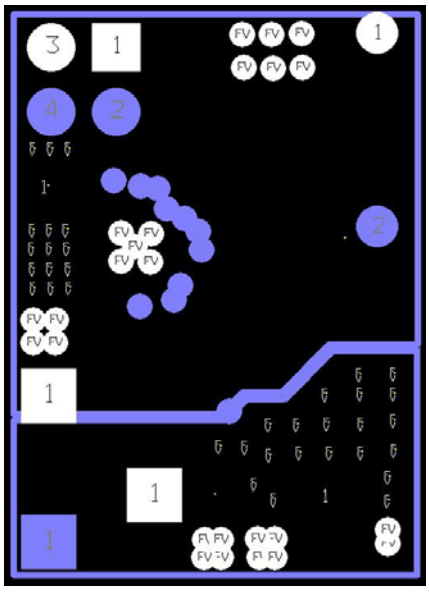
APPLICATIONS INFORMATION



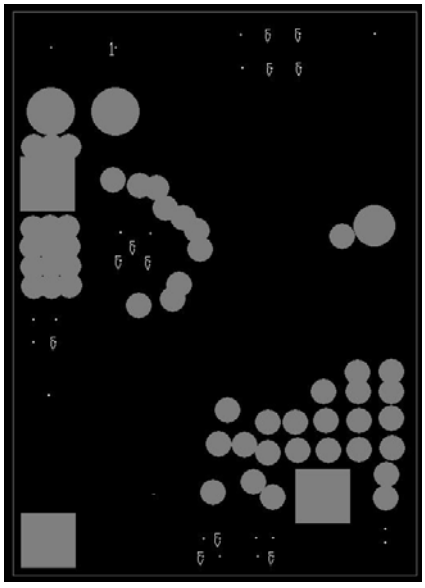
Top Layer



Bottom



Top Layer



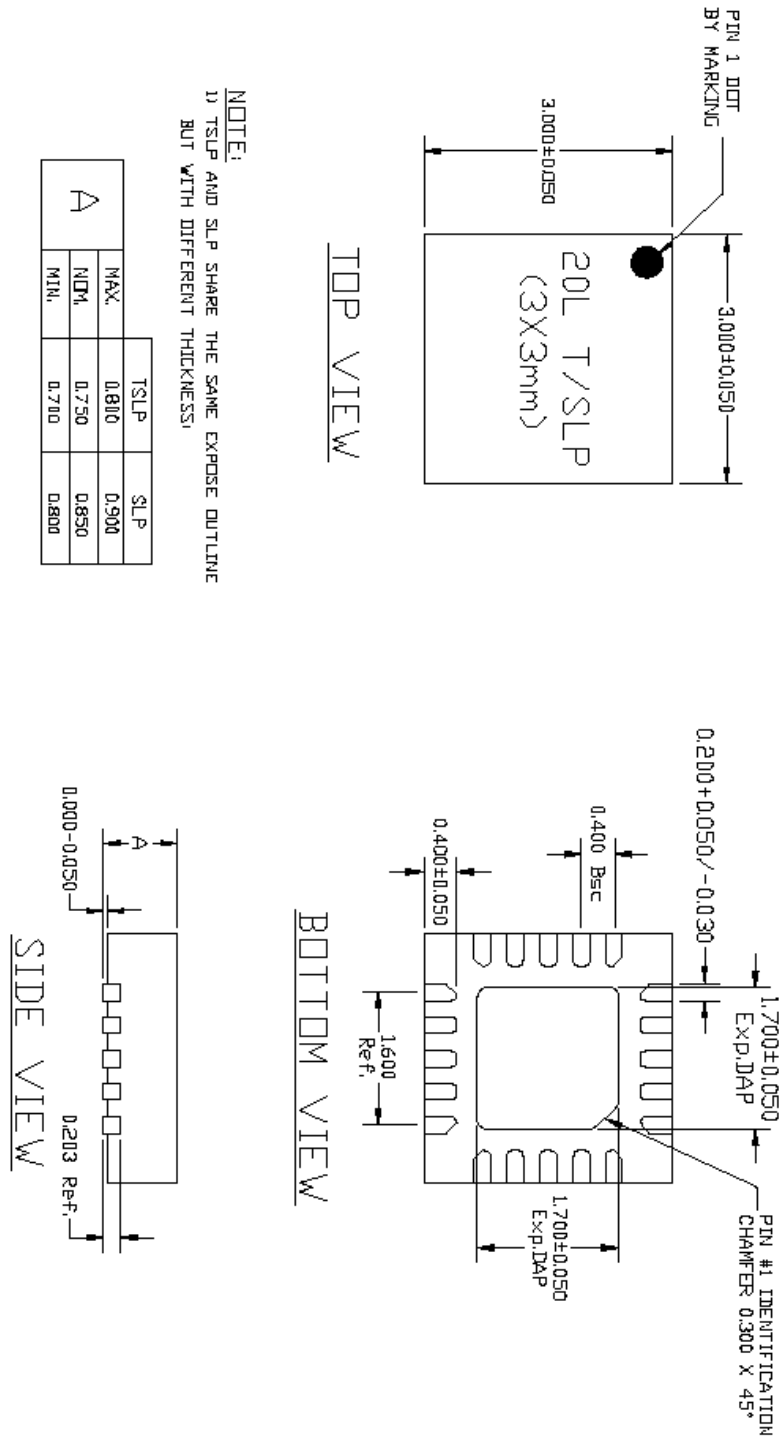
Bottom Layer

Figure 20: SMB209 typical inner ground layer layout displaying placement of critical components and trace routing

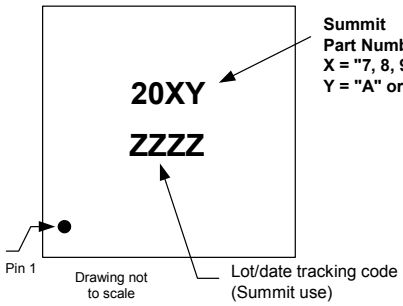
DEVELOPMENT HARDWARE & SOFTWARE

The Windows GUI software will generate the data and send it in I^2C serial bus format so that it can be directly downloaded to the SMB20X/20XA via the programming Dongle and cable. An example of the connection interface is shown in Figure 6. When design prototyping is complete, the software can generate a HEX data file that should be transmitted to Summit for approval. Summit will then assign a unique customer ID to the HEX code and program production devices before the final electrical test operations. This will ensure proper device operation in the end application.

PACKAGE DIMENSIONS (QFN)



PART MARKING



ORDERING INFORMATION

SMB20XY N T nnnn L

Summit Part Number
X = "7,8,9"
Y = Blank or "A"

Package
N= 20 Pad QFN

Tape & Reel

Part Number Suffix
Specific requirements are contained in the suffix

Environmental Attribute
L = 100% Sn Free, RoHS Compliant

NOTICE

NOTE 1 - This is an ***Preliminary Information*** data sheet that describes a Summit product currently in development. It is meant solely as a product description and should not be used as a design tool.

SUMMIT Microelectronics, Inc. reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. SUMMIT Microelectronics, Inc. assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained herein reflect representative operating parameters, and may vary depending upon a user's specific application. While the information in this publication has been carefully checked, SUMMIT Microelectronics, Inc. shall not be liable for any damages arising as a result of any error or omission.

SUMMIT Microelectronics, Inc. does not recommend the use of any of its products in life support or aviation applications where the failure or malfunction of the product can reasonably be expected to cause any failure of either system or to significantly affect their safety or effectiveness. Products are not authorized for use in such applications unless SUMMIT Microelectronics, Inc. receives written assurances, to its satisfaction, that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; and (c) potential liability of SUMMIT Microelectronics, Inc. is adequately protected under the circumstances.

Revision 2.0 - This document supersedes all previous versions. Please check the Summit Microelectronics Inc. web site at www.summitmicro.com for data sheet updates.