ES25M40A, ES25M80A, ES25M16A

4M-BIT, 8M-BIT AND 16M-BIT

Serial Flash Memory with 4KB Sectors and Dual Output SPI

Excel Semiconductor inc.

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1. GENERAL DESCRIPTION

The ES25M40A (4M-bit), ES25M80A (8M-bit) and ES25M16A (16M-bit) and Serial Flash memories provide a storage solution for systems with limited space, pins and power. The 25M series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual SPI and storing voice, text and data. The devices operate on a single 2.7V to 3.6V power supply with current consumption as low as 5mA active and 1μA for power-down. All devices are offered in space-saving packages.

The ES25M40A/80A/16A array is organized into 2,048/4,096/8,192 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time using the Page Program instructions. Pages can be erased in groups of 16 (sector erase), groups of 256 (block erase) or the entire chip (chip erase). The ES25M40A/80A/16A has 128/256/512 erasable sectors and 8/16/32 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See figure 2.)

The ES25M40A/80A/16A supports the standard Serial peripheral Interface (SPI), and a high performance Dual output as well as Dual I/O SPI using pins: Serial Clock, Chip Select, Serial Data I/O0(DI), Serial Data I/O1(DO). SPI clock frequencies of up to 80MHz are supported allowing equivalent clock rates of 160MHz for Dual Output. These transfer rates are comparable to those of 8 and 16-bit Parallel Flash memories.

A Hold pin, Write Protect pin and programmable write protection, with top or bottom array control, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device identification with a 64-bit Unique Serial Number.

2. FEATURES

- **Family of Serial Flash Memories**
  - ES25M40A: 4M-bit / 0.5M–byte (524,288)
  - ES25M80A: 8M-bit / 1M–byte (1,048,576)
  - ES25M16A: 16M-bit / 2M –byte (2,097,152)
  - 256-bytes per programmable page
- **SPI Serial Interface with Single or Dual Outputs**
  - Clock, Chip Select, Data I/O0, Data I/O1
  - Optional Hold function for SPI flexibility
- **Fast Data Transfer up to 160M-bits / Second**
  - Clock operation to 80MHz
  - Fast Read Dual Output instruction
- **Flexible Architecture with 4KB sectors**
  - Uniform Sector Erase (4K-bytes)
  - Block Erase (64K-bytes)
  - Page program up to 256 bytes < 2ms
  - Up to 100,000 erase/write cycles
  - 20-year data retention
- **Low Power, wide Temperature Range**
  - Single 2.7 to 3.6V supply
  - 4mA active current, <1μA Power-down (typ.)
  - -40℃ to +85℃ operating range
- **Advanced Security Features**
  - Software and Hardware Write-protect
  - Top or Bottom, Sector or Block selection
  - 64-Bit Unique ID for each device
- **Space Efficient Packaging**
  - 8-pin SOIC 150-mil
  - 8-pin SOIC 208mil
  - 8-pin WSON 6x5-mm
  - 16-pin SOIC 300-mil

3. PIN CONFIGURATION 8-Pin SOIC 150-MIL

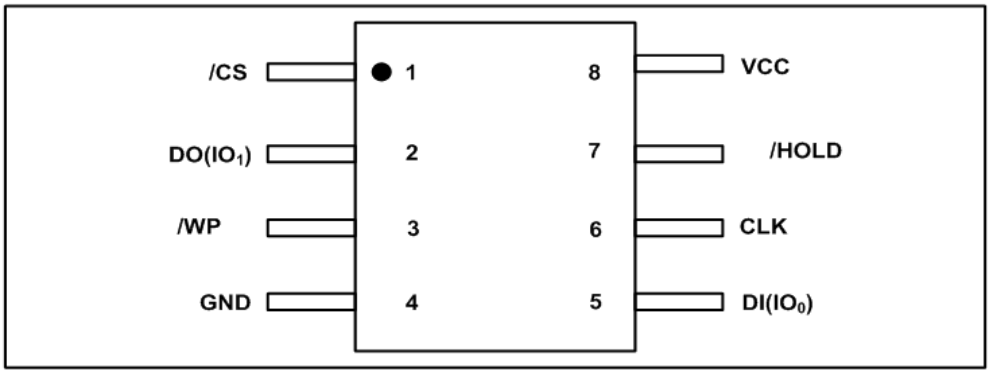


Figure 1a. ES25M40A and ES25M80A Assignments, 8-pin SOIC 150-mil

4. PIN CONFIGURATION 8-Pin SOIC 208-MIL

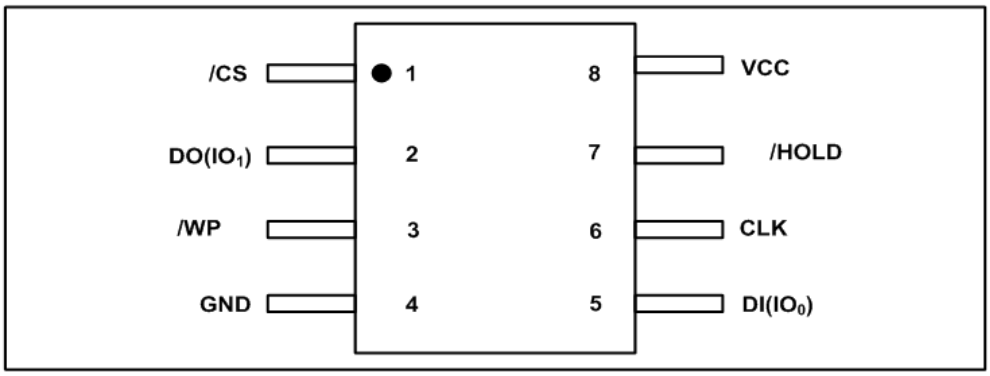


Figure 1b. ES25M40A, ES25M80A and ES25M16A Assignments, 8-pin SOIC 208-mil

5. PIN CONFIGURATION WSON 6X5-MM

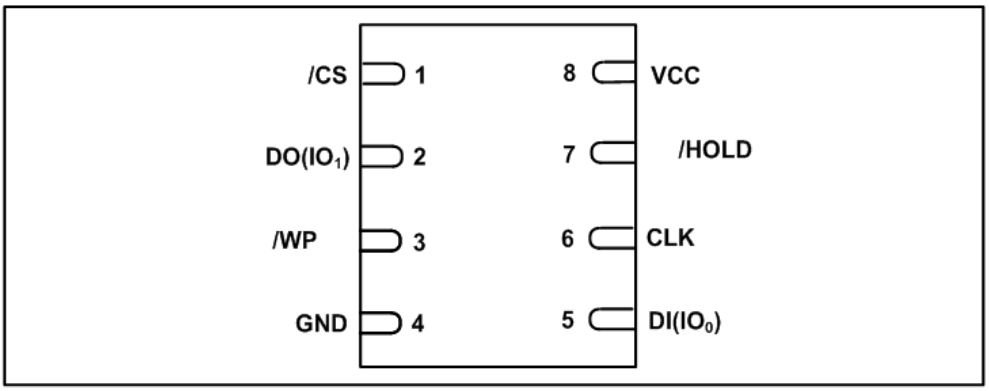


Figure 1c. 8-Contact WSON

6. PIN DESCRIPTION SOIC 150-MIL, SOIC 208-MIL AND WSON 6X5-MM

PIN NO.	PIN NAME	FUCTION
1	/CS	Chip Select Input
2	DO (IO1)	Data Output (Data Input Output1)*
3	/WP	Write Protect Input
4	GND	Ground
5	DI (IO0)	Data Input (Data Input Output0)*
6	CLK	Serial Clock Input
7	/HOLD	Hold Input
8	VCC	Power Supply

* IO0 and IO1 are used for Dual instruction.

7. PIN DESCRIPTION

7.1 Package Types

ES25M40A is offered in an 8-pin plastic 150-mil, 208-mil and 6x5-mm WSON as shown in figure 1a, 1b and 1c respectively. ES25M80A and ES25M16A are offered in an 8-pin plastic 208-mil width SOIC and 6x5-mm WSON as shown in figure 1b and 1c respectively. Package diagrams and dimensions are illustrated at the end of this datasheet.

7.2 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output is at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up (see “Write Protection” and figure 21). If needed a pull-up resister on /CS and be used to accomplish this.

7.3 Serial Data Input (DI)

The SPI Serial Data Input (DI) pin provides a means for instructions, addresses and data to be serially written to (shifted into) the device. Data is latched on the rising edge of the Serial Clock(CLK) input pin. The DI pin is also used as an output when the Fast Read Dual Output and the Fast Read Dual I/O instructions are executed.

7.4 Serial Data Output (DO)

The SPI Serial Data Output(DO) pin provides a means for data and status to be serially read from(shifted out of) the device. Data is shifted out on the falling edge of the Serial Clock(CLK) input pin. The DO pin is also used as an input when the Fast Read Dual I/O instruction is executed.

7.5 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect (SEC. TB. BP2, Bp1 and BP0) bits and Status Register Protect (SRP) bits, a portion or the entire memory array can be hardware protected. The /WP pin is active low.

7.6 HOLD (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low.

7.7 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. (“See SPI Operations”)

8. BLOCK DIAGRAM

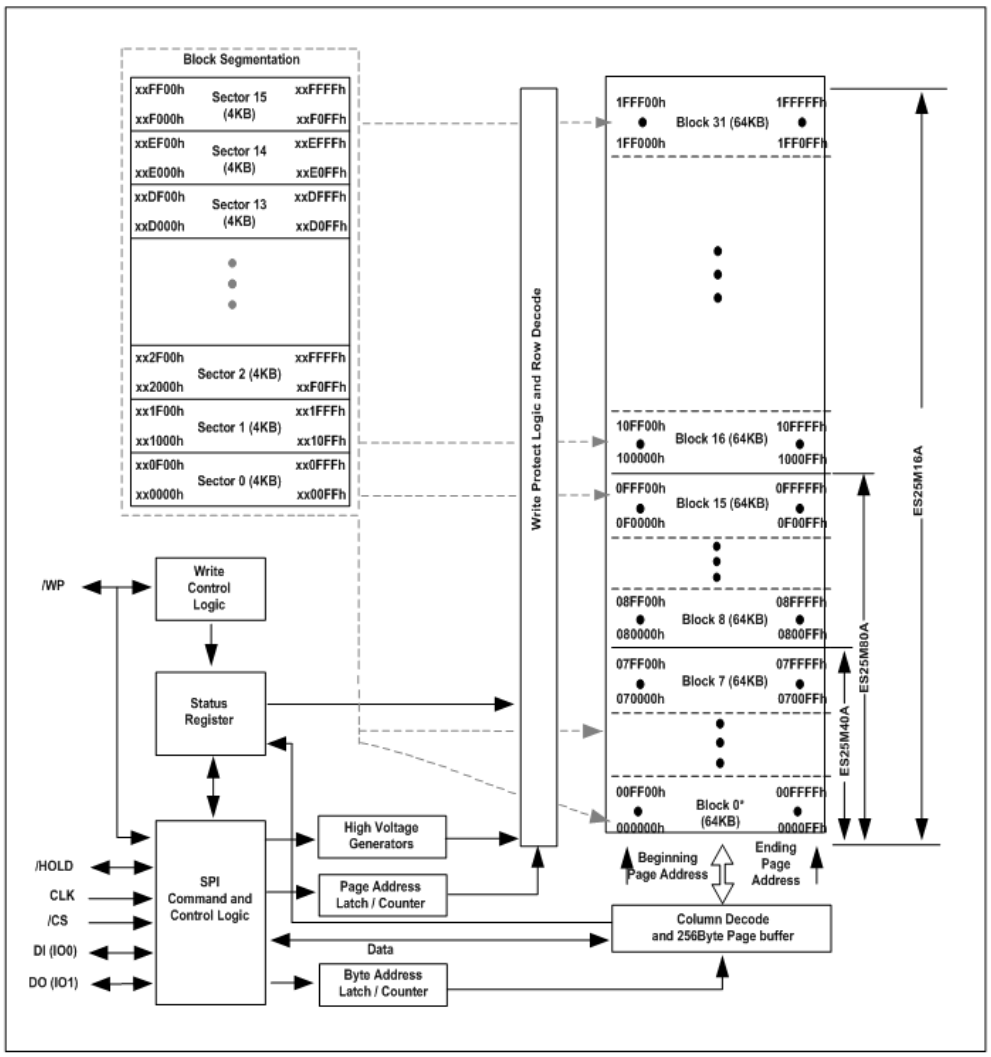


Figure 2. ES25M40A, ES25M80A, ES25M16A Block Diagram

9. FUNCTIONAL DESCRIPTION

9.1 SPI OPERATIONS

9.1.1 Standard SPI Instructions

The ES25M40A/80A/16A is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK). Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge CLK.

SPI bus operation Modes 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3 the CLK signal is normally high on the falling and rising edges of /CS.

9.1.2 Dual SPI Instructions

The ES25M40A/80A/16A supports Dual SPI operation when using the “Fast Read Dual Output and Dual I/O” (3B and BB hex) instructions. These instructions allow data to be transferred to or from the device at two to three the rate ordinary Serial Flash devices. The Dual Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions the DI and DO pins become bidirectional I/0 pins; IO0 and IO1

9.1.3 Hold Function

The /HOLD signal allows the ES25M40A/80A/16A operation to be paused while it is actively selected (When /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again.
To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will terminate after the next falling edge of CLK. During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active (low) for the full duration on the /HOLD operation to avoid resetting the internal logic state of the device.

9.2 WRITE PROTECTION

Applications that use non-volatile memory must take consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern the ES25M40A/80A/16A provides several means to protect data from inadvertent writes.

9.2.1 Write protect Features

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after program and erase
- Software and Hardware (/WP pin) write protection using Status Register
- Write Protection using Power-down instructions

Upon power-up at power down the ES25M40A/80A/16A will maintain a reset condition while VCC is below the threshold value of Vwl, (See Power-up Timing and Voltage Levels and Figure 21). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds Vwl, all program and erase related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached. If needed, a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page program, Sector Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the write Enable (WEL) is automatically cleared to write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register protect (SRP) and Block protect (SEC, TB, BP2, BP1, and BP0) bits. These setting allow a portion or all of the memory to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for Release Power-down instruction.

10. CONTROL AND STATUS REGISTER

The Read Status Register instructions can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled, the state of write protection. The Write Status Register instruction can be used to configure the devices write protection features. Write access to the Status Register is controlled by in some cases the /WP pin.

10.1 STATUS REGISTER

10.1.1 BUSY

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Sector Erase, Block Erase, Chip Erase or Write Register instruction. During this time the device will ignore further instructions except for the Read Status Register (see tW, tPP, tSE, tBE, and tCE in AC Characteristics). When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

10.1.2 Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to a 1 after executing a Write Enable instruction. The WEL status bit is cleared to a 0 when device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register.

10.1.3 Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block protect bits can be set using the Write Status Register Instruction (see tw in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

10.1.4 Top/Bottom Block protect (TB)

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction provided that the Write Enable instruction has been issued. The TB bit can not be written to if the Status Register Protect (SRP) bit is set to 1 and the Write Protect (WP) pin is low.

10.1.5 Sector/Block Protect (SEC)

The non-volatile Sector protect bit (SEC) controls if the Block Protect Bits (BP2, BP1, BP0) protect 4KB Sectors (SEC=1) or 64KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory protection table. The default setting is SEC=0.

10.1.6 Status Register Protect (SRP)

The Status Register Protect (SRP) bit is a non-volatile read/write bit in the status register (S7) that can be used in conjunction with the Write Protect (/WP) pin to disable writes to status register. When the SRP bit is set to a 0 state (factory default), the /WP pin has no control over status register. When the SRP pin is set to a 1, the Write Status Register instruction is locked out while the /WP pin is low. When the /WP pin is high the Write Status Register instruction is allowed.

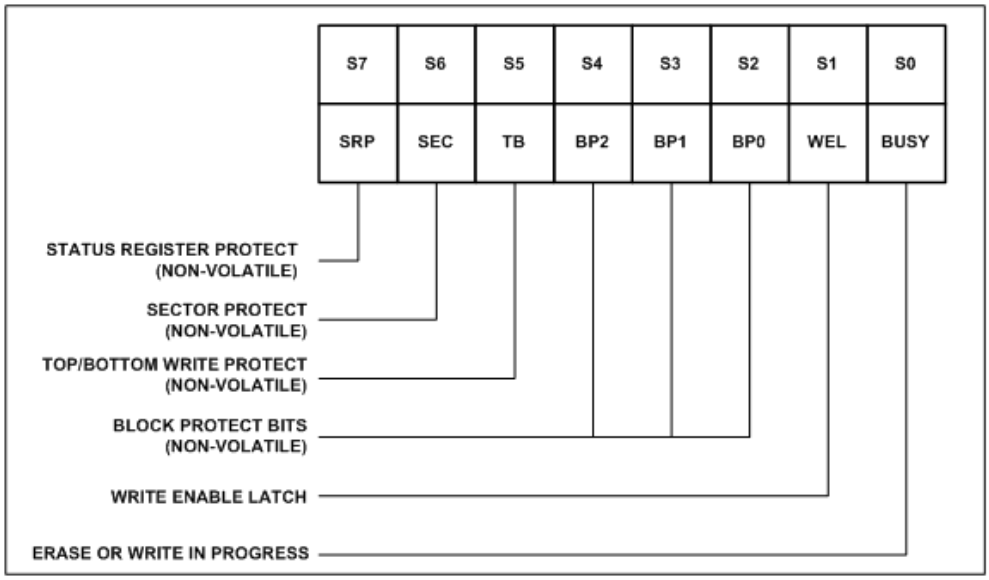


Figure 3. Status Register Bit Locations

10.1.7 Status Register Memory Protection

STATUS REGISTER(1)					ES25M40A (4M-BIT) MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	7	070000h-07FFFFh	64KB	Upper 1/8
0	0	0	1	0	6 and 7	060000h-07FFFFh	128KB	Upper 1/4
0	0	0	1	1	4 thru 7	040000h-07FFFFh	256KB	Upper 1/2
0	1	0	0	1	0	000000h-00FFFFh	64KB	Lower 1/8
0	1	0	1	0	0 and 1	000000h-01FFFFh	128KB	Lower 1/4
0	1	0	1	1	0 thru 3	000000h-03FFFFh	256KB	Lower 1/2
X	X	1	X	X	0 thru 7	000000h-3FFFFFh	512KB	ALL
1	0	0	0	1	7	07F000h-07FFFFh	4KB	Top Block
1	0	0	1	0	7	07E000h-07FFFFh	8KB	Top Block
1	0	0	1	1	7	07C000h-07FFFFh	16KB	Top Block
1	0	1	X	X	7	078000h-07FFFFh	32KB	Top Block
1	1	0	0	1	0	000000h-000FFFh	4KB	Bottom Block
1	1	0	1	0	0	000000h-001FFFh	8KB	Bottom Block
1	1	0	1	1	0	000000h-003FFFh	16KB	Bottom Block
1	1	1	X	X	0	000000h-007FFFh	32KB	Bottom Block

STATUS REGISTER(1)					ES25M80A(8M-BIT) MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PROTION
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	15	0F0000h-0FFFFFh	64KB	Upper 1/16
0	0	0	1	0	14 and 15	0E0000h-0FFFFFh	128KB	Upper 1/8
0	0	0	1	1	12 thru 15	0C0000h-0FFFFFh	256KB	Upper 1/4
0	0	1	0	0	8 thru 15	080000h-0FFFFFh	512KB	Upper 1/2
0	1	0	0	1	0	000000h-00FFFFh	64KB	Lower 1/16
0	1	0	1	0	0 and 1	000000h-01FFFFh	128KB	Lower 1/8
0	1	0	1	1	0 thru 3	000000h-03FFFFh	256KB	Lower 1/8
0	1	1	0	0	0 thru 7	000000h-07FFFFh	512KB	Lower 1/2
X	X	1	0	1	0 thru 15	000000h-0FFFFFh	1MB	ALL
X	X	1	1	X	0 thru 15	000000h-0FFFFFh	1MB	ALL
1	0	0	0	1	15	0FF000h-0FFFFFh	4KB	Top Block
1	0	0	1	0	15	0FE000h-0FFFFFh	8KB	Top Block
1	0	0	1	1	15	0FC000h-0FFFFFh	16KB	Top Block
1	0	1	X	X	15	0F8000h-0FFFFFh	32KB	Top Block
1	1	0	0	1	0	000000h-000FFFh	4KB	Bottom Block
1	1	0	1	0	0	000000h-001FFFh	8KB	Bottom Block
1	1	0	1	1	0	000000h-003FFFh	16KB	Bottom Block
1	1	1	X	X	0	000000h-007FFFh	32KB	Bottom Block

STATUS REGISTER[1]					ES25M16A (16M-BIT) MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PROTION
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	31	1F0000h-1FFFFFh	64KB	Upper 1/32
0	0	0	1	0	30 and 31	1E0000h-1FFFFFh	128KB	Upper 1/16
0	0	0	1	1	28 thru 31	1C0000h-1FFFFFh	256KB	Upper 1/18
0	0	1	0	0	24 thru 31	180000h-1FFFFFh	512KB	Upper 1/4
0	0	1	0	1	16 thru 31	100000h-1FFFFFh	1MB	Upper 1/2
0	1	0	0	1	0	000000h-00FFFFh	64KB	Upper 1/32
0	1	0	1	0	0 and 1	000000h-01FFFFh	128KB	Lower 1/16
0	1	0	1	1	0 thru 3	000000h-03FFFFh	256KB	Lower 1/8
0	1	1	0	0	0 thru 7	000000h-07FFFFh	512KB	Lower 1/4
0	1	1	0	1	0 thru 15	000000h-0FFFFFh	1MB	Lower 1/2
X	X	1	1	X	0 thru 31	000000h-1FFFFFh	2MB	ALL
1	0	0	0	1	31	1FF000h-1FFFFFh	4KB	Top Block
1	0	0	1	0	31	1FE000h-1FFFFFh	8KB	Top Block
1	0	0	1	1	31	1FC000h-1FFFFFh	16KB	Top Block
1	0	1	X	X	31	1F8000h-1FFFFFh	32KB	Top Block
1	1	0	0	1	0	000000h-000FFFh	4KB	Bottom Block
1	1	0	1	0	0	000000h-001FFFh	8KB	Bottom Block
1	1	0	1	1	0	000000h-003FFFh	16KB	Bottom Block
1	1	1	X	X	0	000000h-007FFFh	32KB	Bottom Block

Note :
1. x = don't care

10.2 INSTRUCTIONS

The instruction set of the ES25M40A/80A/16A consists of sixteen basic instructions that are fully controlled through the SPI bus (see Instruction Set table). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in figures 4 through 20. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bit have been clocked) otherwise the instruction will be terminated. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

10.2.1 Manufacturer and Device Identification

MANUFACTRER ID	**(M7-M0)**	
Excel Semiconductor	4Ah	
Device ID	**(ID7-ID0)**	**(ID15-ID0)**
Instruction	**ABh, 90h**	**9Fh**
ES25M40A	12h	3213h
ES25M80A	13h	3214h
ES25M16A	14h	3215h

10.2.2 Instruction Set Table[1]

INSTRUCTION NAME	BYTE 1 (CODE)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Write Enable	**06h**					
Write Disable	**04h**					
Read Status Register	**05h**	(S7-S0)[2]				
Write Status Register	**01h**	(S7-S0)				
Read Data	**03h**	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next Byte)
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Fast Read Dual Output	**3Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0,…)*
Fast Read Dual I/O	**BBh**	A23-A8**	A7-A0, M7-M0**	(D7-D0,…)*		
Page Program	**02h**	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next Byte)
Block Erase (64KB)	**D8h**	A23-A16	A15-A8	A7-A0		
Sector Erase (4KB)	**20h**	A23-A16	A15-A8	A7-A0		
Chip Erase	**C7h/60h**					
Power-down	**B9h**					
Release power down and Device ID	**ABh**	dummy	dummy	dummy	(ID7-ID0)[3]	(ID7-ID0)
Manufacturer/ Device ID[4]	**90h**	dummy	dummy	00h	(M7-M0)	(ID7-ID0)
Read Unique ID	**4Bh**	dummy	dummy	dummy	dummy	(ID63-ID0)
JEDEC ID	**9Fh**	(M7-M0) Manufacturer	(ID15-ID8) Memory Type	(ID7-ID0) Capacity		

Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data being read from the device on the DO pin.
2. The Status Register contents will repeat continuously until /CS terminates the instruction.
3. The Device ID will repeat continuously until /CS terminates the instruction.
4. See Manufacturer and Device Identification table for Device ID information.

* Dual Output data
IO0 = (D6, D4, D2, D0)
IO1 = (D7, D5, D3, D1)

** Dual Input Address
IO0 = (A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0)
IO1 = (A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1)

10.2.3 Write Enable (06h)

The Write Enable instruction (Figure 4) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

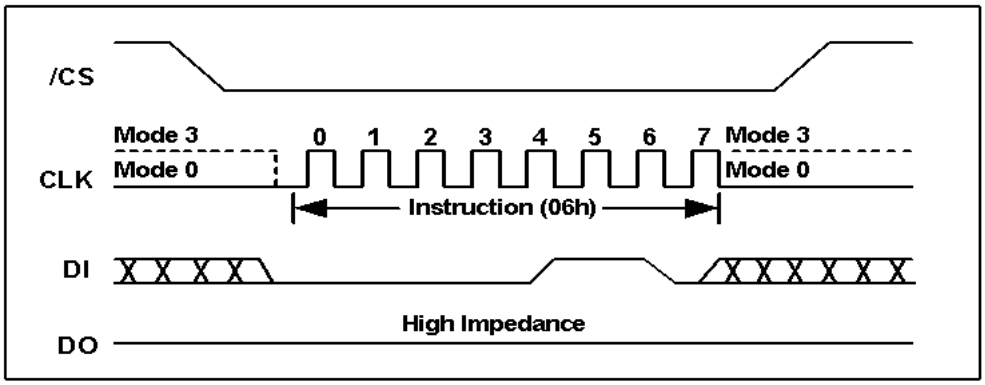


Figure 4. Write Enable Instruction Sequence Diagram

10.2.4 Write Disable (04h)

The Write Disable instruction (Figure 5) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction in entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase instructions.

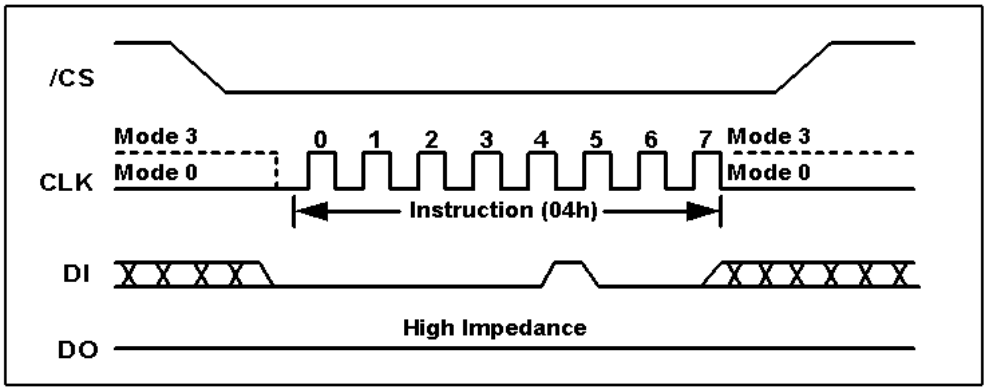


Figure 5. Write Disable Instruction Sequence Diagram

10.2.5 Read Status Register (05h)

The Read Status Register instructions allow the 8-bit Status Register to be read, The instruction is entered by driving /CS low and shifting the instruction code “05h” for Status Register into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in figure 6. The Status Register bits are shown in figure 3a and 3b include the BUSY, WEL, BP0-BP2, TB, SEC and SRP bits (see description of the Status Register earlier in this datasheet).

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 6. The instruction is completed by driving /CS high.

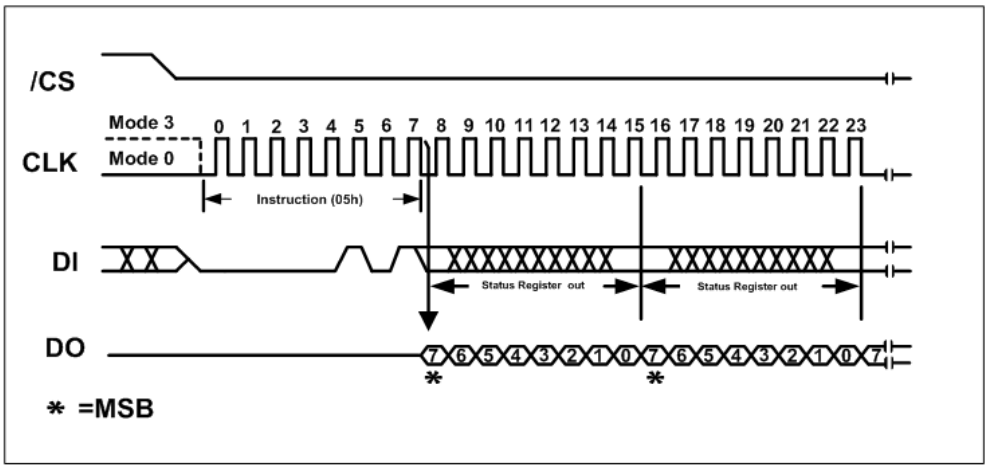


Figure 6. Read Status Register Instruction Sequence Diagram

10.2.6 Write Status Register (01h)

The Write Status Register instruction allows the Status Register to be written. A Write Enable instruction must previously have been executed for the device to accept the Write Status Register Instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code “01h”, and then writing the status register data byte as illustrated in figure 7. The Status Register bits are shown in figure 3 and described earlier in this datasheet.

Only non-volatile Status Register bits SRP, SEC, TB, BP2, BP1, BP0 (bits 7, 6, 5, 4, 3 and 2) can be written to. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction.

The /CS pin must be driven high after the eighth bit of data that is clocked in. If this is not done the Write Status Register instruction will not be executed. After /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of tw (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Register cycle has finished the Write Enable Latch (WEL) bit in Status Register will be cleared to 0.

The Write Status Register instruction allows the Block Protect bits (SEC, TB, BP2, BP1 and BP0) to be set for protecting all, a portion, or none of the memory from erase and program instructions. Protected areas become read-only (see Status Register Memory Protection table and description). The Write Status Register instruction also allows the Status Register Protect bits (SRP) to be set. This bit is used in conjunction with the Write protect (/WP) pin. Please refer to 10.1.6 for detailed descriptions Status Register protection methods. Factory default all status register bits are 0.

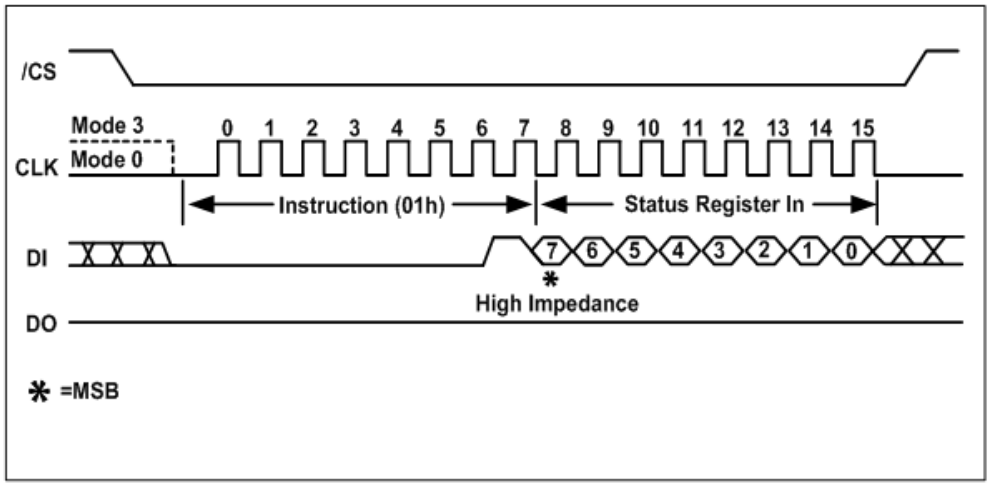


Figure 7. Write Status Register Instruction Sequence Diagram

10.2.7 Read Data (03h)

The Read Data instruction allows one more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifting out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next high address after byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high. The Read Data instruction sequence is shown in figure 8. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_R (see AC Electrical Characteristics).

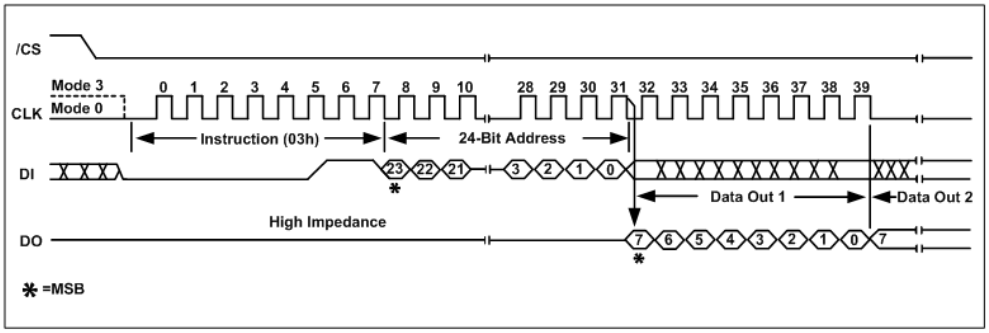


Figure 8. Read Data Register Instruction Sequence Diagram

10.2.8 Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of F_R (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in figure 9. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DO pin is a "don't care".

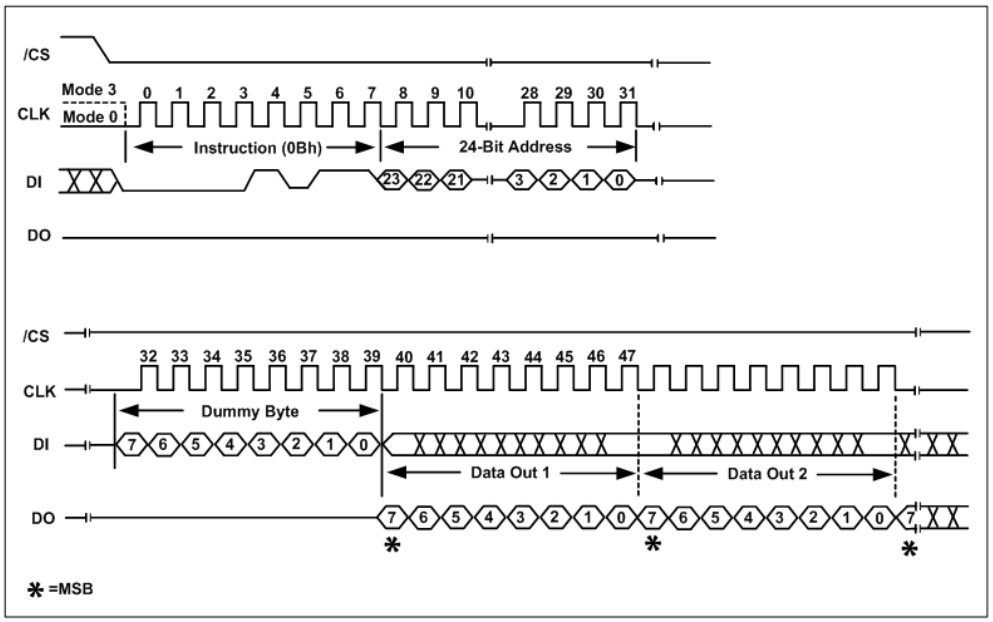


Figure 9. Fast Read Instruction Sequence Diagram

10.2.9 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; DO and DI, instead of just DO. This allows data to be transferred from the ES25M40A/80A/16A at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in figure 10. The dummy clocks allow the device’s internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the DI pin should be high-impedance prior to the falling edge of the first data out clock.

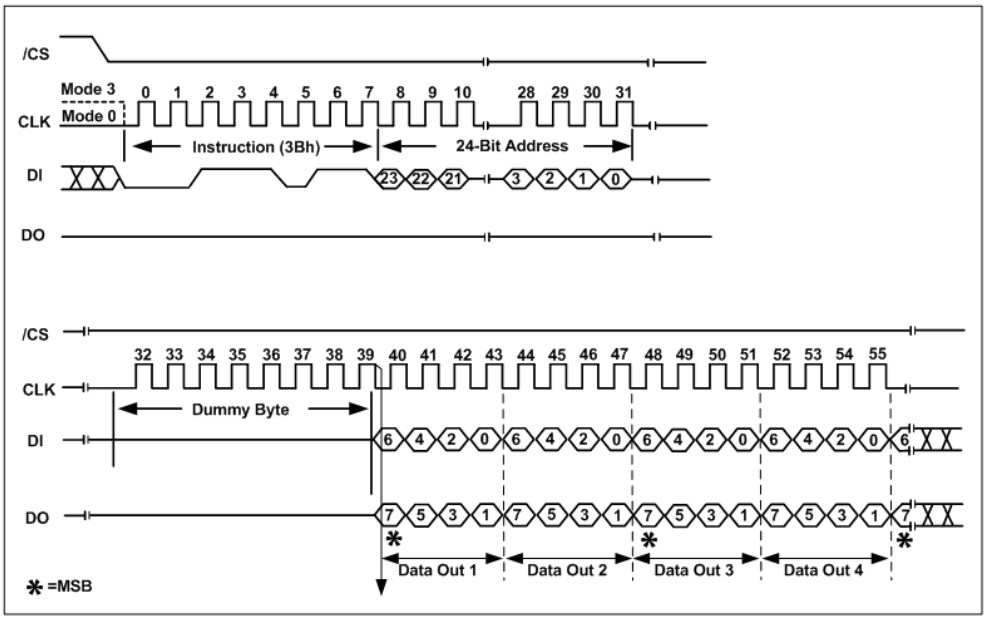


Figure 10. Fast Read Dual Output Instruction Sequence Diagram

10.2.10 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, IO_0 and IO_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications. The Fast Read Dual I/O instruction sequence is shown is figure 11.

The Mode bits (M7-0) are dummy bits. These have to be set to 0xh.

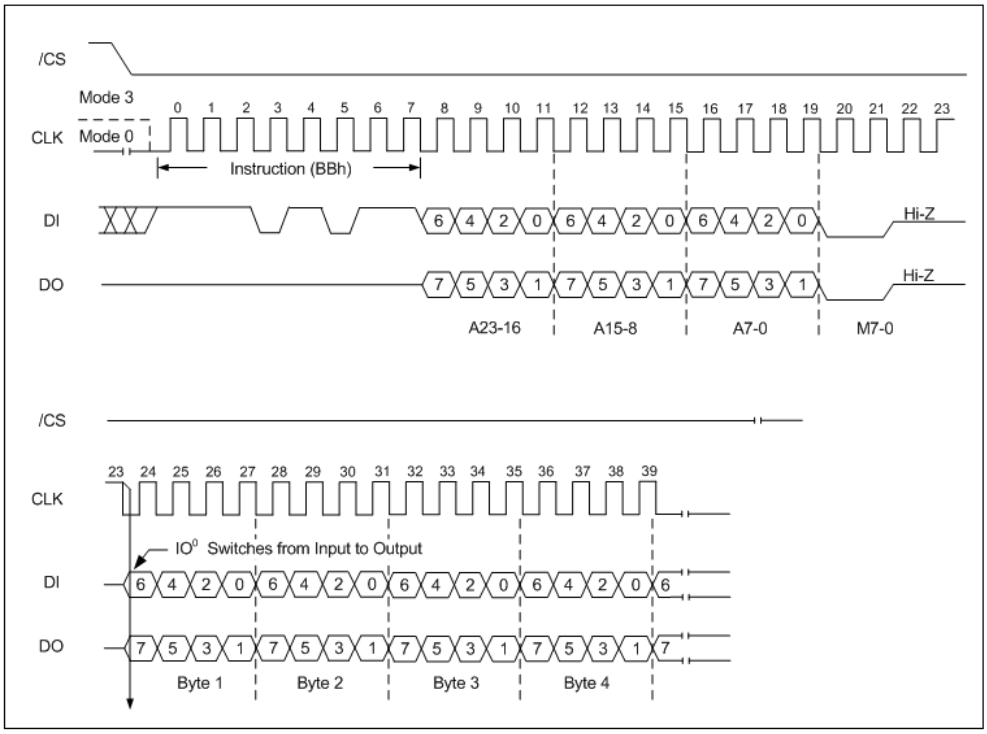


Figure 11. Fast Read Dual Input/Output Instruction Sequence Diagram (M7-0 = 0xh)

10.2.11 Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” followed by a 24-bits address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown is figure 12.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceed the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks can not exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of tpp (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (SEC, TB, BP2, BP1, and BP0) bits.

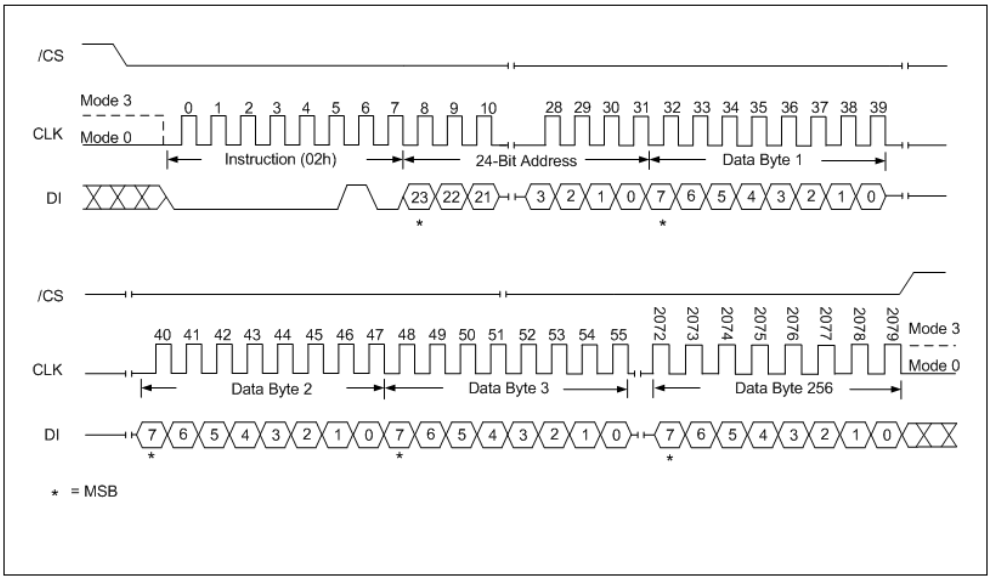


Figure 12. Page Program Instruction Sequence Diagram

10.2.12 Sector Erase (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “20h” followed a 24-bit sector address (A23-A0) (see Figure 2). The Sector Erase instruction sequence is shown in figure 13.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After /CS is driven high, the self-timed Sector Erase instruction will commence for a time duration of t_{SE} (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instruction again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (SEC, TB, BP2, BP1, and BP0) bits (see Status Register Memory protection table).

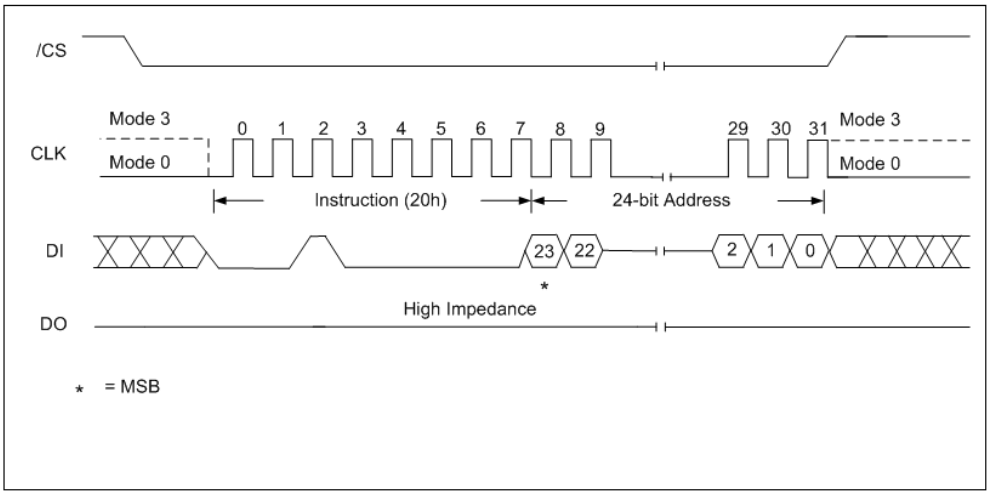


Figure 13. Sector Erase Instruction Sequence Diagram

10.2.13 Block Erase (D8h)

The Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "D8h" followed a 24-bit block address (A23-A0) (see Figure 2). The Block Erase instruction sequence is shown in figure 14.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE} (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

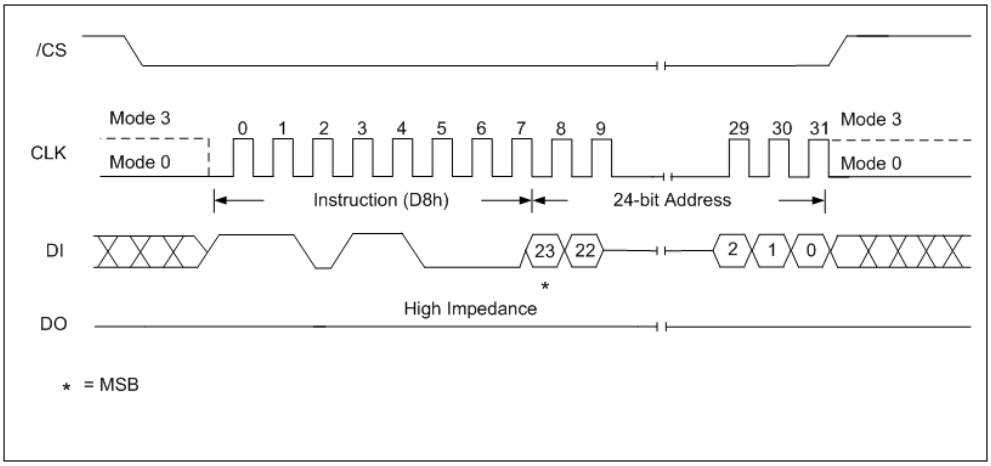


Figure 14. 64KB Block Erase Instruction Sequence Diagram

10.2.14 Chip Erase (C7h / 60h)

The Chip Erase instruction sets all memory within the device to the erased sate of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in figure 15.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of t_{CE} (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any page is protected by the Block Protect (BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

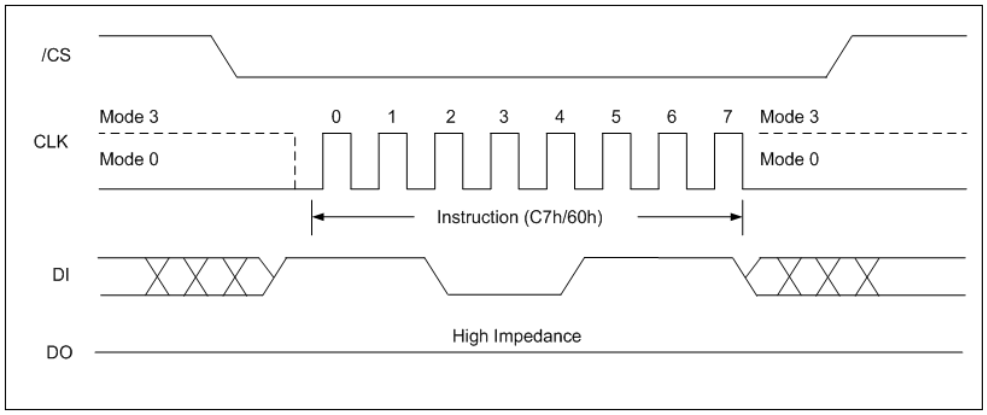


Figure 15. Chip Erase Instruction Sequence Diagram

10.2.15 Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the /CS pin low and shifting the instruction code “B9h” as shown in figure 16.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of t_{DP} (See AC Characteristics). While in the power-down state only the Release from Power-down / Device ID instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

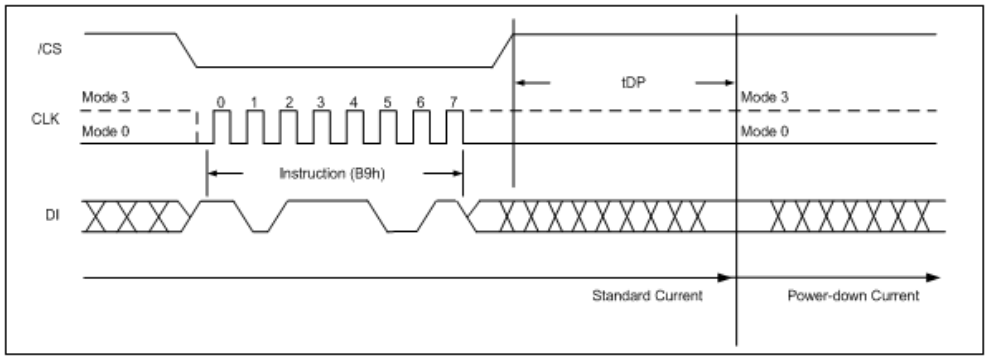


Figure 16. Deep Power-down Instruction Sequence Diagram

10.2.16 Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state or obtain the devices electronic identification (ID) number.

To release the device from the power-down state, the instruction is issued by driving the /CS pin low, shifting the instruction code “ABh” and driving /CS high as shown in figure 17. Release from power-down will take the time duration of t_{RES1} (See AC Characteristics) before the device will resume normal operation and other instructions will be accepted. The /CS pin must remain high during the t_{RES1} time duration.
When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 18. The Device ID values for the ES25M40A, ES25M80A and ES25M16A are listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving /CS high.
When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in figure 18, except that after /CS is driven high it must remain high for a time duration of t_{RES2} (See AC Characteristics). After this time duration the device will resume normal operation and other instructions will be accepted. If the Release from power-down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the instruction is ignored and will not have any effects on the current cycle.

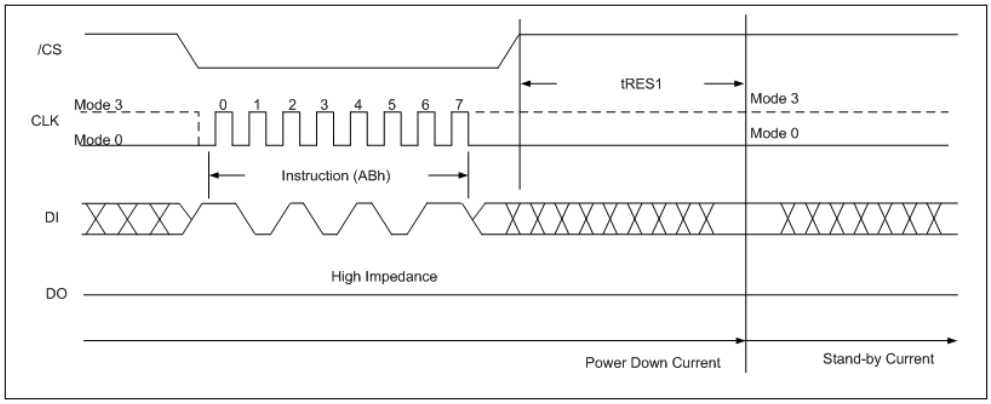


Figure 17. Release Power-down Instruction Sequence

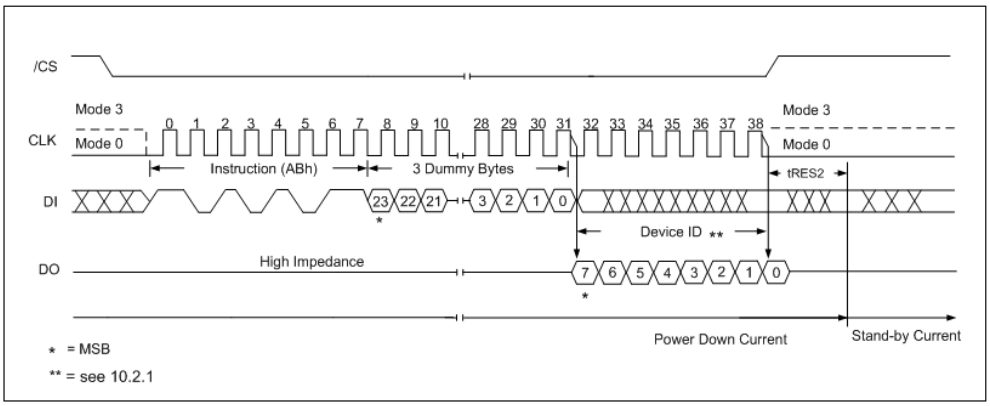


Figure 18. Release Power-down / Device ID Instruction Sequence Diagram

10.2.17 Read Manufacturer / Device ID (90h)

The Read Manufacturer / Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.
The Read Manufacturer / Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “90h” followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Excel Semiconductor (4Ah) and the Device ID are shifted out on the falling edge of CLK with most significant bit(MSB) first as shown in figure 19. The Device ID values for the ES25M40A, ES25M80A or ES25M16A are listed in Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

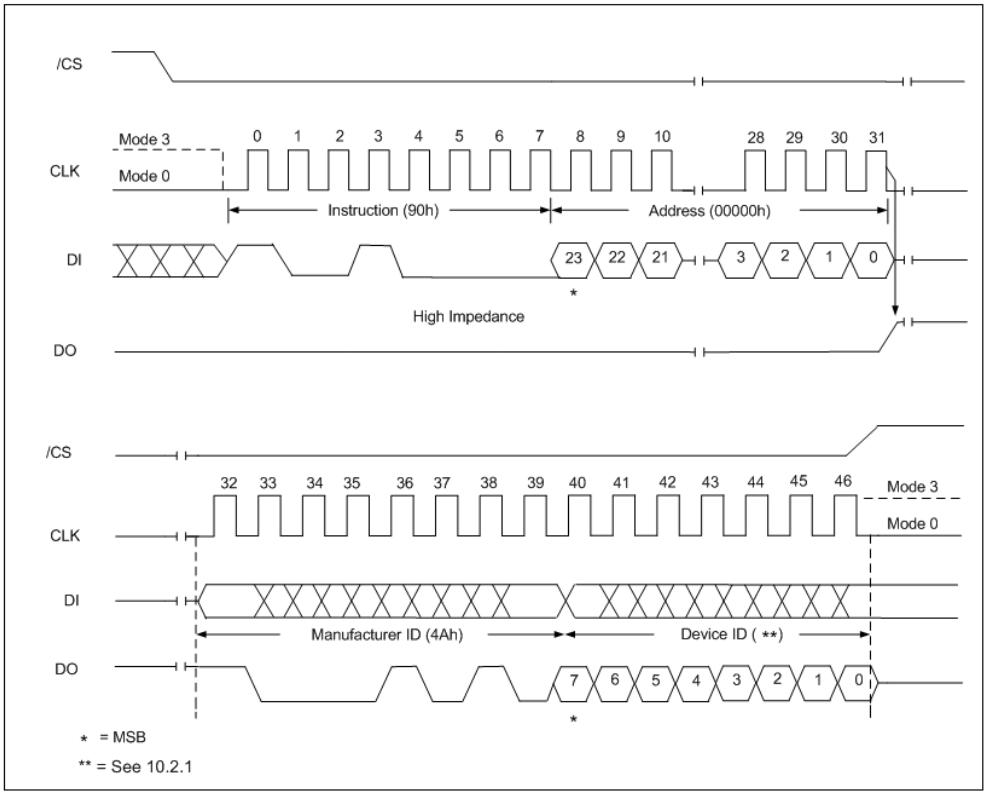


Figure 19. Read Manufacturer/ Device ID Diagram

10.2.18 Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 64-bit number that is unique to each ES25M40A, ES25M80A or ES25M16A device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the /CS pin low and shifting the instruction code “4Bh” followed by a four bytes of dummy clocks. After which, the 64-bit ID is shifted out on the falling edge of CLK as shown in figure 20.

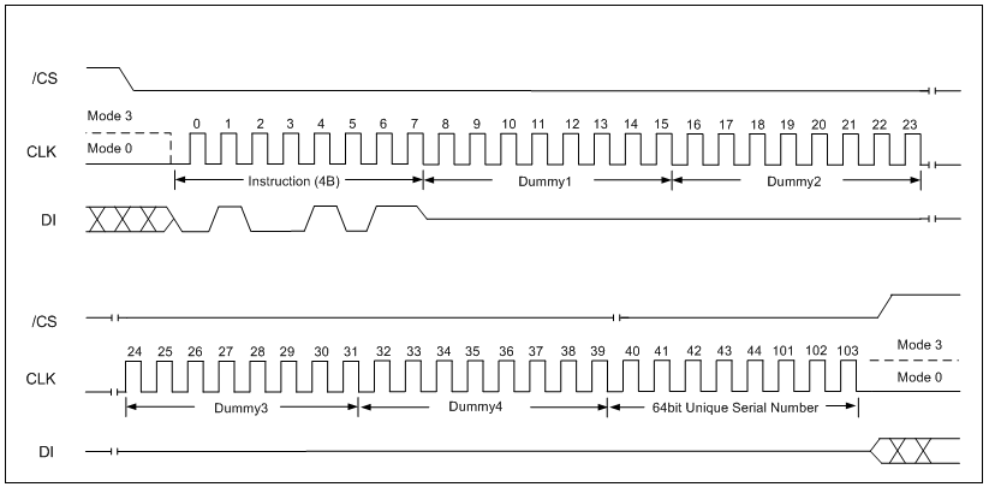


Figure 20. Read Unique ID Number Instruction Sequence

10.2.19 JEDEC ID (9Fh)

For compatibility reasons, the ES25M40A/80A/16A provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the /CS pin low and shifting the instruction code “9Fh”. The instruction JEDEC assigned Manufacturer ID byte for Excel Semiconductor(4Ah) and two Device ID bytes, Memory Type(ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first shown in figure21. For memory type and capacity values refer to Manufacturer and Device Identification table.

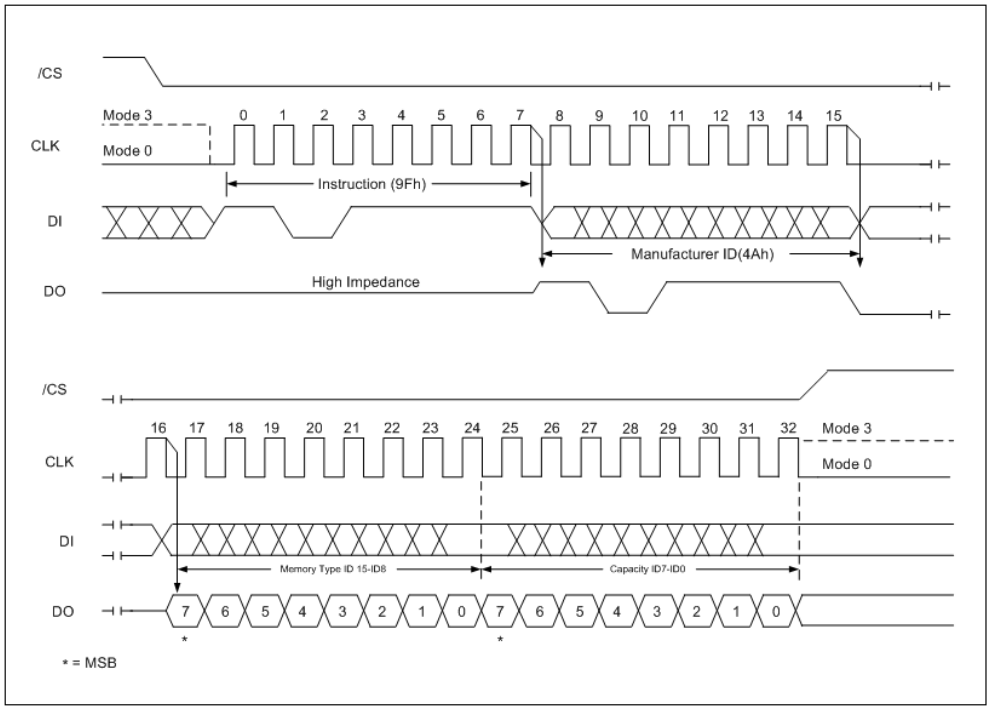


Figure 21. Read JEDEC ID

11. ELECTRICAL CHARACTERISTICS

11.1 Absolute Maximum Ratings(1)

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		-0.6 to +4.0	V
Voltage Applied to Any Pin	V_{IO}	Relative to Ground	-0.6 to VCC+0.4	V
Transient Voltage on any Pin	V_{IOT}	<20ns Transient Relative to Ground	-2.0V to VCC+2.0V	V
Storage Temperature	T_{STG}		-65 TO +150	˚C
Lead Temperature	T_{LEAD}		See Note(2)	˚C
Electrostatic Discharge Voltage	V_{ESD}	Human Body Model(3)	-2000 to +2000	V

Notes:
1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum rating may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100pF, R1=1500ohms, R2=500 ohms).

11.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage(1)	VCC	F_R =80MHz, f_R = 50MHz,	2.7	3.6	V
Ambient Temperature, Operating	T_A	Commercial Industrial	0 -40	+70 +85	˚C

Note:
1. VCC voltage during Read can operate across the min and max range but should not exceed ±10% of the programming (erase/write) voltage.

11.3 Endurance and Data Retention

PARAMETER	CONDITIONS	MIN	MAX	UNIT
Erase/Program Cycles	4KB sector, 64KB block or Full chip.		100,000	Cycles
Data Retention	Full Temperature Range		20	years

11.4 Power-up Timing and Write Inhibit Threshold

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC(min) to /CS Low	t_{VSL}(1)	10		μs
Time Delay Before Write Instruction	t_{PUW}(1)	1	10	ms
Write Inhibit Threshold Voltage	V_{WI}(1)	1	2	V

Note:

1. These parameters are characterized only.

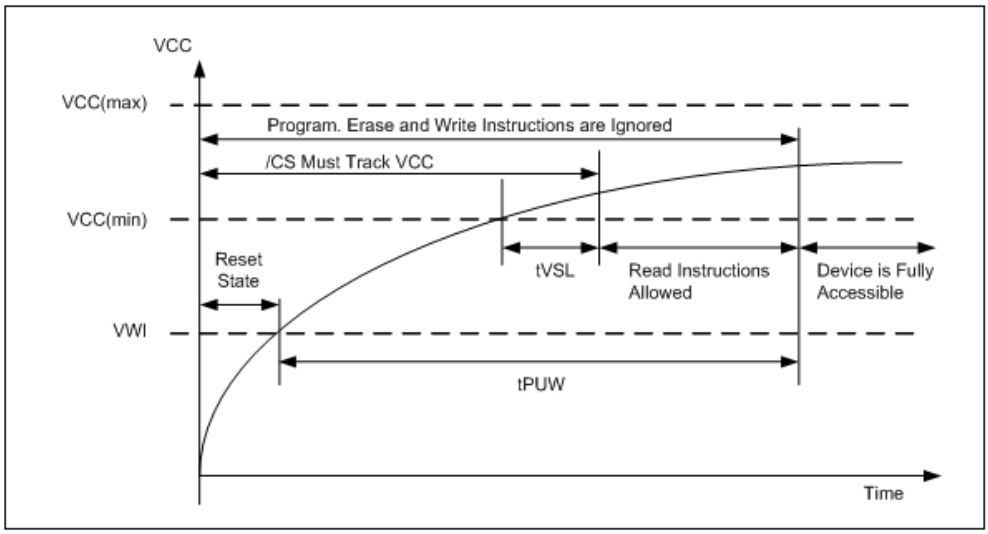


Figure 22. Power-up Timing and Voltage Levels

11.5 DC Electrical Characteristics

PARAMETER	SYMBOL	CONDITION	SPEC			UNIT
			MIN	TYP	MAX	
Input Capacitance	CIN(1)	VIN=0V			6	pF
Output Capacitance	COUT(1)	VOUT=0V			8	pF
Input Leakage	ILI				±2	μA
I/O Leakage	ILO				±2	μA
Standby Current	ICC1	/CS=VCC, VIN=GND or VCC		25	50	μA
Power-down Current	ICC2	/CS=VCC, VIN=GND or VCC		1	5	μA
Current Read Data / Dual Out 1MHz (2)	ICC3	C=0.1 VCC / 0.9VCC DO=Open		5/8	10/12	mA
Current Read Data / Dual Out 50MHz(2)	ICC3	C=0.1 VCC / 0.9VCC DO=Open		10/15	15/20	mA
Current Read Data / Dual Out 80MHz(2)	ICC3	C=0.1 VCC / 0.9VCC DO=Open		15/20	20/25	mA
Current Write Status Register	ICC4	/CS=VCC		8	12	mA
Current page Program	ICC5	/CS=VCC		20	25	mA
Current Sector/Block Erase	ICC6	/CS=VCC		20	25	mA
Current Chip Erase	ICC7	/CS=VCC		20	25	mA
Input Low Voltages	VIL		-0.5		VCCx0.3	V
Input High Voltages	VIH		VCC x0.7		VCC+0.4	V
Output Low Voltages	VOL	IOL=1.6mA			0.4	V
Output High Voltages	VOH	IOH=-100μA	VCC -0.2			V

Notes:

1. Tested on sample basis and specified through design and characterization data, TA=25˚C, VCC=3V.
2, Checker Board Pattern.

11.6 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	C_L		30	pF
Input Rise and Fall Times	T_R, T_F		5	ns
Input Pulse Voltages	V_{IN}	0.2 VCC to 0.8 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC to 0.5 VCC		V

Note:

1. Output Hi-Z is defined as the point where data out is no longer driven.

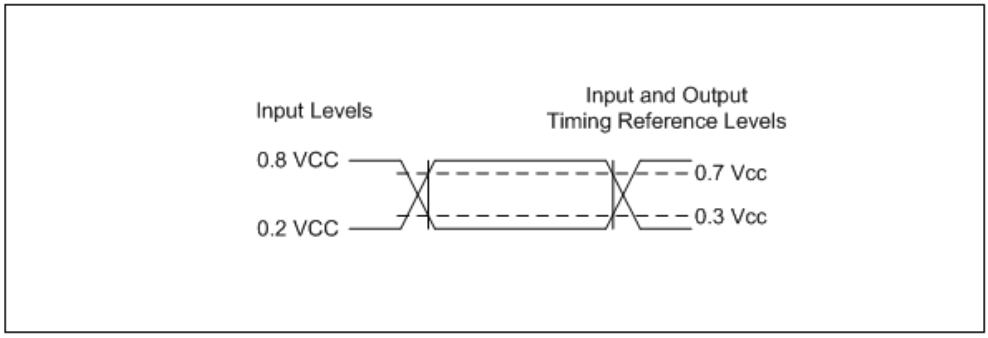


Figure 23. AC Measurement I/O Waveform

11.7 AC Electrical Characteristics

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Clock frequency For all instructions, except Read Data (03h) 2.7V-3.6V VCC & Industrial Temperature	F_R	f_c	D.C.		80	MHz
Clock freq. Read Data instruction (03h)	f_R		D.C.		50	MHz
Clock High, Low Time except Read Data (03h)	t_{CLH}, t_{CLL}(1)		6			ns
Clock High, Low Time for Read Data (03h) instructions	t_{CRLH}, t_{CRLL}(1)		8			ns
Clock Rise Time peak to peak	t_{CLCH}(2)		0.1			V/ns
Clock Fall Time peak to peak	t_{CHCL}(2)		0.1			V/ns
/CS Active Setup Time relative to CLK	t_{SLCH}	t_{CSS}	5			ns
/CS Not Active Hold Time relative to CLK	t_{CHSL}		5			ns
Data In Setup Time	t_{DVCH}	t_{DSU}	2			ns
Data In Hold Time	t_{CHDX}	t_{DH}	5			ns
/CS Active Hold Time relative to CLK	t_{CHSH}		5			ns
/CS Not Active Setup Time relative to CLK	t_{SHCH}		5			ns
/CS Deselect Time (for Read instructions/ Write, Erase and Program instructions)	t_{SHSL}	t_{CSH}	100			ns
Output Disable Time	t_{SHQZ}(2)	t_{DIS}			7	ns
Clock Low to Output Valid 2.7V-3.6V / 3.0V-3.6V	T_{CLQV}	t_V			7/6	ns
Output Hold Time	t_{CLQX}	t_{HO}	0			ns
/Hold Active Setup Time relative to CLK	t_{HLCH}		5			ns

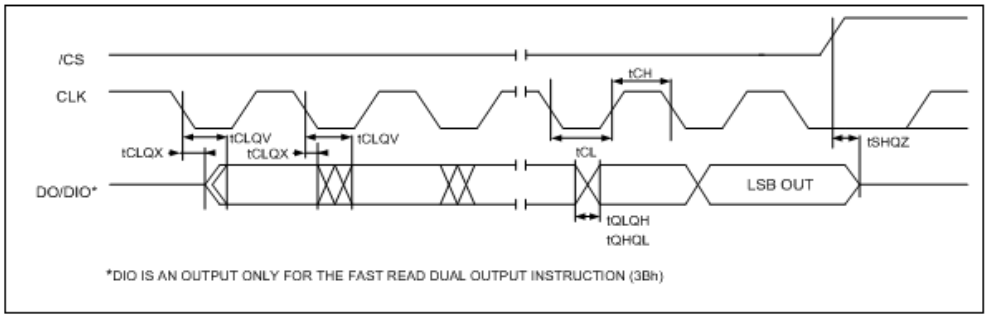
Continued – Next page

11.8 AC Electrical Characteristics (cont'd)

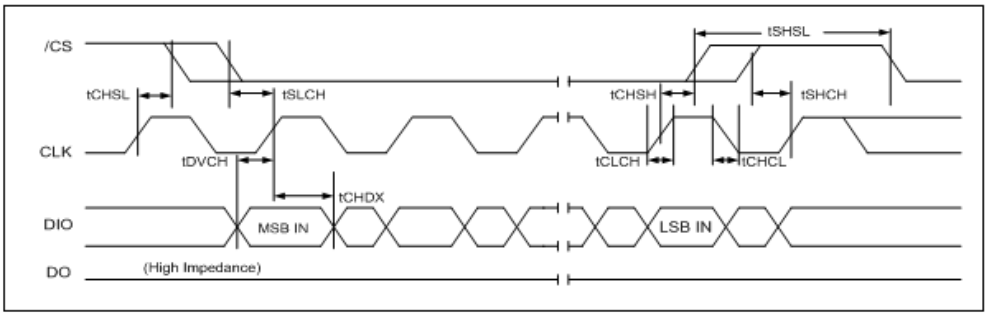
DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
/HOLD Active Hold Time relative to CLK	t_{CHHH}		5			ns
/HOLD Not Active Setup Time relative to CLK	t_{HHCH}		5			ns
/HOLD Not Active Hold Time relative to CLK	t_{CHHL}		5			ns
/HOLD to Output Low-Z	t_{HHQX}(2)	t_{LZ}			7	ns
/HOLD to Output High-Z	t_{HLQZ}(2)	t_{HZ}			12	ns
Write Protect Setup Time Before /CS Low	t_{WHSL}(3)		20			ns
Write Protect Setup Time After /CS High	t_{SHWL}(3)		100			ns
/CS High to Power-down Mode	t_{DP}(2)				3	μs
/CS High to Standby Mode without Electronic Signature Read	t_{RES1}(2)				3	μs
/CS High to Standby Mode with Electronic Signature Read	t_{RES2}(2)				1.8	μs
Write Status Register Time	tw			10	15	ms
Byte Program Time	t_{BP}			10	150	μs
Page Program Time	t_{PP}			1.5	3	ms
Sector Erase Time(4KB)	t_{SE}			120	200	ms
Block Erase Time(64KB)	t_{BE2}			0.75	1.5	s
Chip Erase Time ES25M40A	t_{CE}			6	12	s
Chip Erase Time ES25M80A				12	25	s
Chip Erase Time ES25M16A				25	40	s

Notes:
1. Clock high + Clock low must be less than or equal to 1/fc.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Only applicable as a constraint for a Write Status Register instruction when Sector Protect Bit is set to 1.
4. Commercial temperature only applies to Fast Read(F_R).Industrial temperature applies to all other parameters.

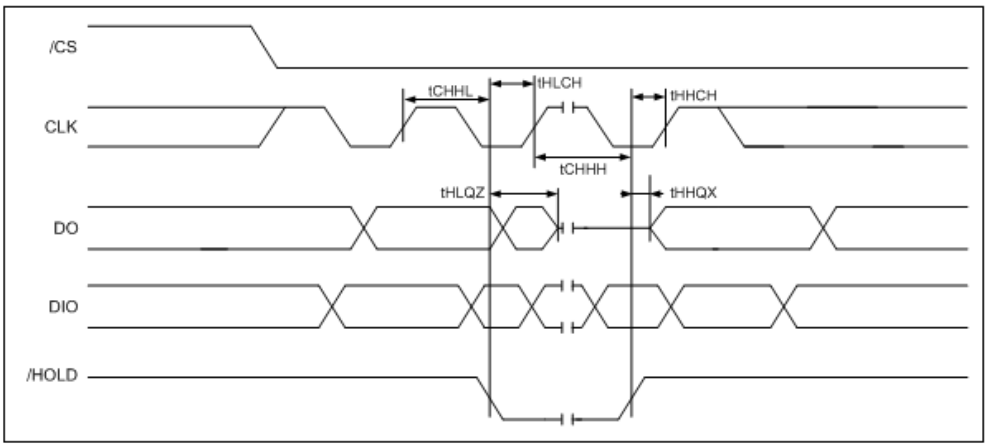
11.9 Serial Output Timing



11.10 Input Timing

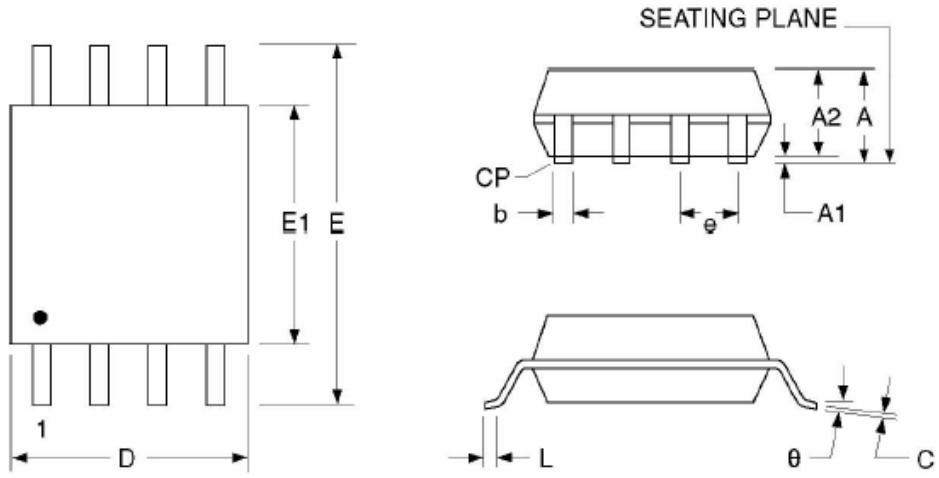


11.11 Hold Timing



12. PACKAGE SPECIFICATION

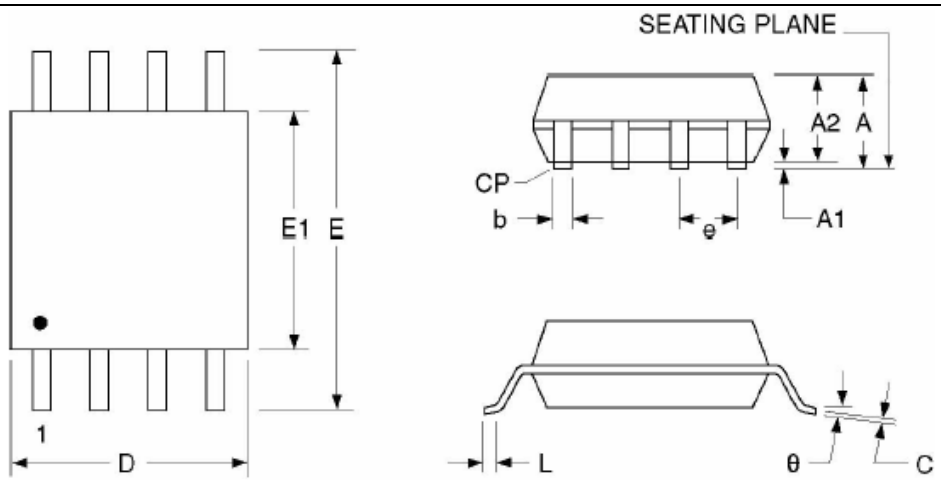
12.1 8-Pin SOIC 150-mil



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.47	1.72	0.058	0.068
A1	0.10	0.24	0.004	0.009
A2	1.45		0.057	
b	0.33	0.50	0.013	0.020
C	0.19	0.25	0.0075	0.098
D(3)	4.8	4.95	0.189	0.195
E	5.8	6.19	0.228	0.244
E1(3)	3.8	4.00	0.150	0.157
e(2)	1.27BSC		0.050 BSC	
L	0.40	1.27	0.015	0.050
Θ	0°	8°	0°	8°
y	---	0.076	---	0.003

Notes:
1. Controlling dimensions: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.

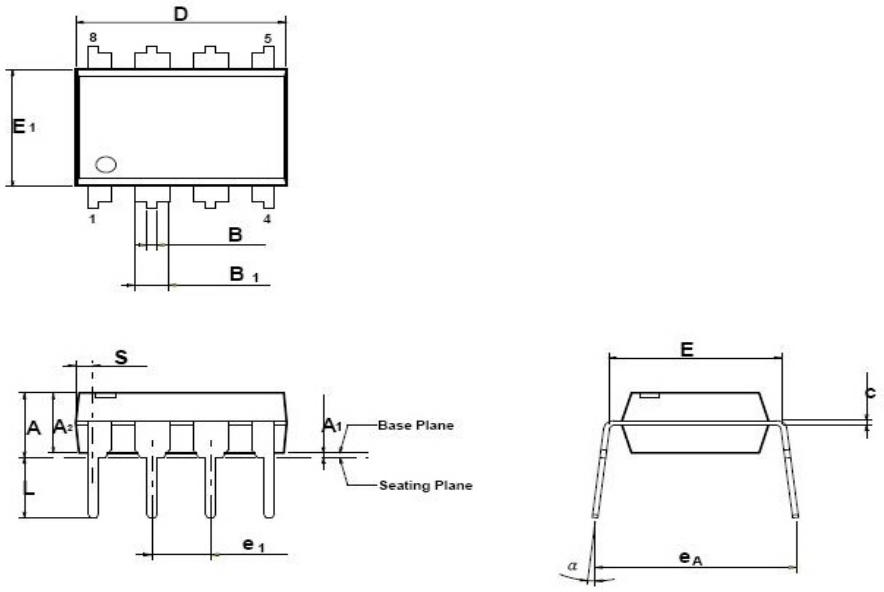
12.2 8-Pin SOIC 208-mil



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.75	2.16	0.069	0.085
A1	0.05	0.25	0.002	0.010
A2	1.70	1.91	0.067	0.075
b	0.35	0.48	0.014	0.019
C	0.19	0.25	0.007	0.010
D	5.18	5.38	0.204	0.212
E	7.70	8.10	0.303	0.319
E1	5.18	5.38	0.204	0.212
e	1.27 BSC		0.050 BSC	
L	0.50	0.80	0.020	0.031
θ	0°	8°	0°	8°
y	---	0.10	---	0.004

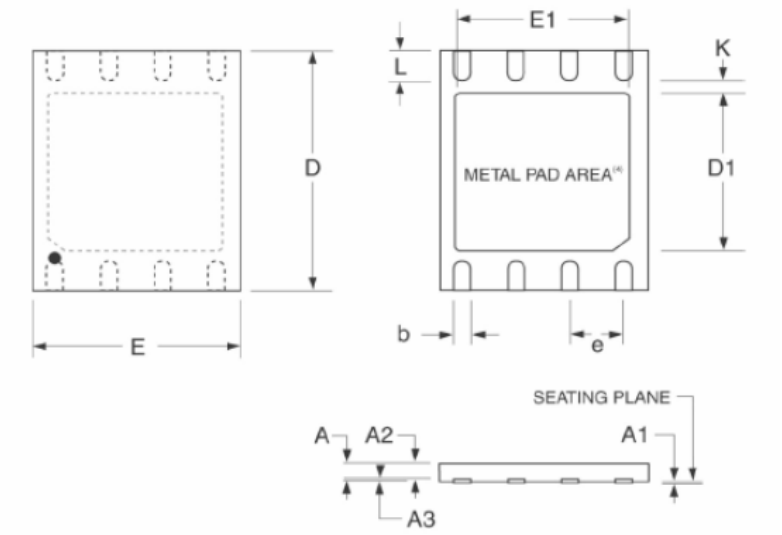
Notes:
1. BSC = Basic lead spacing between centers.
2. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
3. Formed leads shall be planar with respect to one another within. 0004 inches at the seating plane.

12.3 8-Pin PDIP 300-mil



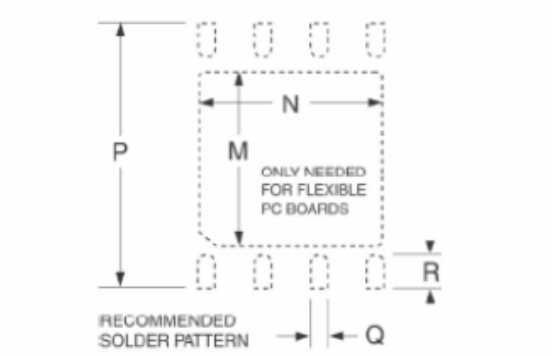
SYMBOL	Dimension in inch			Dimension in mm		
	MIN	Nom	MAX	MIN	Nom	MAX
A	---	---	0.175	---	---	4.45
A_1	0.010	---	---	0.25	---	---
A_2	0.125	0.130	0.135	3.18	3.30	3.43
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.058	0.060	0.064	1.47	1.52	1.63
c	0.008	0.010	0.014	0.20	0.25	0.36
D	---	0.360	0.380	---	9.14	9.65
E	0.290	0.300	0.310	7.37	7.62	7.87
E_1	0.245	0.250	0.255	6.22	6.35	6.48
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
α	0	---	15	0	---	15
e A	0.335	0.355	0.375	8.51	9.02	9.53
S	---	---	0.045	---	---	1.14

12.4 8-contact 6x5 WSON



SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP.	MAX	MIN	TYP.	MAX
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	0.02	0.05	0.0000	0.0008	0.0019
A2		0.55			0.0126	
A3	0.19	0.20	0.25	0.0075	0.0080	0.0098
b	0.36	0.40	0.48	0.0138	0.0157	0.0190
D(3)	5.90	6.00	6.10	0.2320	0.2360	0.2400
D1	3.30	3.40	3.50	0.1299	0.1338	0.1377
E	4.90	5.00	5.10	0.1930	0.1970	0.2010
E1(3)	4.20	4.30	4.40	0.1653	0.1692	0.1732
e(2)	1.27 BSC			0.0500 BSC		
K	0.20			0.0080		
L	0.50	0.60	0.75	0.0197	0.0236	0.0295

12.5 8-contact 6x5 WSON Cont'd.



SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP.	MAX	MIN	TYP.	MAX
SOLDER PATTERN						
M		3.40			0.1338	
N		4.30			0.1692	
P		6.00			0.2360	
Q		0.50			0.0196	
R		0.75			0.0255	

Notes:
1. Advanced Packaging Information; please contact to Excel Semiconductor for the latest minimum and maximum specifications.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. The metal pad area on the bottom center of the package is connected to the device ground (GND pin). Avoid placement of exposed PCB bias under the pad.

13. ORDERING INFORMATION

Standard Products

Excel Semiconductor standard products are available in several package and operating ranges.

The order number (Valid Combination) is formed by a combination of the following:

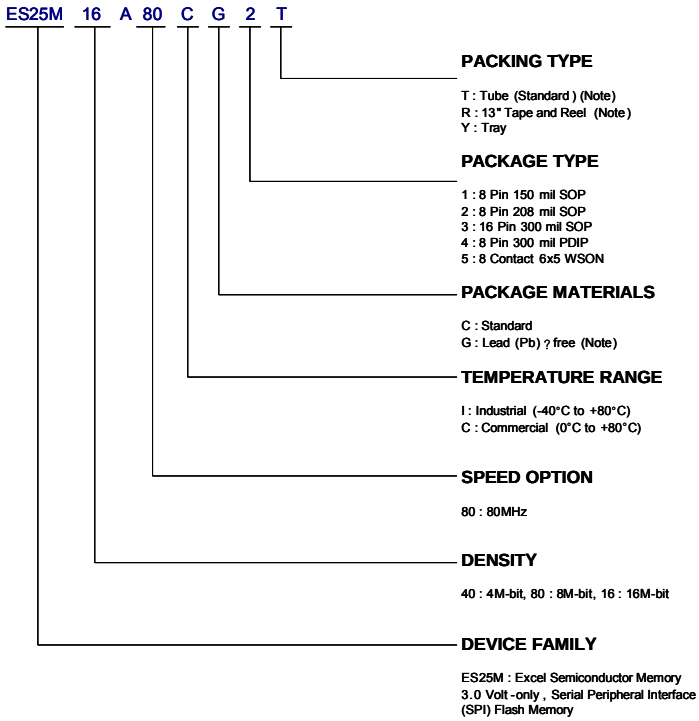


Table 1. ES25MxxA Valid Combinations

ES25MxxA Valid Combinations					
Base Ordering Part Number	Speed Option	Temperature & Package Material	Package Type	Packing Type	Package Marking
ES25M40A ES25M80A ES25M16A	80	CG, CC, IG, IC (Note)	1, 2, 4, 5 2, 4, 5 2, 3, 4, 5	T, R, Y (Note)	M16A + (Speed) +(Temp) + (Package Material)

Notes.
Contact your local sales office for availablity

14. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPSION
A	12/28/07		Initial release of data sheet
B	01/03/08		Changed device name (ES25Mxx → ES25MxxA)
C	02/19/08		Added Fast Read Dual I/O
D	02/25/08	47	Changed Ordering Informaton.
E	08/14/08	40	Changed Byte Program Time