

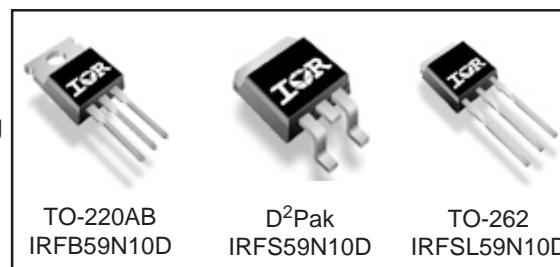
Applications

- High frequency DC-DC converters

V_{DSS}	R_{DS(on)} max	I_D
100V	0.025Ω	59A

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	59	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	42	
I _{DM}	Pulsed Drain Current ①	236	
P _D @ T _A = 25°C	Power Dissipation ②	3.8	W
P _D @ T _C = 25°C	Power Dissipation	200	
	Linear Derating Factor	1.3	W/°C
V _{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	3.3	V/ns
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw④	10 lbf•in (1.1N•m)	

Typical SMPS Topologies

- Half-bridge and Full-bridge DC-DC Converters
- Full-bridge Inverters

Notes ① through ④ are on page 11
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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.025	Ω	$V_{GS} = 10V, I_D = 35.4A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 100V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 80V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	18	—	—	S	$V_{DS} = 50V, I_D = 35.4A$
Q_g	Total Gate Charge	—	76	114	nC	$I_D = 35.4A$
Q_{gs}	Gate-to-Source Charge	—	24	36		$V_{DS} = 80V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	36	54		$V_{GS} = 10V, \text{④}$
$t_{d(on)}$	Turn-On Delay Time	—	16	—	ns	$V_{DD} = 50V$
t_r	Rise Time	—	90	—		$I_D = 35.4A$
$t_{d(off)}$	Turn-Off Delay Time	—	20	—		$R_G = 2.5\Omega$
t_f	Fall Time	—	12	—		$V_{GS} = 10V, \text{④}$
C_{iss}	Input Capacitance	—	2450	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	740	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	190	—		$f = 1.0\text{MHz}$ ⑥
C_{oss}	Output Capacitance	—	3370	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	390	—		$V_{GS} = 0V, V_{DS} = 80V, f = 1.0\text{MHz}$
$C_{oss\ eff.}$	Effective Output Capacitance	—	690	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 80V$ ⑤

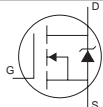
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	510	mJ
I_{AR}	Avalanche Current ①	—	35.4	A
E_{AR}	Repetitive Avalanche Energy ①	—	20	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ⑥	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ⑦	—	62	
$R_{\theta JA}$	Junction-to-Ambient ⑦	—	40	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	59	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	236		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 35.4A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	130	200	ns	$T_J = 25^\circ\text{C}, I_F = 35.4A$
Q_{rr}	Reverse Recovery Charge	—	0.75	1.1	μC	$di/dt = 100A/\mu\text{s}$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

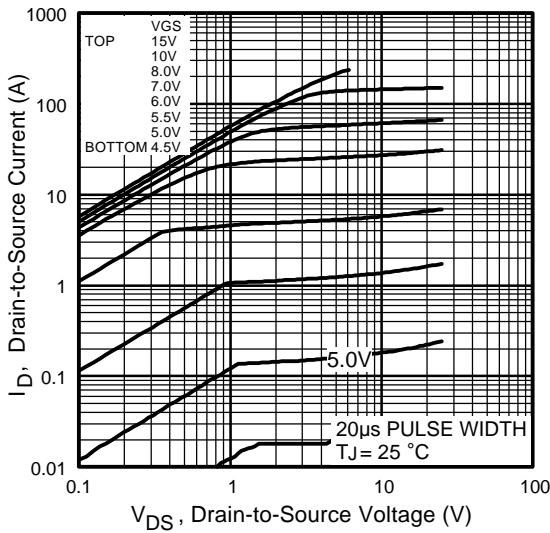


Fig 1. Typical Output Characteristics

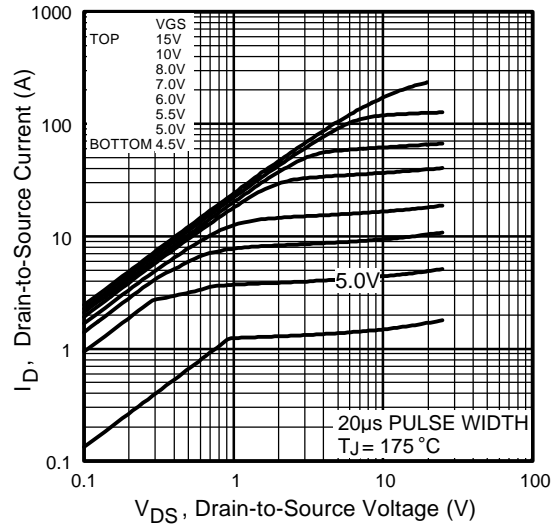


Fig 2. Typical Output Characteristics

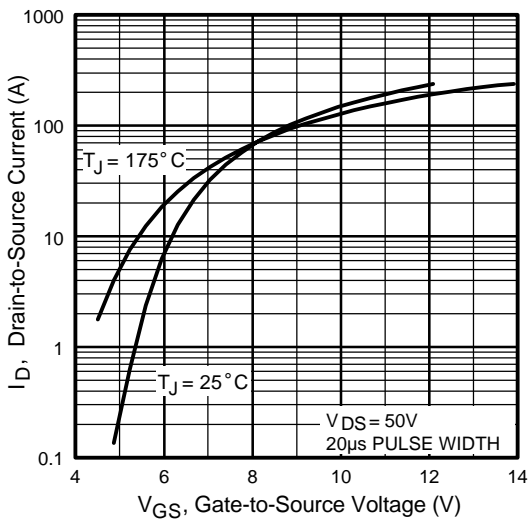


Fig 3. Typical Transfer Characteristics

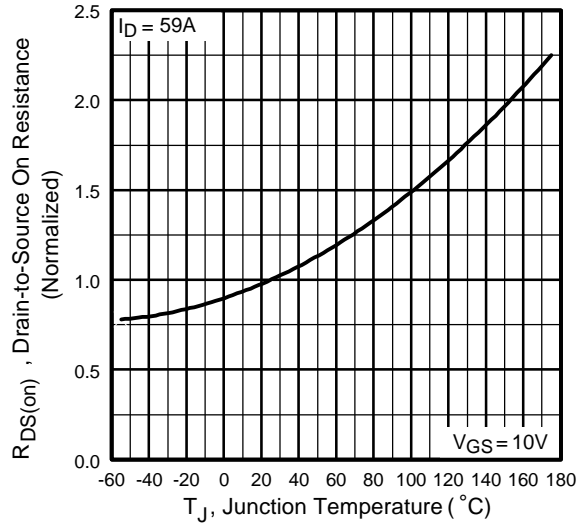


Fig 4. Normalized On-Resistance Vs. Temperature

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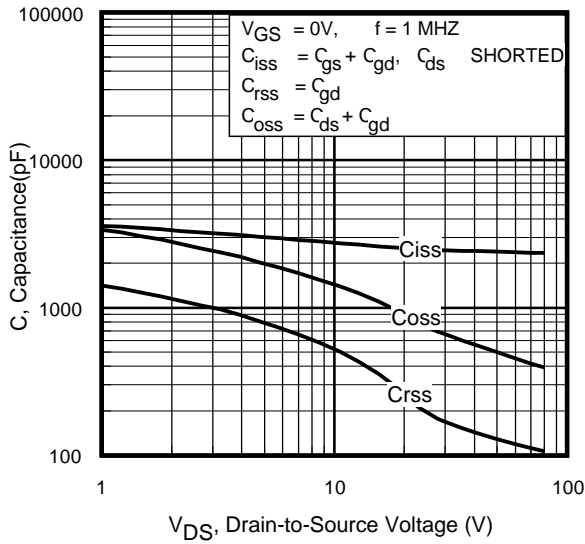


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

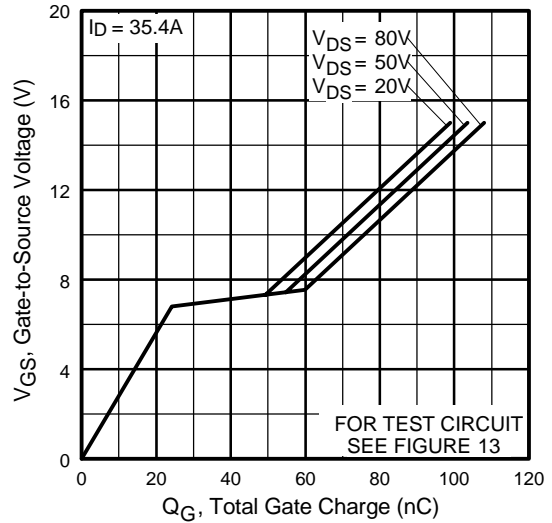


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

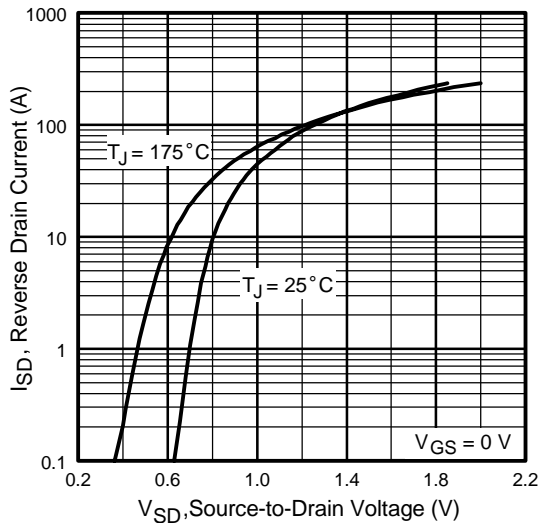


Fig 7. Typical Source-Drain Diode Forward Voltage

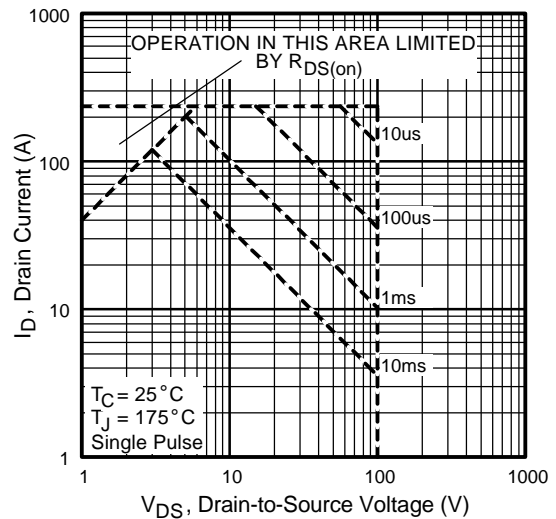


Fig 8. Maximum Safe Operating Area

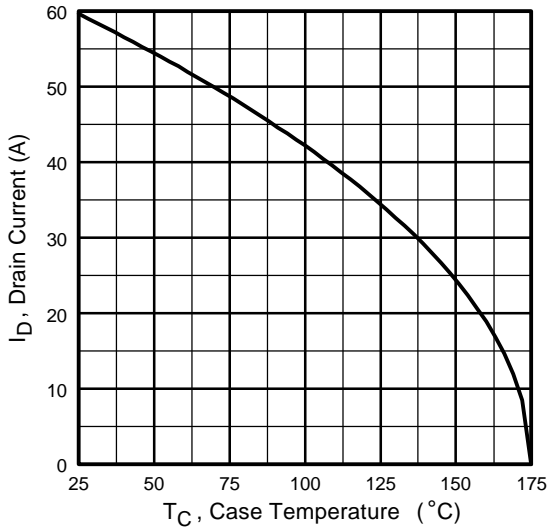


Fig 9. Maximum Drain Current Vs. Case Temperature

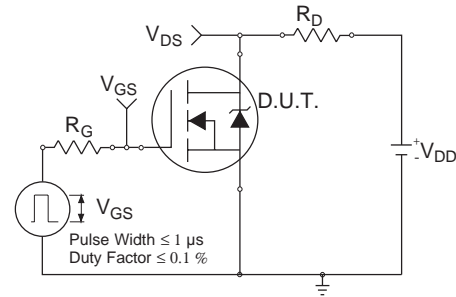


Fig 10a. Switching Time Test Circuit

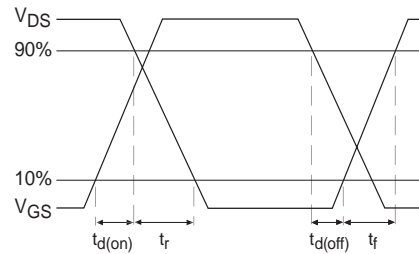


Fig 10b. Switching Time Waveforms

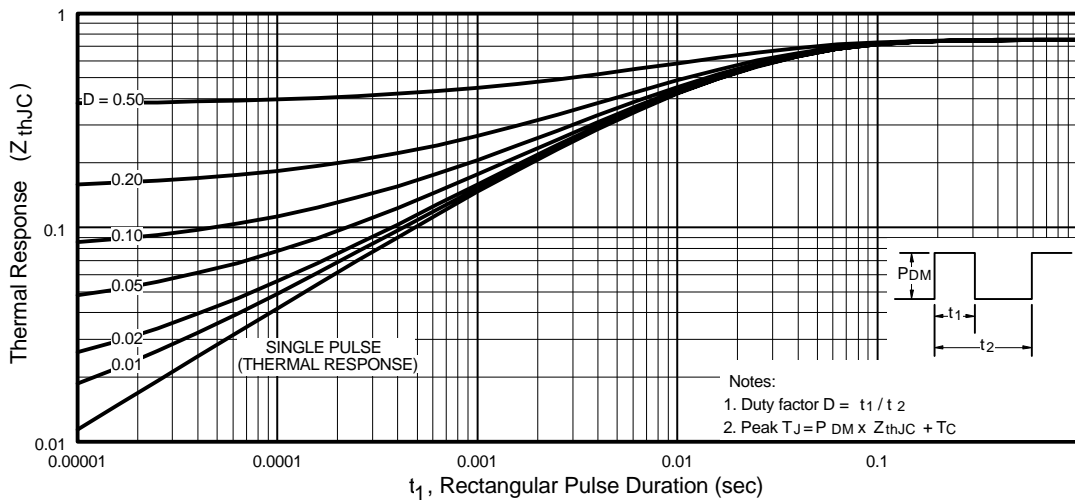


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

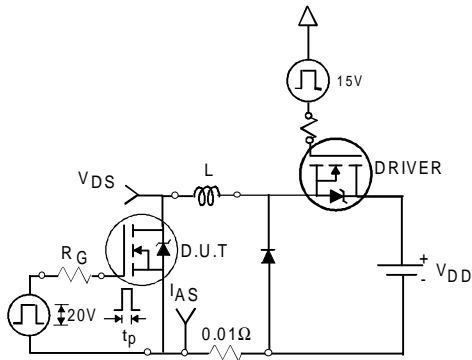


Fig 12a. Unclamped Inductive Test Circuit

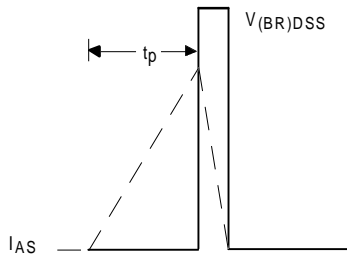


Fig 12b. Unclamped Inductive Waveforms

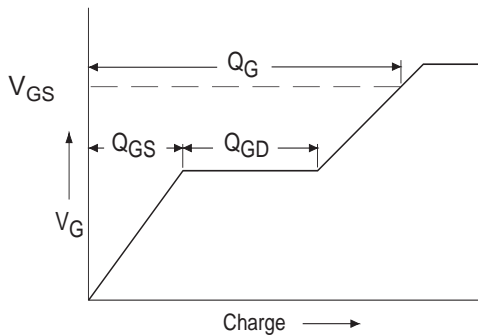


Fig 13a. Basic Gate Charge Waveform

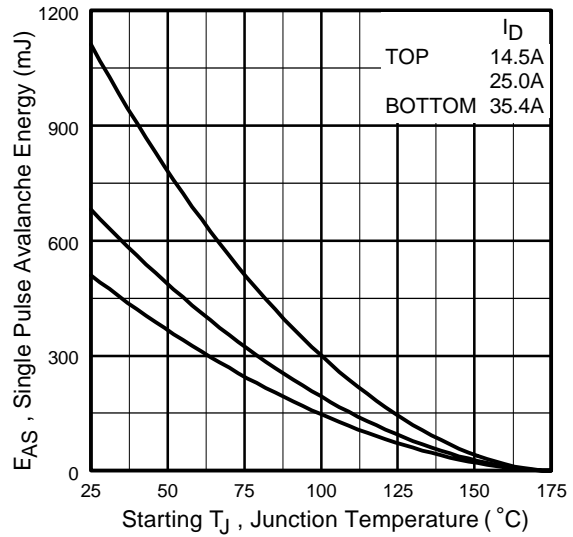


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

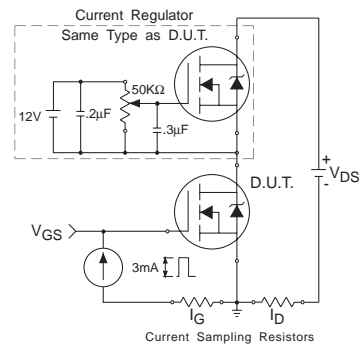
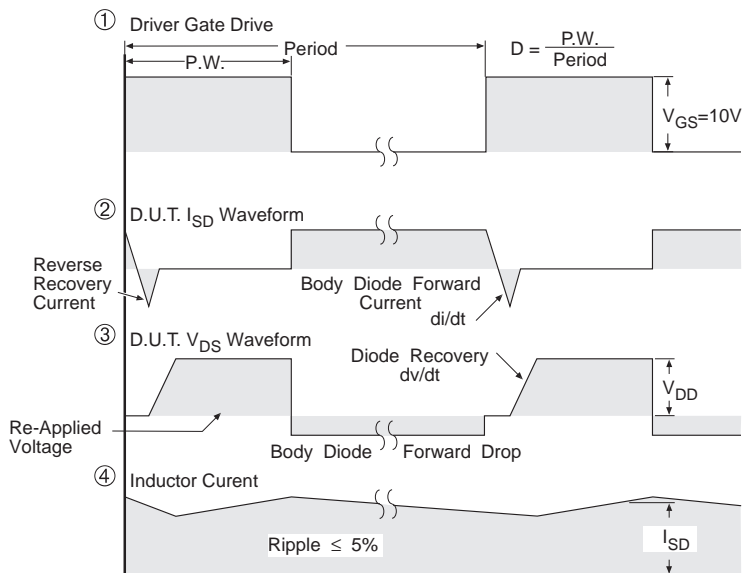
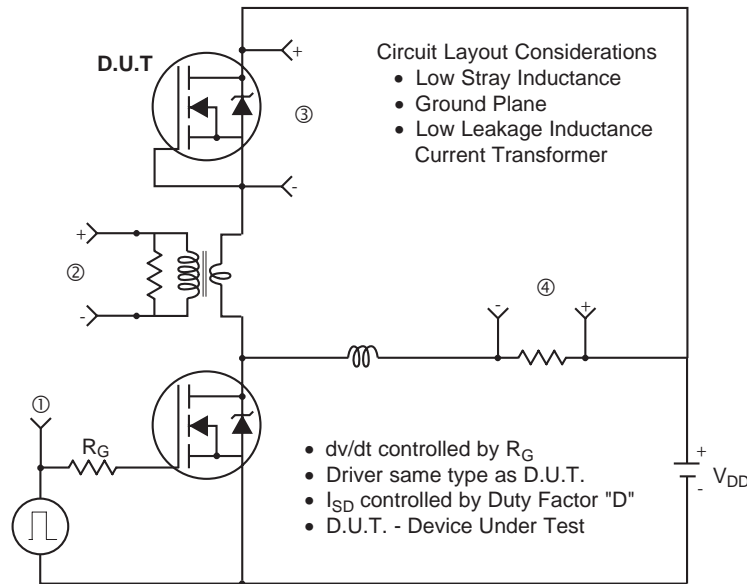


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

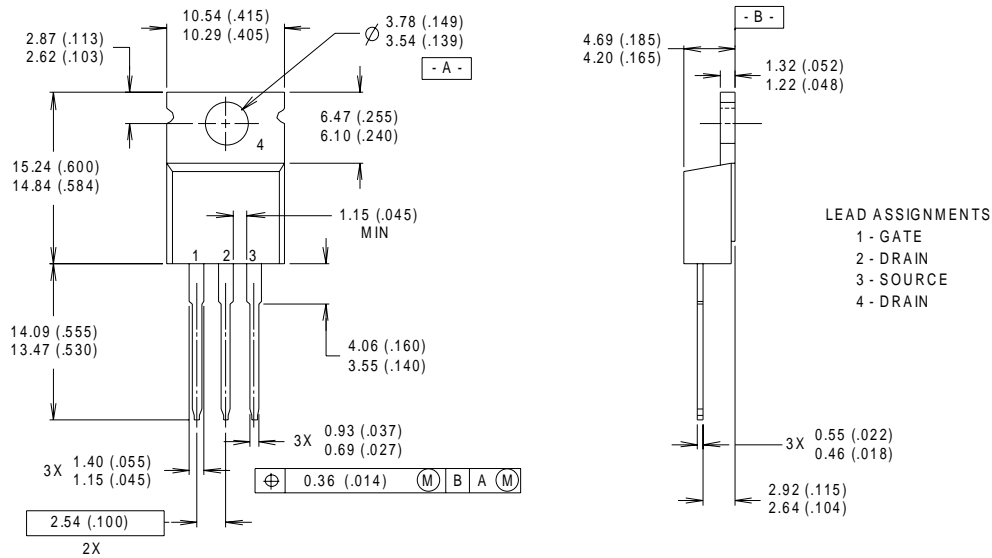
Fig 14. For N-Channel HEXFET® Power MOSFETs

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TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

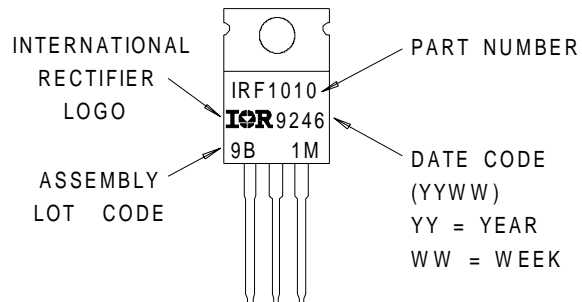


NOTES:

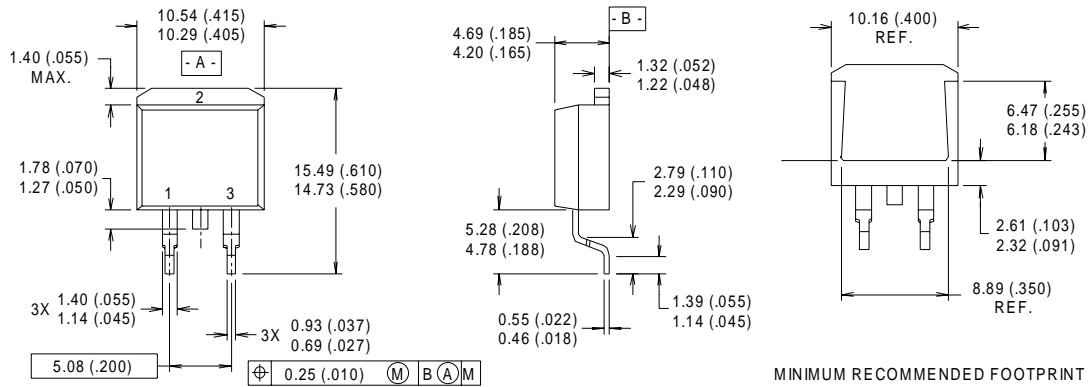
- 1 DIMENSIONING & TOLERANCING PER ANS Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE : THIS IS AN IRF1010
 WITH ASSEMBLY
 LOT CODE 9B1M



D²Pak Package Outline

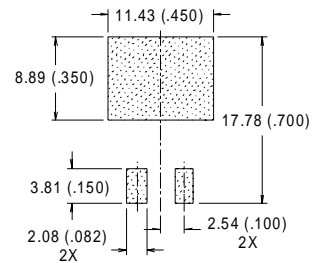


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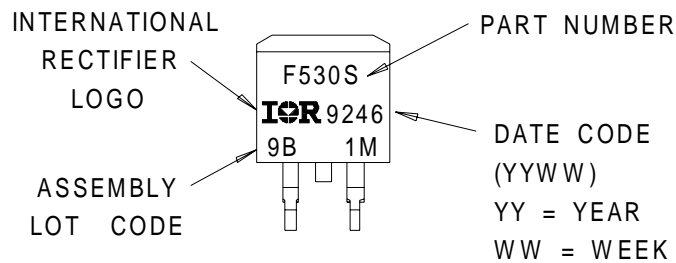
- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE



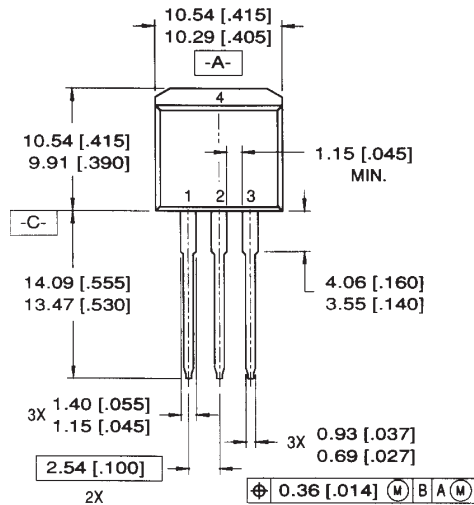
D²Pak Part Marking Information



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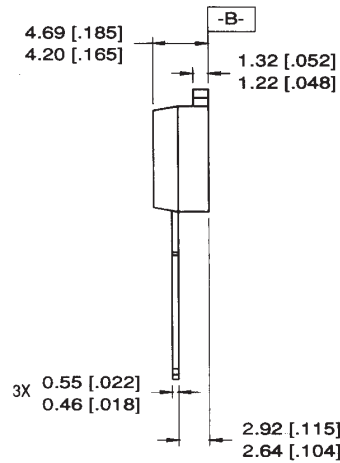
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TO-262 Package Outline



LEAD ASSIGNMENTS

1 = GATE 3 = SOURCE
2 = DRAIN 4 = DRAIN

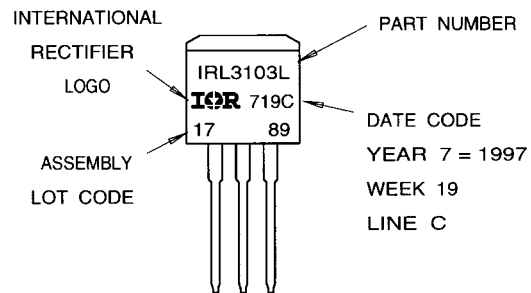


NOTES:

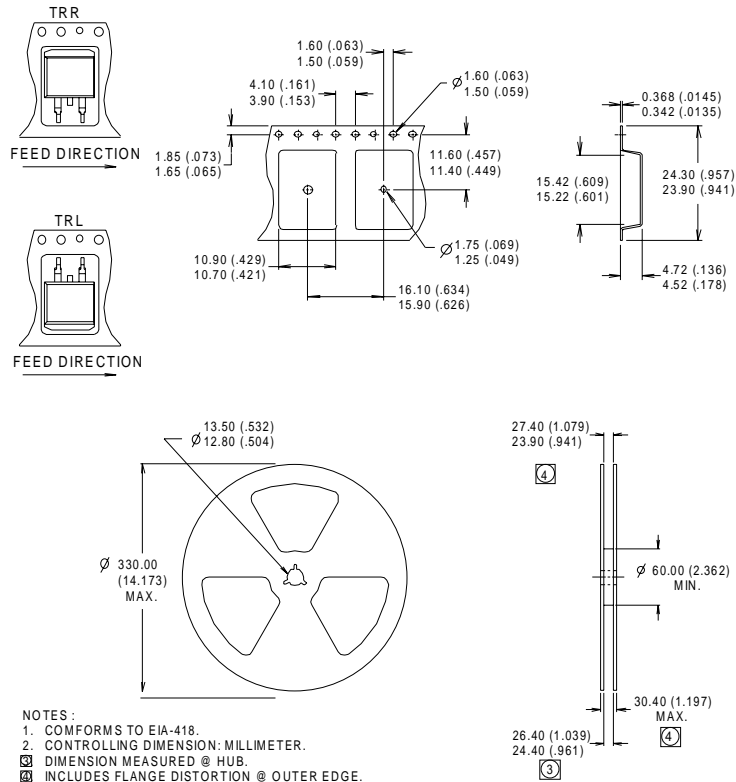
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



D²Pak Tape & Reel Information



NOTES:
 1. CONFORMS TO EIA-418.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION MEASURED @ HUB.
 4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.8\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 35.4\text{A}$.
- ③ $I_{SD} \leq 35.4\text{A}$, $di/dt \leq 350\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ This is only applied to TO-220AB package
- ⑦ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material).
 For recommended footprint and soldering techniques refer to application note #AN-994.

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
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IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN: 16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
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