

## FEATURES

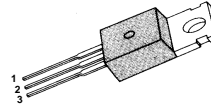
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 10  $\mu$ A (Max.) @  $V_{DS} = 200V$
- Low  $R_{DS(ON)}$  : 0.333  $\Omega$  (Typ.)

$$BV_{DSS} = 200 V$$

$$R_{DS(on)} = 0.4 \Omega$$

$$I_D = 9 A$$

## TO-220



1.Gate 2. Drain 3. Source

## Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
$V_{DSS}$	Drain-to-Source Voltage	200	V
$I_D$	Continuous Drain Current ( $T_C=25^\circ C$ )	9	A
	Continuous Drain Current ( $T_C=100^\circ C$ )	5.7	
$I_{DM}$	Drain Current-Pulsed ①	36	A
$V_{GS}$	Gate-to-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy ②	162	mJ
$I_{AR}$	Avalanche Current ①	9	A
$E_{AR}$	Repetitive Avalanche Energy ①	7.2	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
$P_D$	Total Power Dissipation ( $T_C=25^\circ C$ )	72	W
	Linear Derating Factor	0.57	
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	- 55 to +150	$^\circ C$
$T_L$	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

## Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	1.74	$^\circ C/W$
$R_{\theta CS}$	Case-to-Sink	0.5	--	
$R_{\theta JA}$	Junction-to-Ambient	--	62.5	

Rev. B

### Electrical Characteristics (T<sub>C</sub>=25°C unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	200	--	--	V	V <sub>GS</sub> =0V, I <sub>D</sub> =250 μA
ΔBV/ΔT <sub>J</sub>	Breakdown Voltage Temp. Coeff.	--	0.21	--	V/°C	I <sub>D</sub> =250 μA <b>See Fig 7</b>
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	--	4.0	V	V <sub>DS</sub> =5V, I <sub>D</sub> =250 μA
I <sub>GSS</sub>	Gate-Source Leakage, Forward	--	--	100	nA	V <sub>GS</sub> =30V
	Gate-Source Leakage, Reverse	--	--	-100		V <sub>GS</sub> =-30V
I <sub>DSS</sub>	Drain-to-Source Leakage Current	--	--	10	μA	V <sub>DS</sub> =200V
		--	--	100		V <sub>DS</sub> =160V, T <sub>C</sub> =125°C
R <sub>DS(on)</sub>	Static Drain-Source On-State Resistance	--	--	0.4	Ω	V <sub>GS</sub> =10V, I <sub>D</sub> =4.5A ④
g <sub>fs</sub>	Forward Transconductance	--	3.87	--	Ω	V <sub>DS</sub> =40V, I <sub>D</sub> =4.5A ④
C <sub>iss</sub>	Input Capacitance	--	500	650	pF	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1MHz <b>See Fig 5</b>
C <sub>oss</sub>	Output Capacitance	--	95	110		
C <sub>rss</sub>	Reverse Transfer Capacitance	--	45	55		
t <sub>d(on)</sub>	Turn-On Delay Time	--	13	40	ns	V <sub>DD</sub> =100V, I <sub>D</sub> =9A, R <sub>G</sub> =12Ω <b>See Fig 13</b> ④ ⑤
t <sub>r</sub>	Rise Time	--	13	40		
t <sub>d(off)</sub>	Turn-Off Delay Time	--	30	70		
t <sub>f</sub>	Fall Time	--	18	50		
Q <sub>g</sub>	Total Gate Charge	--	22	29	nC	V <sub>DS</sub> =160V, V <sub>GS</sub> =10V, I <sub>D</sub> =9A <b>See Fig 6 &amp; Fig 12</b> ④ ⑤
Q <sub>gs</sub>	Gate-Source Charge	--	4.3	--		
Q <sub>gd</sub>	Gate-Drain( "Miller" ) Charge	--	10.9	--		

### Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I <sub>S</sub>	Continuous Source Current	--	--	9	A	Integral reverse pn-diode in the MOSFET
I <sub>SM</sub>	Pulsed-Source Current ①	--	--	36		
V <sub>SD</sub>	Diode Forward Voltage ④	--	--	1.5	V	T <sub>J</sub> =25°C, I <sub>S</sub> =9A, V <sub>GS</sub> =0V
t <sub>rr</sub>	Reverse Recovery Time	--	137	--	ns	T <sub>J</sub> =25°C, I <sub>F</sub> =9A
Q <sub>rr</sub>	Reverse Recovery Charge	--	0.68	--	μC	dI <sub>F</sub> /dt=100A/μs ④

#### Notes ;

- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ② L=3mH, I<sub>AS</sub>=9A, V<sub>DD</sub>=50V, R<sub>G</sub>=27Ω, Starting T<sub>J</sub>=25°C
- ③ I<sub>SD</sub> ≤ 9A, di/dt ≤ 220A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub>=25°C
- ④ Pulse Test : Pulse Width = 250 μs, Duty Cycle ≤ 2%
- ⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

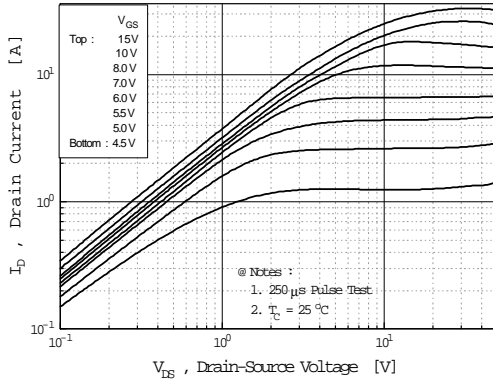


Fig 2. Transfer Characteristics

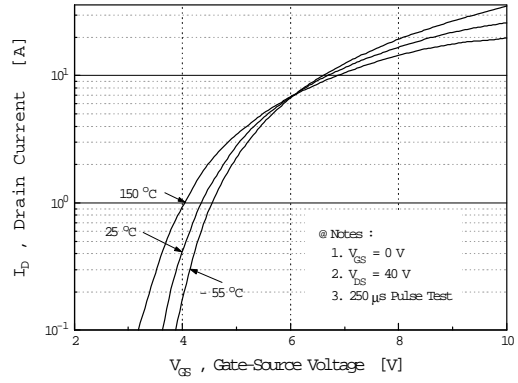


Fig 3. On-Resistance vs. Drain Current

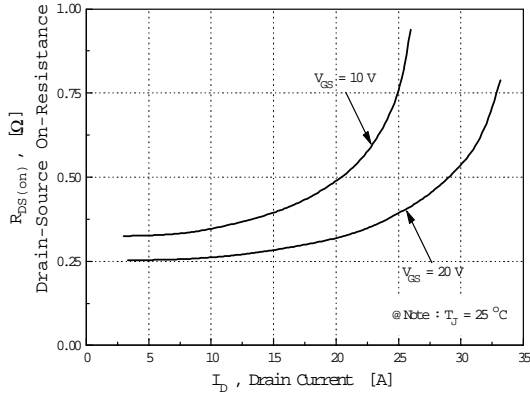


Fig 4. Source-Drain Diode Forward Voltage

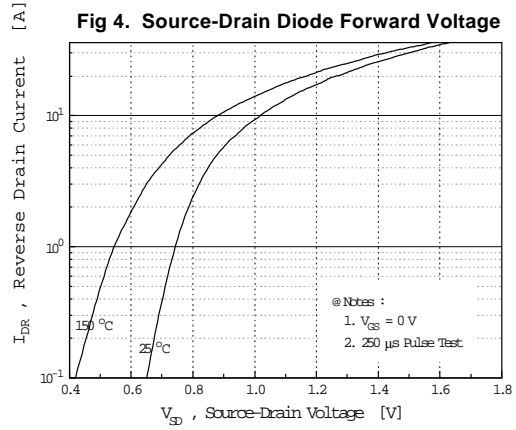


Fig 5. Capacitance vs. Drain-Source Voltage

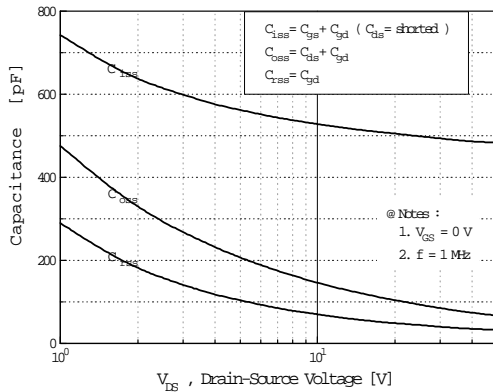
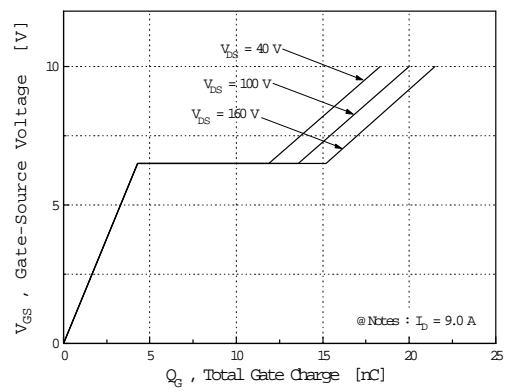


Fig 6. Gate Charge vs. Gate-Source Voltage



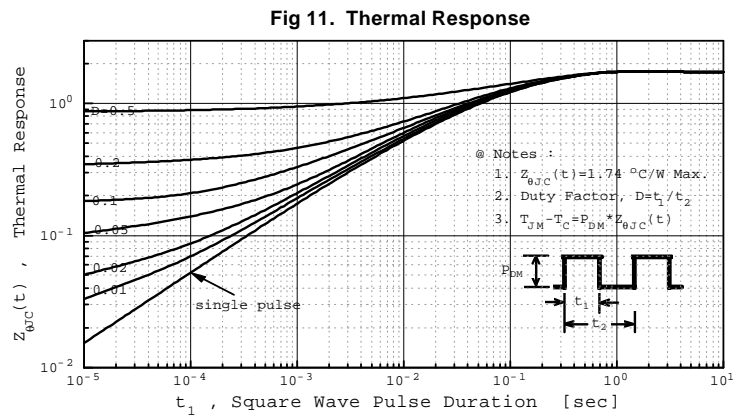
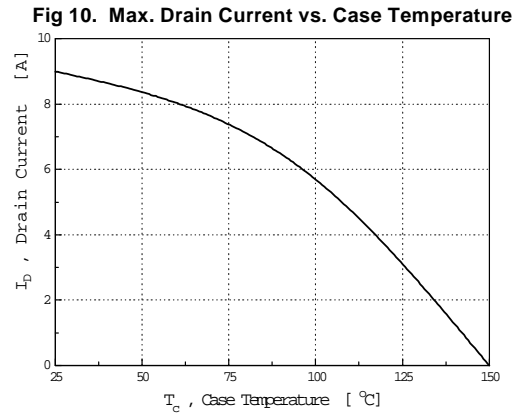
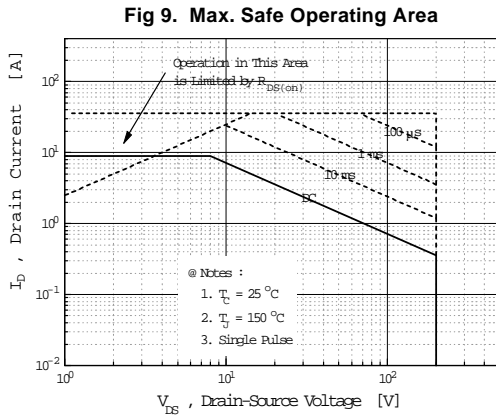
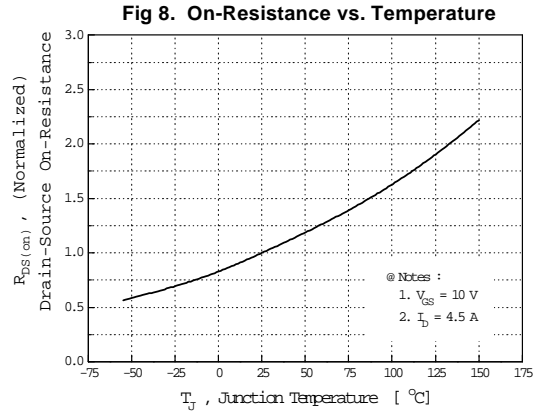
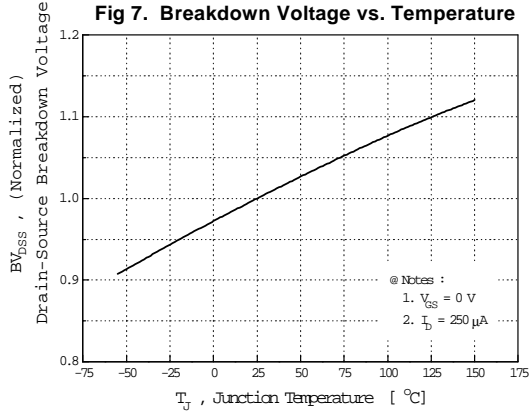


Fig 12. Gate Charge Test Circuit & Waveform

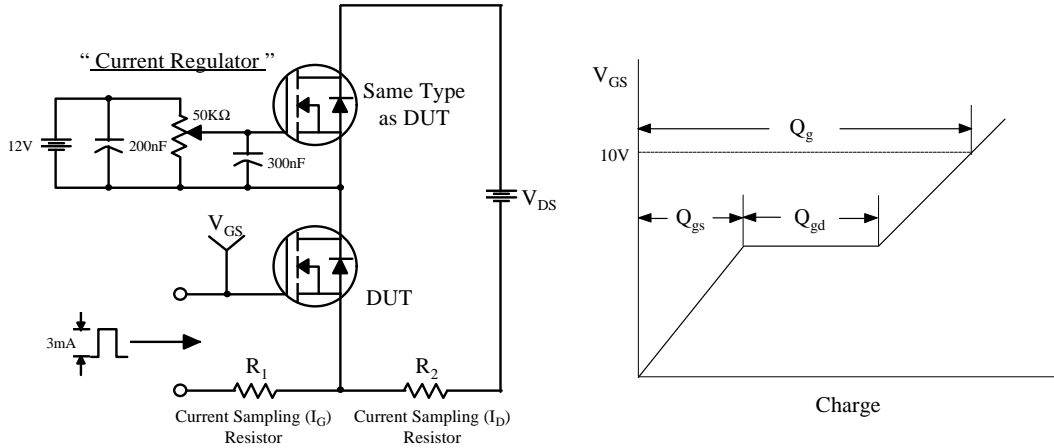


Fig 13. Resistive Switching Test Circuit & Waveforms

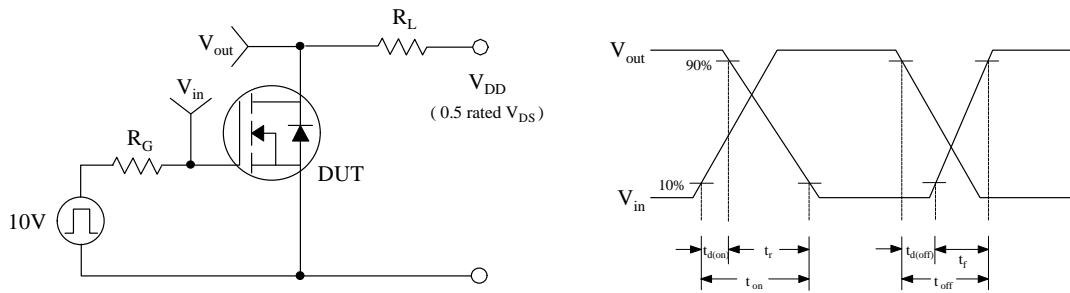


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

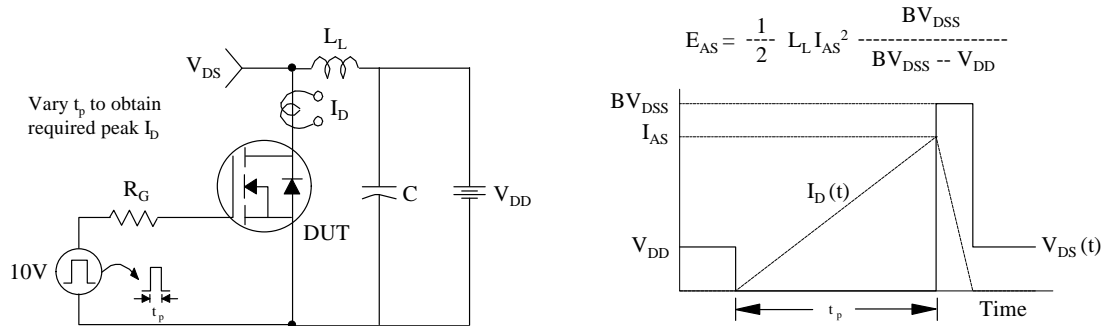
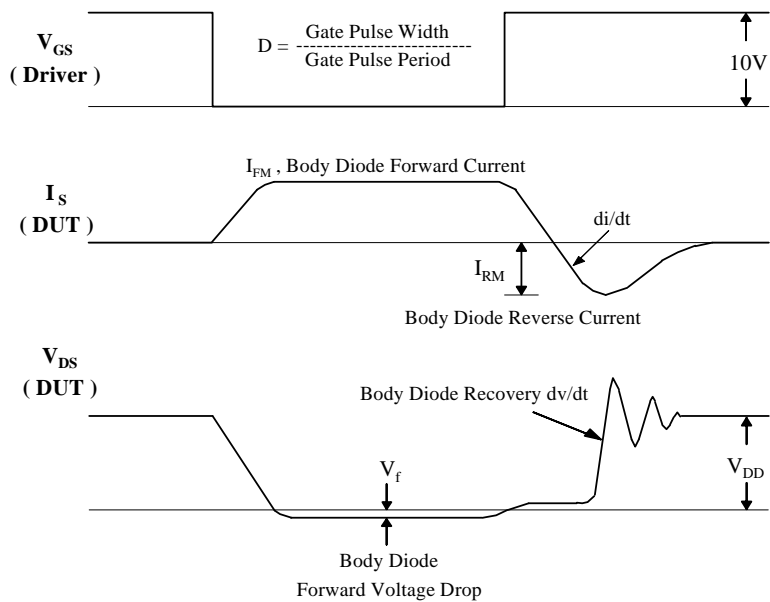
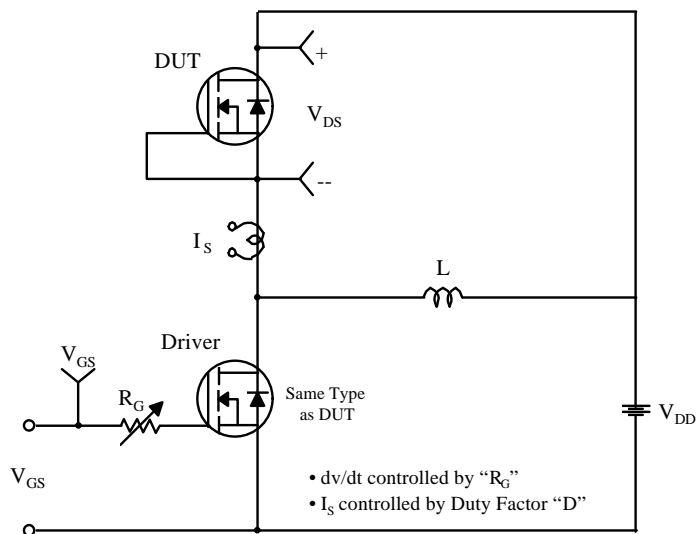


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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