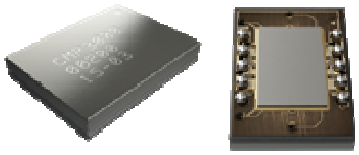
Doc.Nr. 82112900.A.02

Product Family Specification



CMR3000-D0X Series

3-axis gyro

TABLE OF CONTENTS

1 General Description

1.1 Introduction

CMR3000-D0X is a three axis gyroscope family targeted for high volume products requiring small size, low price and low power consumption. It consists of a 3D-MEMS sensing element and a signal conditioning ASIC in a wafer level package.

Block diagram of CMR3000-D0X is shown in Figure 1 below.

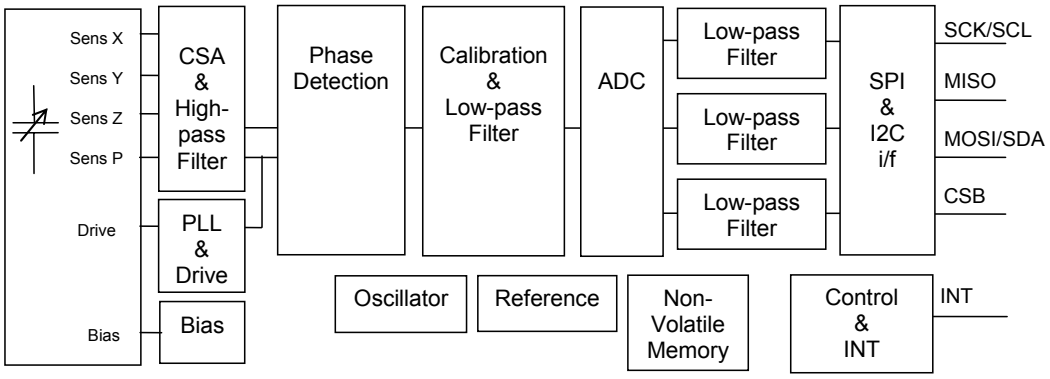


Figure 1. CMR3000-D0X block diagram with digital SPI and I^2C interface

This document, no. 82112900, describes the product specification (e.g. operation modes, user accessible registers, electrical properties and application information) for the CMR3000-D0X family. The specification for an individual sensor is available in the corresponding data sheet.

1.2 Functional Description

1.2.1 Sensing element

The sensing element is manufactured using proprietary bulk 3D-MEMS process, which enables robust, stable and low noise & power capacitive sensors.

The sensing element consists of a primary resonator and three secondary resonators. Primary resonator is driven by the ASIC and the Coriolis force will couple to the secondary resonators. Detected signal will be converted into a phase difference and then into a voltage in the signal conditioning ASIC.

1.2.2 Interface IC

CMR3000 includes an internal oscillator, reference and non-volatile memory that enable the sensor's autonomous operation within a system.

The sensing element is interfaced via drive circuitry, charge-sensitive-amplifiers (CSA) and phase detector used for XYZ-angular rate detection. Followed by calibration and filtering in analog domain, the signal is A/D-converted and then digitally filtered. Sensor output is user selectable digital SPI or I^2C interface.

Angular rate data can be read via the serial bus and in power down mode the device is in-active. Measurement bandwidth can be selected by register command.

1.2.3 Factory calibration

Sensors are factory calibrated. Trimmed parameters are sensitivity, offset, internal current & voltage references and frequency of the internal oscillator. Calibration parameters will be read automatically from the internal non-volatile memory during sensor startup.

1.2.4 Supported features

Supported features are listed in Table 1 below.

Table 1. CMR3000-D0X devices' summary.

Features	CMR3000-D01
Supply voltage	2.5 V – 3.6 V
I/O voltage	1.6 V – 3.6 V
Measuring range	2000 dps
Resolution	0.75 dps
Sensitivity	1.33 count/dps
Interface	SPI max 500 kHz, I^2C fast mode 400 kHz
Clock	Internal

1.2.5 Operation modes

1.2.5.1 Power Down

In Power Down (PD) mode device's volatile registers keep their contents and the current consumption is minimized. Power down mode is the default mode after start up.

1.2.5.2 Stand By

Stand By (SB) mode can be used to start-up the sensor quickly. In SB mode only the primary resonator loop is on with reduced bias current while the other blocks are off.

1.2.5.3 Measurement

In Measurement mode (Meas) the sensor offers angular rate information via the digital SPI/I^2C interface. Interrupt can be activated via INT-pin, when each xyz-angular rate sample is ready to be read.

Measurement bandwidth can be selected through register command.

1.2.6 Interrupt

The CMR3000 has a dedicated output pin (INT) to be used as the interrupt for the master controller. Interrupt conditions can be activated and deactivated via the SPI or I^2C bus.

1.2.7 Operational flow chart

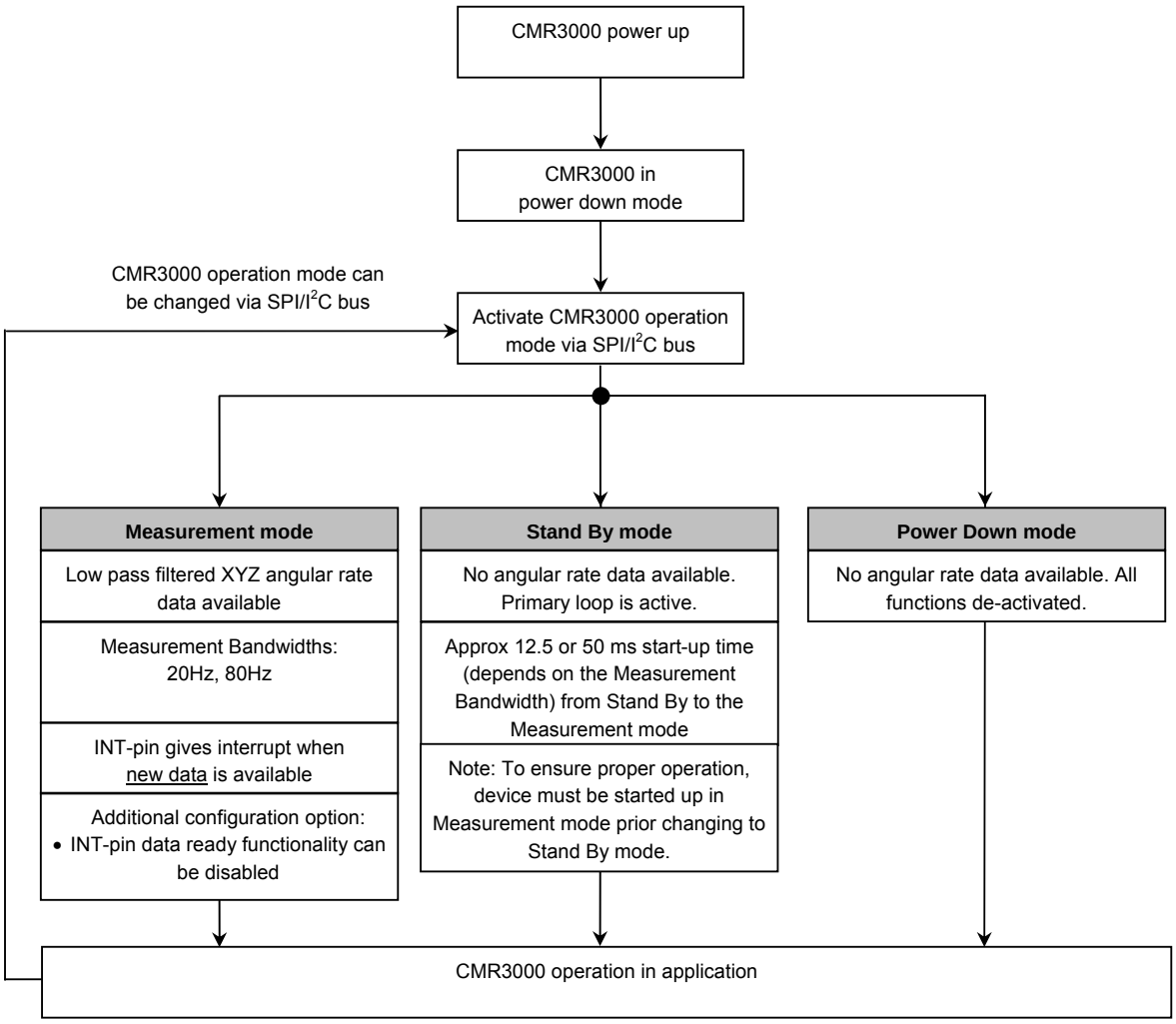


Figure 2. CMR3000 operational flow chart.

2 Reset and power up, Operation Modes, HW functions and Clock

2.1 Reset and power up

The CMR3000 has internal power-on reset circuit. It releases the internal reset-signal once the power supplies will be within the specified range. After releasing the internal reset, the CMR3000 will read configuration and calibration data from the non-volatile memory to volatile registers. Then the CMR3000 will make parity check to the read memory content. The STATUS register's PERR-bit="0" shows successful memory read operation.

Device can be externally reset by writing RESET=1b to CTRL register and then waiting 2 ms for reset to complete.

2.2 Power Down mode

The CMR3000-D0X enters the power down mode by default after power-on reset and initialization of the volatile registers. PD can also be set by writing MODE[1:0] = 00b to CTRL register.

Output registers will keep their content in the power down mode.

2.3 Measurement Mode

2.3.1 Description

The CMR3000-D0X is set to a measurement mode by writing MODE[1:0] = 1Xb to CTRL register. Data will be reliable in the output registers after the product specific turn-on time.

Sample rate is 2000 Hz. The measurement bandwidth is 80 Hz (MODE[1:0] = 11b) or 20 Hz (MODE[1:0] = 10b).

INT-pin gives an interrupt by default when new data is available.

2.3.2 Usage

Angular rate data can be read from data output registers X_LSB, X_MSB, Y_LSB, Y_MSB, Z_LSB and Z_MSB. See section 2.5 for INT-pin configuration details.

2.4 Stand By Mode

The CMR3000-D0X is set to Stand By mode by writing MODE[1:0] = 01b to CTRL register. No measurement data will be available in the output registers.

As the startup-up time from Stand By to Measurement mode is much faster than from Power Down to Measurement mode, Stand By mode can be used to optimize system level power consumption. Due to operation principle, Stand By mode must be preceded by starting up the device in Measurement mode.

2.5 Interrupt function (INT-pin)

Interrupt polarity (active high/low) can be configured with CTRL register's INT_LEVEL bit.

INT pin is automatically cleared by reading the angular rate output data. INT-pin data ready functionality can be disabled by setting the CTRL register's INT_DIS bit. See section 3.3 for CTRL and INT_STATUS register details.

2.6 Clock

The CMR3000 has an internal factory trimmed oscillator and clock generator.

3 Addressing Space

The CMR3000 register contents and bit definitions are described in more detail in the following sections.

3.1 Register Description

The CMR3000 addressing space is presented in Table 2 below.

Table 2. List of registers

Address	Name	Description	Mode (R, RW, NV)	Reg. type
00h	**WHO_AM_I**	Identification register	**R**	Output
01h	**REVID**	ASIC revision ID, fixed in metal	**R**	Output
02h	**CTRL**	Configuration (POR, operation modes)	**RW**	Conf
03h	**STATUS**	Status (POR, EEPROM parity)	**R**	Output
04h-08h		Reserved		
0Ch	**X_LSB**	Angular rate X LSB	**R**	Output
0Dh	**X_MSB**	Angular rate X MSB	**R**	Output
0Eh	**Y_LSB**	Angular rate Y LSB	**R**	Output
0Fh	**Y_MSB**	Angular rate Y MSB	**R**	Output
10h	**Z_LSB**	Angular rate Z LSB	**R**	Output
11h	**Z_MSB**	Angular rate Z MSB	**R**	Output
12h-21h		Reserved		
22h	**I2C_ADDR**	I^2C device address	**RW**	Conf
23h-25h		Reserved		
26h	**PDR**	Product data register	**R**	output
27h-3Fh		Reserved		

Address is the register address in hex format.
RW – Read / Write register, R – Read-only register, NV – non-volatile register content.

3.2 Non-volatile memory

The CMR3000 has an internal non-volatile memory for calibration and configuration data. Memory content will be programmed during production and is not user configurable. Initial configuration values mirrored to volatile registers after reset can be found in the following section 3.3.

3.3 Registers

Address: **00h**
Register name: **WHO_AM_I**, Identification register

Bits	Mode	Initial Value	Name	Description
7	R	0		Reserved
6:0	R	xxh		Identification register

Address: **01h**
Register name: **REVID**, ASIC revision ID

Bits	Mode	Initial Value	Name	Description
7:4	R	1h	REVMAJ	Major revision number
3:0	R	0h	REVMIN	Minor revision number (metal mask change)

Address: **02h**
Register name: **CTRL**, Control register

Bits	Mode	Initial Value	Name	Description
7	RW	0	RESET	1 – device in reset stage 0 – reset cleared
6	RW	0	INT_LEVEL	0 – Interrupt is active when INT pin is set to logic high 1 – Interrupt is active when INT pin is set to logic low
5		0		reserved
4	RW	0	I2C_DIS	0 – I^2C interface enabled 1 – I^2C interface disabled. See section 4.1.3 for details.
3		0		Reserved. Write '0'.
2:1	RW	0	MODE[1:0]	00 – Power down mode, default mode. 01 – Stand by mode TBD 10 – Measurement mode, BW=20 Hz. 11 – Measurement mode, BW=80 Hz.
0	RW	0	INT_DIS	0 – Interrupt enabled: data ready 1 – Interrupts disabled

Note that after changing MODE bits it may take some time to recover the target operating state.

Address: **03h**
Register name: **STATUS**, Status register

Bits	Mode	Initial Value	Name	Description
7:4		0h		Reserved
3	R	0	PORST	1 means Power-on-Reset state. Reading the register sets always bit to 0.
2:1		0h		Reserved
0	R	0	PERR	0 – No EEPROM Parity Error 1 – EEPROM Parity Error. Reading this register sets bit to '0'

Address: **0Ch**
Register name: **X_LSB**, X-channel LSB output register

Bits	Mode	Initial Value	Name	Description
7:0	R	0h	X_LSB	See SPI data frame description for more info.

Address: **0Dh**
Register name: **X_MSB**, X-channel MSB output register

Bits	Mode	Initial Value	Name	Description
7:0	R	0h	X_MSB	See SPI data frame description for more info.

Address: **0Eh**
Register name: **Y_LSB**, Y-channel LSB output register

Bits	Mode	Initial Value	Name	Description
7:0	R	0h	Y_LSB	See SPI data frame description for more info.

Address: **0Fh**
Register name: **Y_MSB**, Y-channel MSB output register

Bits	Mode	Initial Value	Name	Description
7:0	R	0h	Y_MSB	See SPI data frame description for more info.

Address: **10h**
Register name: **Z_LSB**, Z-channel LSB output register

Bits	Mode	Initial Value	Name	Description
7:0	R	0h	Z_LSB	See SPI data frame description for more info.

Address: **11h**
Register name: **Z_MSB**, Z-channel MSB output register

Bits	Mode	Initial Value	Name	Description
7:0	R	0h	Z_MSB	See SPI data frame description for more info.

The bit level description for angular rate data from X_LSB…Z_MSB registers is presented in Table 3 below. The acceleration data is presented in 2's complement format. At 0 dps rate the output is ideally 0h.

Table 3. Bit level description in [dps] for angular rate registers of CMR3000-D01.

MSB								LSB							
B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0
x	x	s	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	x
x	x	+/-	1536	768	384	192	96	48	24	12	6	3	1.5	0.75	0.375

s = sign bit
x= don't care

Address: **22h**
Register name: **I2C_ADDR**, Device address for I^2C bus

Bits	Mode	Initial Value	Name	Description
7:6		0		Reserved
5:0	RW	0Fh	ADDR[6:1]	6 MSB bits of the 7-bit device address for I^2C bus. LSB bit of the I^2C address ADDR[0] is according to MISO pin state. I.e. I^2C address can be selected between 1Eh and 1Fh. Register content is non-volatile.

Address: **26h**
Register name: **PDR**, Product data register

Bits	Mode	Initial Value	Name	Description
7:0	R		PDR[7:0]	Linearization parameters

4 Serial Interfaces

Communication between the CMR3000 sensor and master controller is based on serial data transfer and a dedicated interrupt line (INT-pin). Two different serial interfaces are available for the CMR3000 sensor: SPI and I^2C (Phillips specification V2.1). Selection between these two interfaces is done using the chip select signal. The I^2C interface can be also disabled by re-configuring register content. The CMR3000 acts as a slave on both the SPI and I^2C bus.

4.1 SPI Interface

SPI bus is a full duplex synchronous 4-wire serial interface. It consists of one master device and one or more slave devices. The master is defined as a micro controller providing the SPI clock, and the slave as any integrated circuit receiving the SPI clock from the master. The CMR3000 sensor always operates as a slave device in master-slave operation mode. A typical SPI connection is presented in Figure 3.

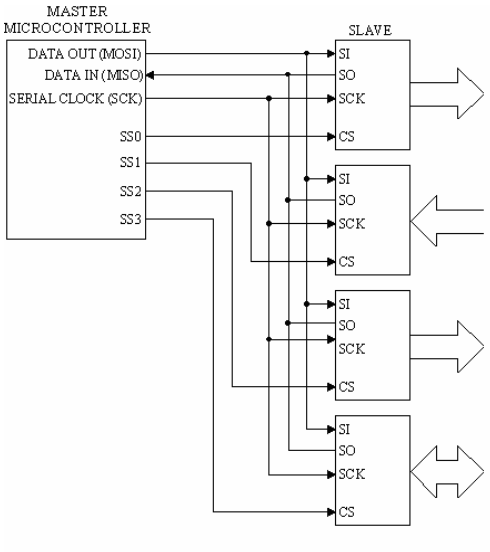


Figure 3. Typical SPI connection

The data transfer uses the following 4-wire interface:

MOSI	master out slave in	µC → CMR3000
MISO	master in slave out	CMR3000 → µC
SCK	serial clock	µC → CMR3000
CSB	chip select (low active)	µC → CMR3000

4.1.1 SPI frame format

CMR3000 SPI frame format and transfer protocol is presented in Figure 4 below.

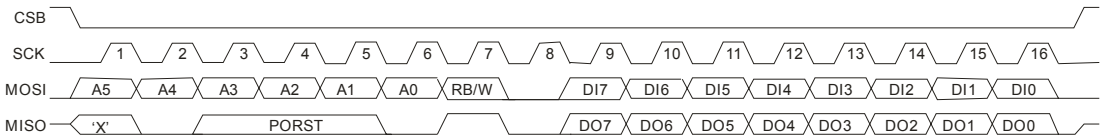


Figure 4. SPI frame format

Each communication frame contains 16 bits. The first 8 bits in MOSI line contain info about the register address being accessed and the operation (read/write). The first 6 bits define the 6 bit

address for the selected operation, which is defined by bit 7 (‘0’ = read ‘1’ = write), which is followed by one zero bit. The later 8 bits in the MOSI line contain data for a write operation and are ‘don’t-care’ for a read operation. CMR3000 samples bits in from MOSI line on the rising edge of SCK and bits out to MISO line on falling edge of SCK.

The first bits in MISO line are not defined bit (bit 1), fixed zero bit (bit 2), power reset status (bits 3-5), fixed zero bit (bit6), fixed one bit (bit7) and fixed zero bit (bit8). The later 8 bits contain data for a read operation. During the write operation, these data bits are zero.

For write commands, data is written into the addressed register on the falling edge of 16th SCK pulse.

For read commands, data is latched into the internal SPI output register (shift register) on the 8th rising edge of SCK. The output register is shifted out MSB first over MISO output.

When the CSB is high state between data transfers, the MISO line is in the high-impedance state.

Multiple read operation mode (decrement reading) is supported for angular rate output data registers (0Ch...11h). Reading can be started from any of these registers and address is reduced by one continuously. From register address 0Ch the address jumps to 11h.

4.1.2 Examples of SPI communication

4.1.2.1 Example of register read

An example of Z-axis angular read command is presented in Figure 5. The master gives the register address to be read via the MOSI line: '11' in hex format and '010001' in binary format, register name is Z_MSB. 7th bit is set to '0' to indicate the read operation.

The sensor replies to a requested operation by transferring the register content via MISO line. After transferring the asked Z_MSB register content, the master gives next register address to be read: '10' in hex format and '010000' in binary format, register name is Z_LSB. The sensor replies to the requested operation by transferring the register content MSB first.

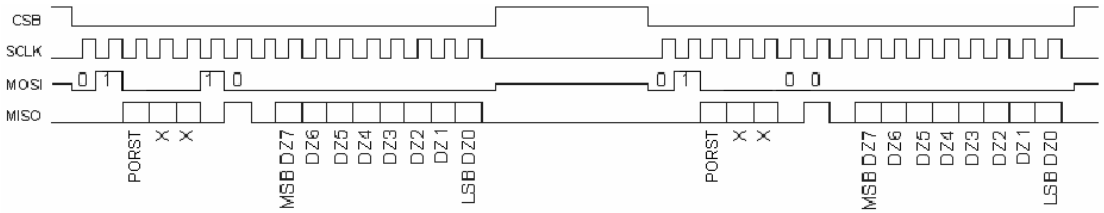


Figure 5. An example of SPI read communication.

4.1.3 Multiple slave devices in SPI bus

Since both SPI and I^{2}C interfaces are enabled by default, certain precautions should be taken care of when the CMR3000 is connected to a SPI bus with multiple slave devices. In case of multiple devices on same SPI bus, it's important to prevent MOSI_SDA pin changes during SCK_SCL pin high state. If the MOSI_SDA pin state is changed when the SCK_SCL pin is in high state, the I^{2}C transmission is engaged, see Figure 6 below.

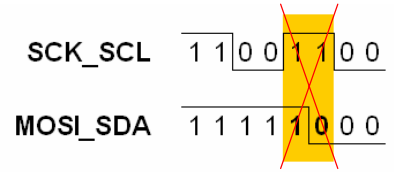


Figure 6. MOSI_SDA pin change during SCK_SCL high state engages I²C transmission.

In cases with multiple slaves in SPI bus it is recommended that I2C transmission is disabled by setting I2C_DIS bit to '1' in CRTL register. After CMR3000 start up the I2C_DIS bit is always 0 (I²C transmission enabled).

4.1.4 Output register data refresh

When the CSB is pulled '0', the latest data is available in the output registers. Output register data refresh is enabled only when CSB is '1'.

4.2 I²C Interface

I²C is a 2-wire serial interface. It consists of one master device and one or more slave devices. The master is defined as a micro controller providing the serial clock (SCL), and the slave as any integrated circuit receiving the SCL clock from the master. The CMR3000 sensor always operates as a slave device in master-slave operation mode. When using an SPI interface, a hardware addressing is used (slaves have dedicated CSB signals), the I²C interface uses a software based addressing (slave devices have dedicated bit patterns as addresses). The default I²C device address for CMR3000 is 1Eh or 1Fh (pre-programmed during CMR3000 production). LSB bit of the I2C address is according to MISO pin state.

The CMR3000 is compatible to the Philips I²C specification V2.1. Main used features of the I²C interface are:

- 7-bit addressing, CMR3000 I²C device address is TBD
- Supports standard mode and fast mode
- Start / Restart / Stop
- Slave transceiver mode
- Designed for low power consumption
- Multiple read operation mode (decrement reading)
    - reading of any register decrements data address by one even if only one register is read
    - from register address 0Ch address jumps to 11h

4.2.1 I²C frame format

4.2.1.1 I²C write mode

In I²C write mode, the first 8 bits after device address define the CMR3000 internal register address to be written.

4.2.1.2 I²C read mode

The read mode operates as described in Philips I²C specification. I²C read operation returns the content of the register which address is defined in I2C read frame. Read data is acknowledged by I²C master.

4.2.2 Examples of I²C communication

Examples of I²C communication are presented below in **Error! Reference source not found.**. Address byte includes 7 device address bits (1E=0011110b) followed by the R/W bit.

CASE 1: I2C 8 bit read from register X_MSB

S	device addr byte **0011110**	0	SA	register address byte **00010001**	SA	RS	device addr byte **0011110**	1	SA	register data MSB first	MA	E

CASE 2: I2C 8 bit write to register CTRL

S	device addr byte **0011110**	0	SA	register address byte **00000010**	SA	register data to write MSB first	SA	E

S = Start condition
RS = Repeated Start Condition
E = End condition
SA = Slave acknowledgement
MA = Master acknowledgement

Figure 7. I²C format

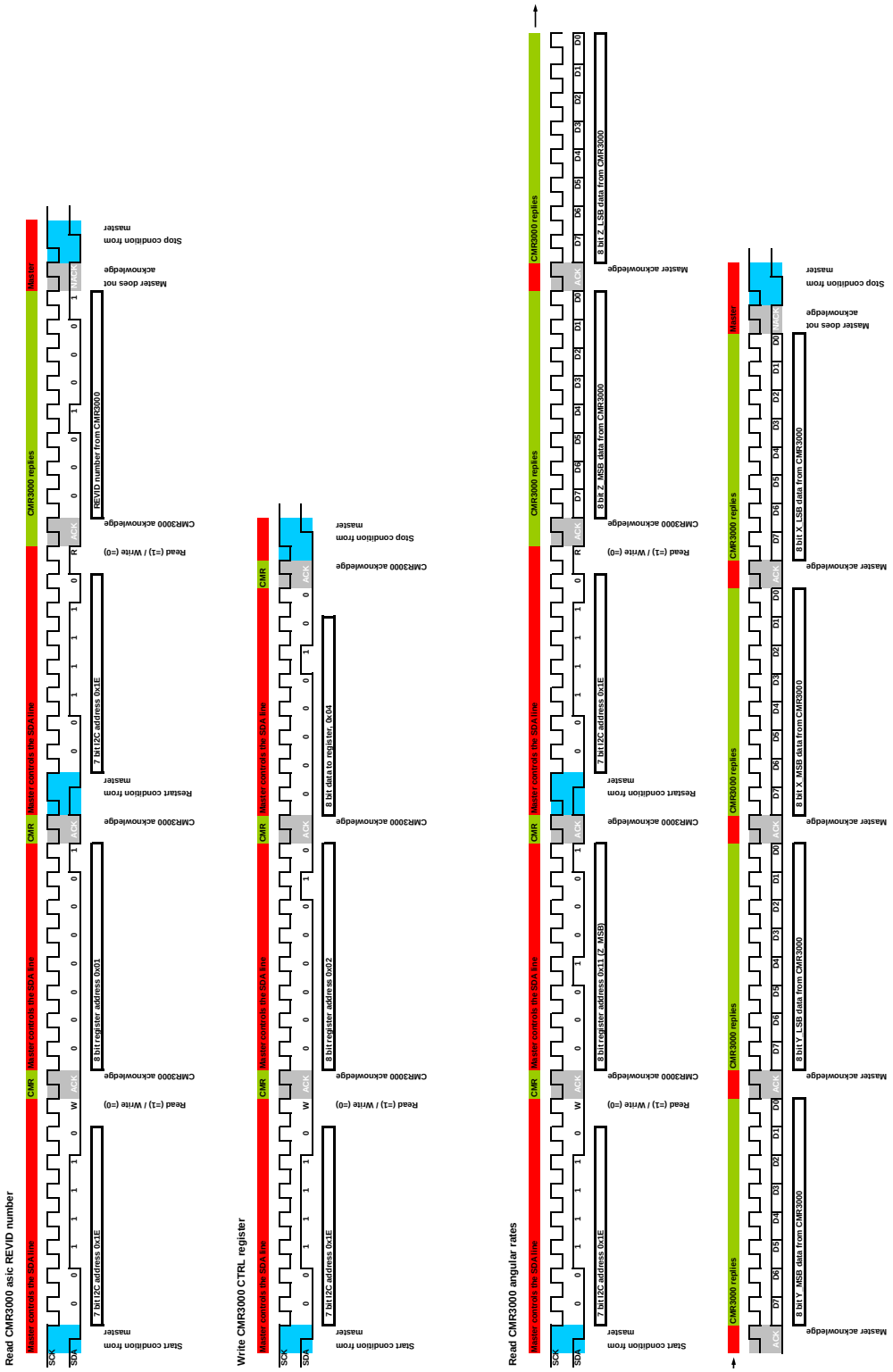


Figure **8** Bit level I2C format description

4.2.3 Output register data refresh

Angular rate output registers are refreshed when the address of the output register is written. Use decrement reading to ensure XYZ data from the same moment.

4.2.4 Electrical Characteristics

All voltages are reference to ground. Currents flowing into the circuit have positive values.

4.3 Absolute maximum ratings

The absolute maximum ratings of the CMR3000 are presented in Table 4 below.

Table 4. Absolute maximum ratings of the CMR3000

Parameter	Value	Unit
Supply voltage (V_{dd}, DVIO)	-0.3 to +3.6	V
Voltage at input / output pins	-0.3 to (V_{dd} + 0.3)	V
ESD (Human body model)	±2	kV
Storage temperature	-40 ... +125	°C
Storage / operating temperature	-40 ... +85	°C
Mechanical shock *	< 10 000	g
Exposure to ultrasonic energy (e.g. ultra sonic washing or welding)	Not allowed	

* 1 m drop on concrete may cause >>10000 g shock.

4.4 Power Supply

Please refer to the corresponding product datasheet.

4.5 Digital I/O Specification

4.5.1 Digital I/O DC characteristics

Table 5. DC characteristics of digital I/O pins.

No.	Parameter	Conditions	Symbol	Min	Typ	Max	Unit
CSB with pull up SCK and MOSI (I^2C disabled) with pull down SDA and SCL without pull up							
2	Pull up/down resistor		R_{PUD}		160		kΩ
2a.	Input Leakage	V_{IN} = DVIO	I_{IN}	TBD		TBD	µA
3	Input high voltage		V_{IH}	0.7*Dvio			V
4	Input low voltage		V_{IL}			0.3*Dvio	V
5	Hysteresis		V_{HYST}	0.1*Dvio			V
Output terminal: MISO, SDA, INT							
7	Output high voltage	I > -1 mA	V_{OH}	0.7*Dvio		Dvio	V
8	Output low voltage	I < 1 mA	V_{OL}	0		0.3*Dvio	V
9	Tristate leakage	0 < V_{MISO} < DVIO	I_{LEAK}	-0.5		0.5	µA

4.5.2 Digital I/O level shifter

All the CMR3000 products have an internal level shifter that can be used to interface e.g. a micro controller using lower supply than the CMR3000. The level shifter is "programmed" by providing the supply voltage of the interfaced device to the DVIO-pin. Please refer to the corresponding product data sheet for details.

4.5.3 SPI AC characteristics

The AC characteristics of the CMR3000 SPI interface are defined in Figure 9 and in Table 6.

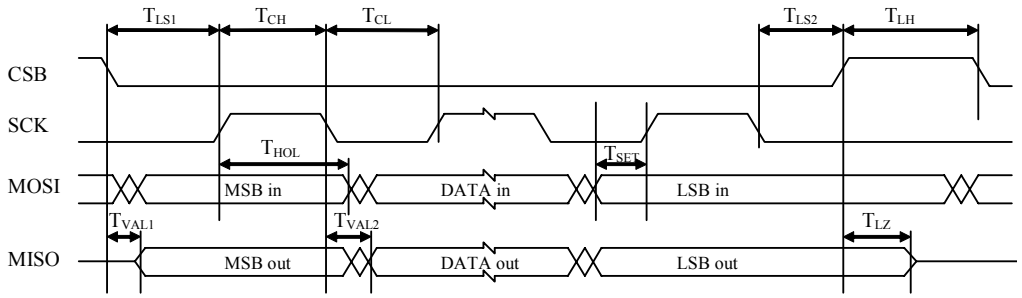


Figure 9. Timing diagram for SPI communication.

Table 6. AC characteristics of SPI communication.

No.	Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Terminal CSB, SCK							
1	Time from CSB (10%) to SCK (90%) [1]		T_{LS1}	$T_{per}/2$			ns
2	Time from SCK (10%) to CSB (90%) [1]		T_{LS2}	$T_{per}/2$			ns
3	Time from CSB (90%) to SCK (90%)		T_{LS3}	$T_{per}/4$			ns
4	Time from SCK (10%) to CSB (10%)		T_{LS4}	$T_{per}/4$			ns
Terminal SCK							
5	SCK low time	C_L at MISO < 50 pF	T_{CL}	0.8* $T_{per}/2$	$T_{per}/2$		ns
6	SCK high time	C_L at MISO < 50 pF	T_{CH}	0.8* $T_{per}/2$	$T_{per}/2$		ns
7	SCK Frequency		fsck = $1/T_{per}$			0.5	MHz
Terminal MOSI, SCK							
8	Time from changing MOSI (10%, 90%) to SCK (90%) Data setup time		T_{SET}	$T_{per}/4$			ns
9	Time from SCK (90%) to changing MOSI (10%, 90%) Data hold time		T_{HOL}	$T_{per}/4$			ns
Terminal MISO, CSB							
10	Time from CSB (10%) to stable MISO (10%, 90%)	C_L at MISO < 50 pF	T_{VAL1}			$T_{per}/4$	ns
11	Time from CSB (90%) to high impedance state of MISO [1].	C_L at MISO < 50 pF	T_{LZ}			$T_{per}/4$	ns
Terminal MISO, SCK							
12	Time from SCK (10%) to stable MISO (10%, 90%) [1].	C_L at MISO < 50 pF	T_{VAL2}			1.3*$T_{per}/4$	ns
Terminal MISO, CSB							
13	Time between SPI cycles, CSB at high level (90%)		T_{LH}	12			µs

[1] T_{per} is SCK period

4.5.4 I²C AC characteristics

Please, see Phillips Semiconductors, The I²C bus specification, Version 2.1, January 2000, pp. 31-33.

5 Package Characteristics

5.1 Dimensions

The package dimensions are presented in Figure 10 below (dimensions in millimeters [mm]).

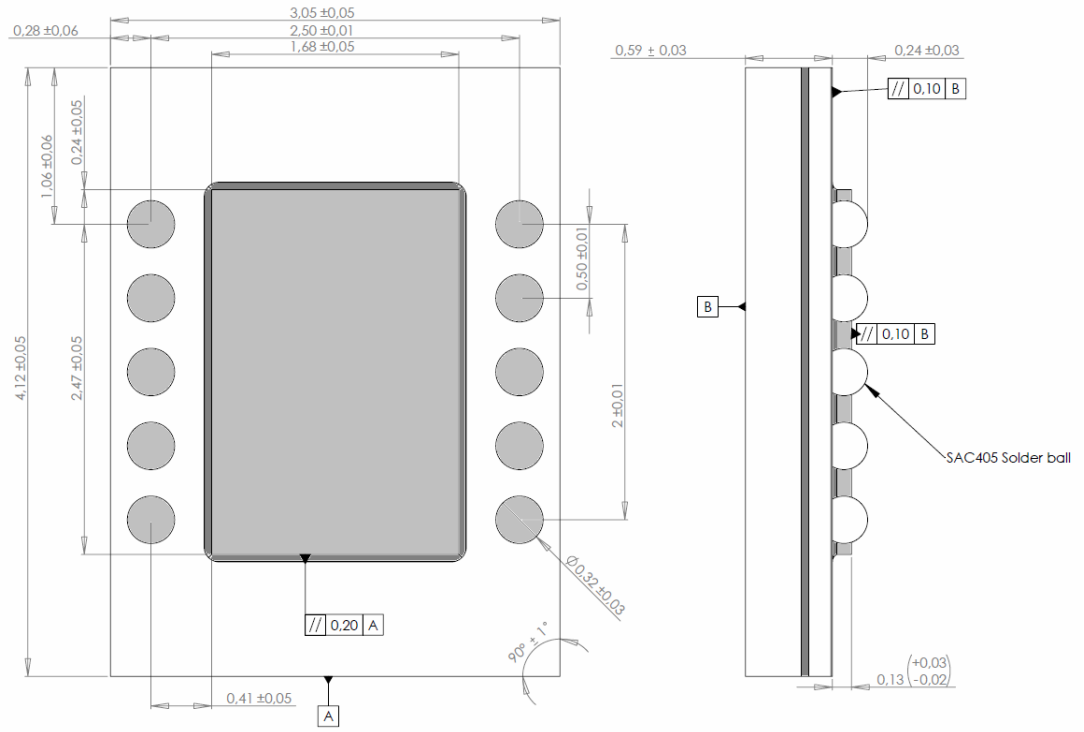


Figure 10. Package dimensions in mm for reference only. Please check the corresponding data sheet for details.

6 Application information

6.1 Pin Description

CMR3000 pin numbers are presented in Figure 12 below and pin descriptions in Table 7.

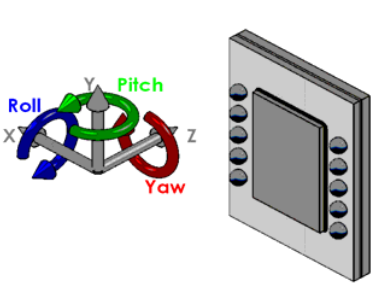


Figure 11. CMR3000 sensing directions

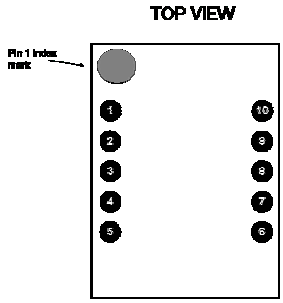


Figure 12. CMR3000 pin numbers

Table 7. CMR3000 pin descriptions

Pin #	Name	CMR3000-D01
1	DVSS	Digital ground
2	INT	Interrupt
3	MOSI_SDA	SPI Serial Data Input (MOSI) / I^2C Serial Data (SDA)
4	CSB	Chip select / I^2C enable
5	AVSS	Analog ground
6	AVDD	Analog supply voltage
7	SCK_SCL	SPI Serial Clock (SCK) / I^2C Serial Clock (SCL)
8	MISO	SPI Serial Data Output (MISO) / I2C slave address LSB ADDR[0]
9	DVIO	I/O Supply
10	DVDD	Digital supply voltage

6.2 Recommended circuit diagram

1. Connect 100 nF SMD capacitor between each supply voltage and ground level.
2. Use separate regulator for digital IO supply (DVIO).
3. Serial interface (SPI or I^2C) logical '1' level is determined by DVIO supply voltage level.

Recommended circuit diagrams for the CMR3000 are presented in Figure 13 below.

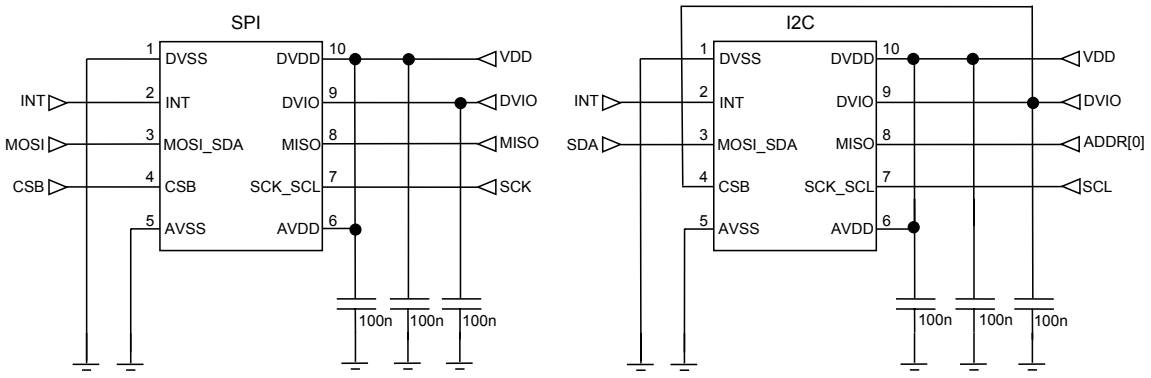


Figure 13 Recommended circuit diagrams for CMR3000-D0X

6.3 Recommended PWB layout

General PWB layout recommendations for CMR3000 products (refer to Figure 13 and Figure 14):

1. Locate 100 nF SMD capacitors right next to the CMR3000 package
2. Ensure low impedance by maximizing the ground plane under the component.

Recommended PWB pad layout for CMR3000 is presented in Figure 14 below (dimensions in micrometers, [µm]).

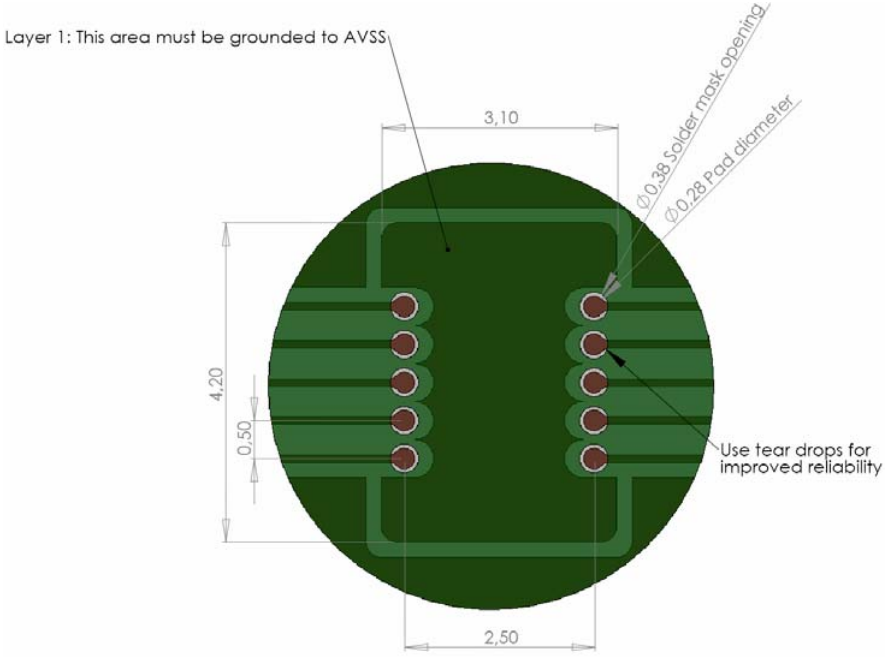


Figure 14. Recommended PWB pad layout for CMR3000.

Recommended PWB layout for the CMR3000-D0X is presented in Figure 15 below (circuit diagram presented in Figure 13 above).

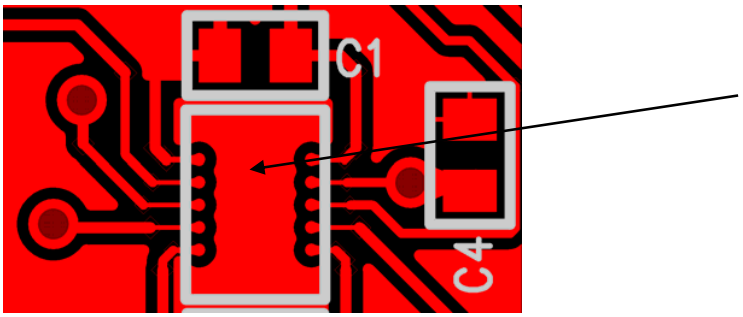


Figure 15. Recommended PWB layout for CMR3000-D0X with SPI interface (not actual size, for reference only).

6.4 Mounting recommendations

For the best sensor stability mechanical stresses due to mounting should be minimized. Potential causes of mechanical stress to be avoided are

- Contact with other structures due to too small mechanical tolerances.
- Placement under or next to mechanical push button contacts.
- Locations near hot spots (micro controller, power amplifier etc) due to temperature effects.
- Mounting close to PWB attachment point e.g. screw or snap.
- PWB areas that can bend or vibrate.
- The use of under fill or coating. Please note that under fill or coating the neighboring component should not be in contact with the sensor.

Due to sampled signal conditioning strong magnetic or electric fields may cause noise in the sensor output. Therefore mounting near strong magnetic or electric fields is not recommended.

6.5 Assembly instructions

The Moisture Sensitivity Level (MSL) of the CMR3000 component is 2 according to the IPC/JEDEC J-STD-020D. Please refer to the document TN81_CMR3000_Assembly_Instructions for more detailed information about CMR3000 assembly.

6.6 Tape and reel specifications

Please refer to the document TN81_CMR3000_Assembly_Instructions for tape and reel specifications.

7 Data sheet references

7.1 Offset

CMR3000's offset will be calibrated in $\Omega_X = \Omega_Y = \Omega_Z = 0$ dps.

7.1.1 Offset calibration error

Offset calibration error is the difference between the sensor's actual output reading and the nominal output reading in calibration conditions. Error is calculated by

Equation 1

$$Offset_{X-axisCalibEr} = \frac{Output_{X-axis} - Output}{Sens},$$

where $\mathrm{Output}_{\mathrm{X\text{-}axisCalibEr}}$ is sensor's X-axis calibration error in [dps], $\mathrm{Output}_{\mathrm{X\text{-}axis}}$ is sensor's X-axis output reading [counts], Output is sensor's nominal output in 0 dps angular rate and Sens sensor's nominal sensitivity [counts/dps].

7.1.2 Offset temperature error

Offset temperature error is the difference between the sensor's output reading in different temperatures and the sensor's calibrated offset value at room temperature. Error is calculated by

Equation 2

$$Offset_{X-axisTempEr@T} = \frac{Output_{X-axis@T} - Output_{X-axis@RT}}{Sens},$$

where $\mathrm{Output}_{\mathrm{X\text{-}axisTempEr@T}}$ is sensor's X-axis temperature error in [dps] in temperature T, $\mathrm{Output}_{\mathrm{X\text{-}axis@T}}$ is sensor's X-axis output reading [counts] in temperature T, $\mathrm{Output}_{\mathrm{X\text{-}axis@T}}$ X-axis output reading [counts] at room temperature RT and Sens sensor's nominal sensitivity [counts/g]. Sensor's angular rate is 0 dps for every measurement point.

7.2 Sensitivity

During the sensitivity calibration, sensor is rotated in sensing directions (Figure 11) at ±Ω dps rate.

Sensitivity is calculated by

Equation 3

$$Sens_{Y-axis} = \frac{Output_{Y-axis@+\Omega} - Output_{Y-axis@-\Omega}}{2\Omega},$$

where $\mathrm{Sens}_{\mathrm{Y\text{-}axis}}$ is sensor's Y-axis sensitivity in [counts/dps], $\mathrm{Output}_{\mathrm{Y\text{-}axis@+\Omega}}$ sensor's Y-axis output reading [counts] in +Ω dps angular rate and $\mathrm{Output}_{\mathrm{Y\text{-}axis@\text{-}\Omega}}$ is sensor's Y-axis output reading [counts] in -Ω dps angular rate.

7.2.1 Sensitivity calibration error

Sensitivity calibration error is the difference between sensor's measured sensitivity and the nominal sensitivity at room temperature conditions. Error is calculated by

Equation 4

$$Sens_{Y-axisCalibEr} = \frac{Sens_{Y-axis} - Sens}{Sens} \cdot 100\%,$$

where $Sens_{Y\text{-}axisCalibEr}$ is sensor's Y-axis sensitivity calibration error in [%], $Sens_{Y\text{-}axis}$ sensor's Y-axis sensitivity [counts/dps] at room temperature conditions and $Sens$ is sensor's nominal sensitivity [counts/dps].

7.2.2 Sensitivity temperature error

Sensitivity temperature error is the difference between sensor's sensitivity at different temperatures and the calibrated sensitivity. Error is calculated by

Equation 5

$$Sens_{Y-axisTempEr@T} = \frac{Sens_{Y-axis@T} - Sens_{Y-axis@RT}}{Sens_{Y-axis@RT}} \cdot 100\% ,$$

where $Sens_{Y\text{-}axisTempEr@T}$ is sensor's Y-axis sensitivity temperature error in [%] in temperature T, $Sens_{Y\text{-}axis@T}$ is sensor's measured Y-axis sensitivity [counts/dps] at temperature T and $Sens_{Y\text{-}axis@RT}$ is sensor's measured Y-axis sensitivity [counts/dps] at room temperature RT.

7.3 Linearity

During linearity measurement sensor is rotated in sensing directions and the rate is swept between ±FS.

Linearity error is the deviation from the best bit straight line. See Figure 16.

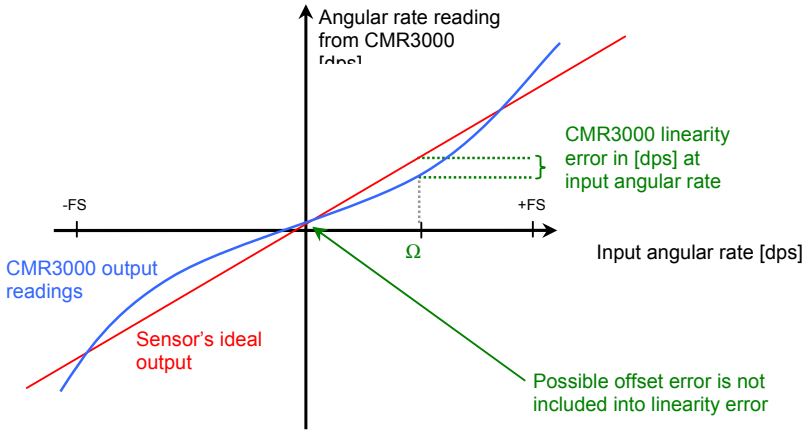


Figure 16. CMR3000's linearity error at input angular rate Ω.

Linearity error is calculated by

Equation 6

$$LinEr_{Z-axis@\Omega} = \frac{Output_{Z-axis@\Omega} - Output_{@\Omega}}{Sens \cdot FS} \cdot 100\% ,$$

where $LinEr_{Z\text{-}axis@\Omega}$ is sensor's Z-axis linearity error [%FS] on input angular rate Ω, $Output_{Z\text{-}axis@\Omega}$ is sensor's measured Z-axis output [counts] on input angular rate Ω, $Output_{@\Omega}$ is sensor's nominal output [counts] on input angular rate Ω, Sens is sensor's nominal sensitivity [counts/dps] and FS is sensor's full scale measuring range [dps] (for example for CMR3000-D01 with ±1000 dps setting → FS = 1000 dps).

Sensor's ideal output $Output_{@\Omega}$ (in Equation 6) is calculated by fitting a straight line to measured angular rate from –FS to FS.

7.4 Noise

Output noise n_X, n_Y and n_Z in X,Y and Z directions is the measured standard deviation of the output values when the sensor is not moved nor rotated ($\Omega_X = \Omega_Y = \Omega_Z = 0$ dps) in room temperature. Average noise/axis is calculated by

Equation 7

$$n = \sqrt{\frac{1}{3}\left(n_X^2 + n_Y^2 + n_Z^2\right)},$$

where n is sensor's noise [dps] per axis, n_X is sensor's X-axis noise [dps], n_Y is sensor's Y-axis noise [dps] and n_Z is sensor's Z-axis noise [dps].

7.5 Bandwidth

Signal bandwidth is measured with a rate table by rotating the table between two positions while sweeping the rotating frequency and keeping the angular rate constant.

7.6 Cross-axis sensitivity

Cross-axis sensitivity is sum of the alignment and the inherent sensitivity errors. Cross-axis sensitivity of one axis is a geometric sum of the sensitivities in two perpendicular directions.

Cross-axis sensitivity [%] of X-axis is given by

Equation 8

$$Cross_X = \pm\frac{\sqrt{S_{XY}{}^2 + S_{XZ}{}^2}}{S_X} \cdot 100\%,$$

where S_{XY} is X-axis sensitivity to Y-axis angular rate [Count/dps], S_{XZ} is X-axis sensitivity to Z-axis angular rate [Count/dps] and S_X is sensitivity of X-axis [Count/dps] angular rate.

Cross-axis sensitivity [%] of Y-axis is given by

Equation 9

$$Cross_Y = \pm\frac{\sqrt{S_{YX}{}^2 + S_{YZ}{}^2}}{S_Y} \cdot 100\%,$$

where S_{YX} is Y-axis sensitivity to X-axis angular rate [Count/dps], S_{YZ} is Y-axis sensitivity to Z-axis angular rate [Count/dps] and S_Y is sensitivity of Y-axis [Count/dps] angular rate.

Cross-axis sensitivity [%] of Z-axis is given by

Equation 10

$$Cross_Z = \pm\frac{\sqrt{S_{ZX}{}^2 + S_{ZY}{}^2}}{S_Z} \cdot 100\%,$$

where S_{ZX} is Z-axis sensitivity to X-axis angular rate [Count/dps], S_{ZY} is Z-axis sensitivity to Y-axis angular rate [Count/dps] and S_Z is sensitivity of Z-axis [Count/dps] angular rate.

Cross-axis sensitivity of CMR3000 family is measured in rate table over specified measurement range during qualification. Correct mounting position of component is important during the measurement of cross-axis sensitivity.

7.7 Turn-on time

Turn-on time is the time when the last of one X, Y, Z axis output readings stabilizes into its final value after measurement mode has been activated. The final value limits in turn-on time measurements is defined to be ±1 % of the sensor's full scale measuring range (for example for CMR3000-D01 ±1000 dps → FS = 1000 dps). Turn-on time definition for Z-axis is presented in Figure 17 below.

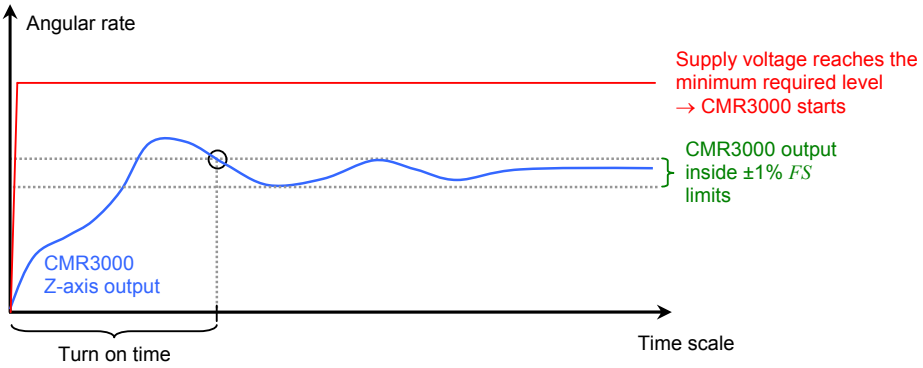


Figure 17. Turn-on time definition for one axis.

8 Document Change Control

Version	Date	Change Description
0.1	06-Nov-09	Initial draft.
0.2	18-Nov-09	Datasheet references updated
0.3	20-May-10	Section 1.2.5.2 removed, section 2.1, 4.1.4 updated, section 4.2.3 added, Tables 1, 2, 3, 4, 7 updated, Figs 2, 12, 16 updated, PDR-register added, CTRL-register content updated
0.4	12-Aug-10	X,Y,Z output register addresses table 2 updated, Fig 14 updated
0.5	20-Sep-10	Section 1.2.5.2 added, Figure 2 updated.
0.6	26-Oct-10	Figure 8 added
A.01	03-Nov-10	°/s changed to dps, Fig 5, Fig 10, Table 5 updated
A.02	21-Dec-10	Section 4.1.2.1, Fig 5, section 4.1.4, Table 6 updated