

12A, 80V and 100V, 0.200 Ohm, N-Channel Power MOSFETs

These are N-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA09594.

Ordering Information

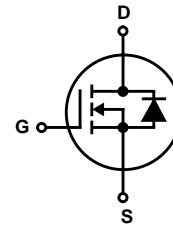
PART NUMBER	PACKAGE	BRAND
RFM12N08	TO-204AA	RFM12N08
RFM12N10	TO-204AA	RFM12N10
RFP12N08	TO-220AB	RFP12N08
RFP12N10	TO-220AB	RFP12N10

NOTE: When ordering, use the entire part number.

Features

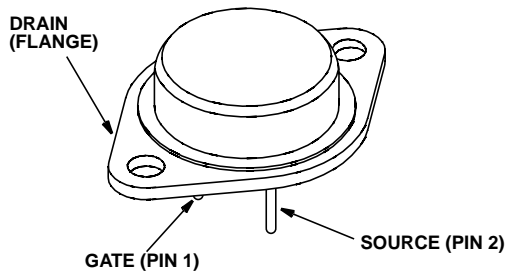
- 12A, 80V and 100V
- $r_{DS(ON)} = 0.200\Omega$
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol

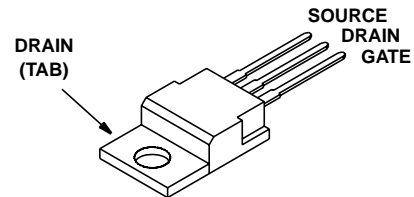


Packaging

JEDEC TO-204AA



JEDEC TO-220AB



RFM12N08, RFM12N10, RFP12N08, RFP12N10

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	RFM12N08	RFM12N10	RFP12N08	RFP12N10	UNITS	
Drain to Source Voltage (Note 1)	V_{DSS}	80	100	80	100	V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1)	V_{DGR}	80	100	80	100	V
Continuous Drain Current	I_D	12	12	12	12	A
Pulsed Drain Current (Note 3)	I_{DM}	30	30	30	30	A
Gate to Source Voltage	V_{GS}	± 20	± 20	± 20	± 20	V
Maximum Power Dissipation	P_D	75	75	60	60	W
Linear Derating Factor		0.6	0.6	0.48	0.48	W/ $^\circ\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	-55 to 150	-55 to 150	-55 to 150	$^\circ\text{C}$
Maximum Temperature for Soldering						
Leads at 0.063in (1.6mm) from Case for 10s.	T_L	300	300	300	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg}	260	260	260	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^\circ\text{C}$ to 125°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage RFM12N08, RFP12N08	BV_{DSS}	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	80	-	-	V
			100	-	-	V
RFM12N10, RFP12N10						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$ (Figure 8)	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}$	-	-	1	μA
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, T_C = 125^\circ\text{C}$	-	-	25	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	-	-	± 100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 12\text{A}, V_{GS} = 10\text{V}$ (Figures 6, 7)	-	-	0.200	Ω
Drain to Source On Voltage (Note 2)	$V_{DS(ON)}$	$I_D = 12\text{A}, V_{GS} = 10\text{V}$	-	-	2.4	V
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 50\text{V}, I_D = 6\text{A}, R_G = 50\Omega,$ $V_{GS} = 10\text{V}, R_L = 8\Omega,$ (Figures 10, 11, 12)	-	45	70	ns
Rise Time	t_r		-	250	375	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	85	130	ns
Fall Time	t_f		-	100	150	ns
Input Capacitance	C_{ISS}		$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$ (Figure 9)	-	-	850
Output Capacitance	C_{OSS}	-		-	300	pF
Reverse Transfer Capacitance	C_{RSS}	-		-	150	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	RFM12N08, RFM12N10	-	-	1.67	$^\circ\text{C/W}$
		RFP12N08, RFP12N10	-	-	2.083	$^\circ\text{C/W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Voltage (Note 2)	V_{SD}	$I_{SD} = 6\text{A}$	-	-	1.4	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 4\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	150	-	ns

NOTE:

2. Pulse test: Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
3. Repetitive rating: pulse width is limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

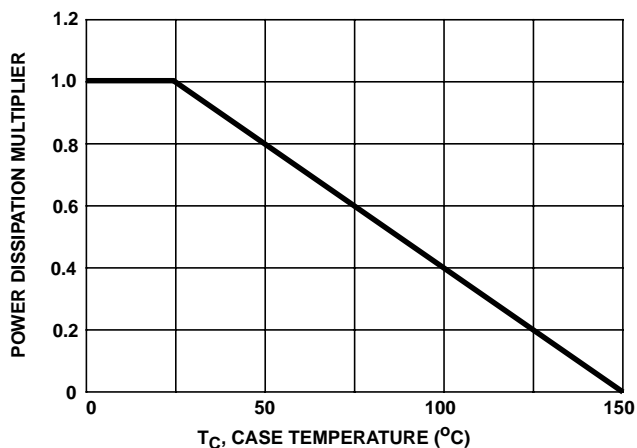


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

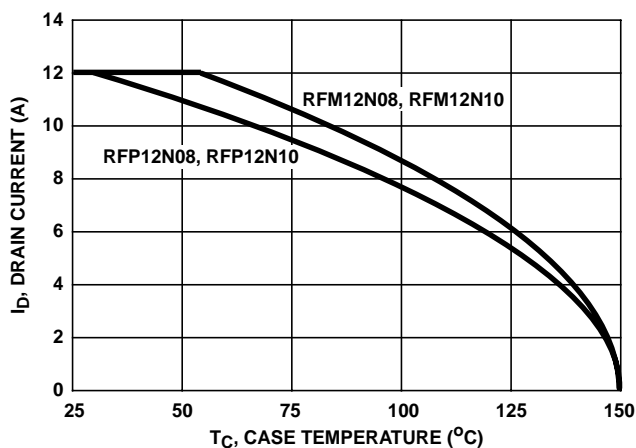


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

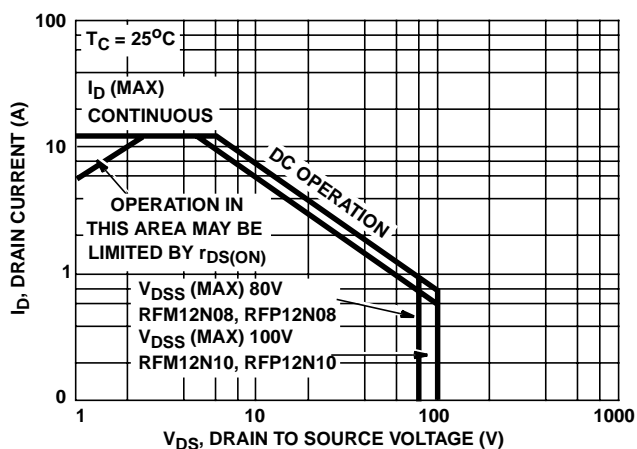


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

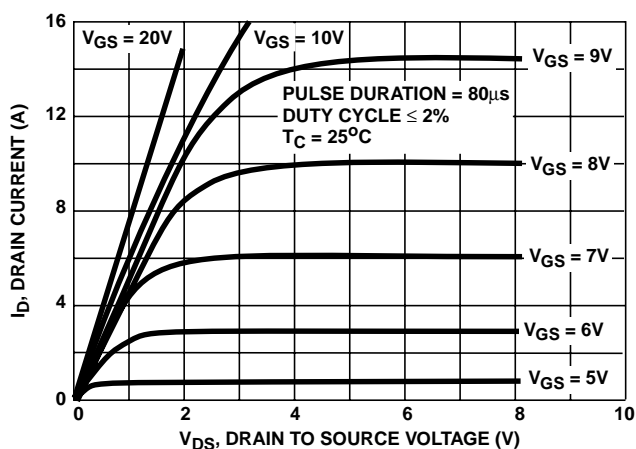


FIGURE 4. SATURATION CHARACTERISTICS

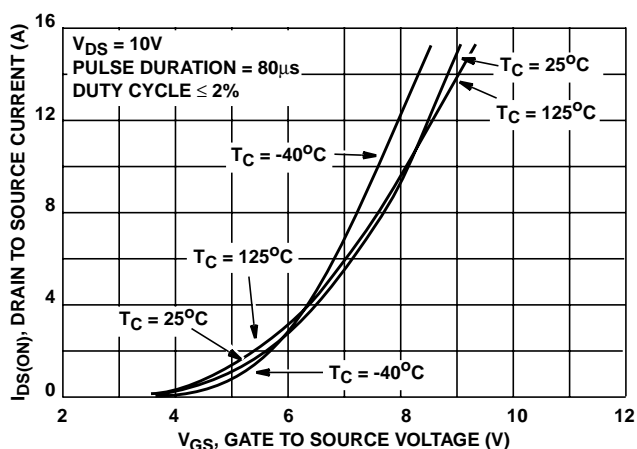


FIGURE 5. TRANSFER CHARACTERISTICS

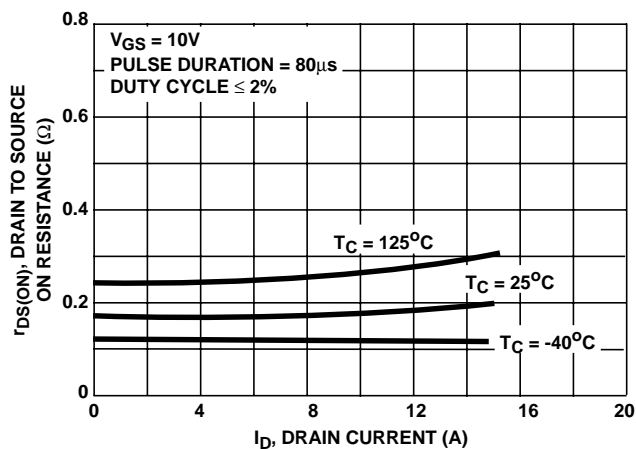


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

Typical Performance Curves Unless Otherwise Specified (Continued)

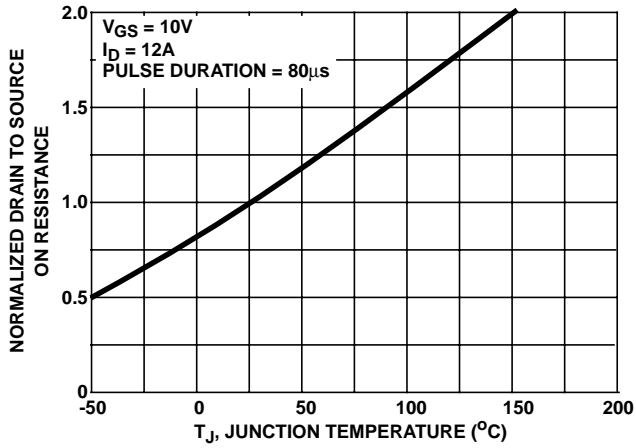


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

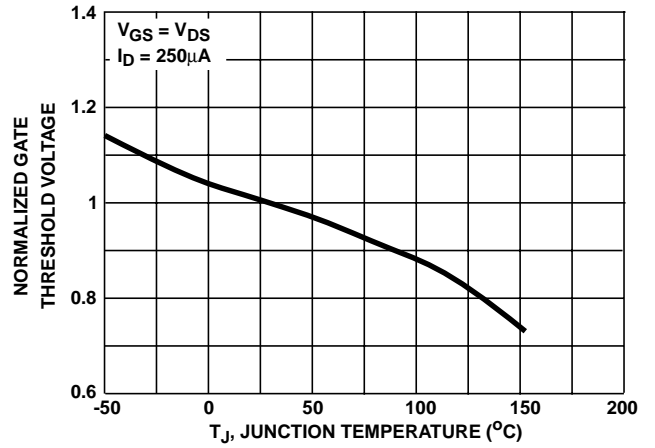


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

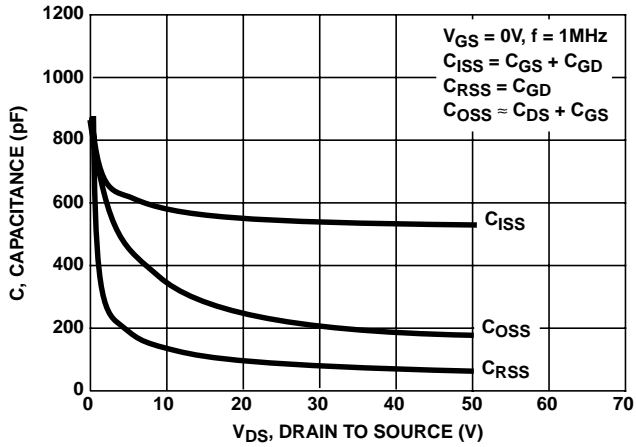
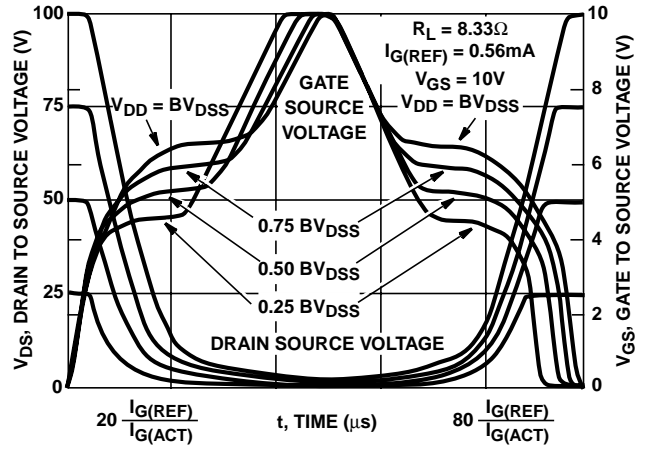


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

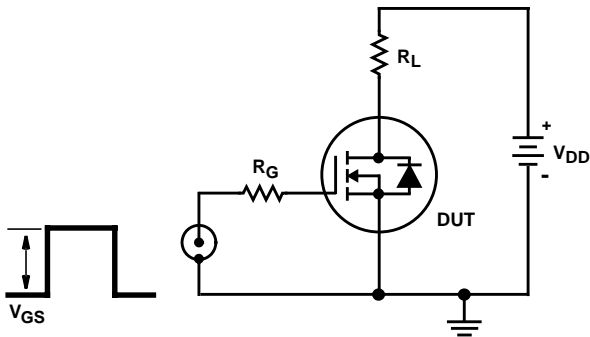


FIGURE 11. SWITCHING TIME TEST CIRCUIT

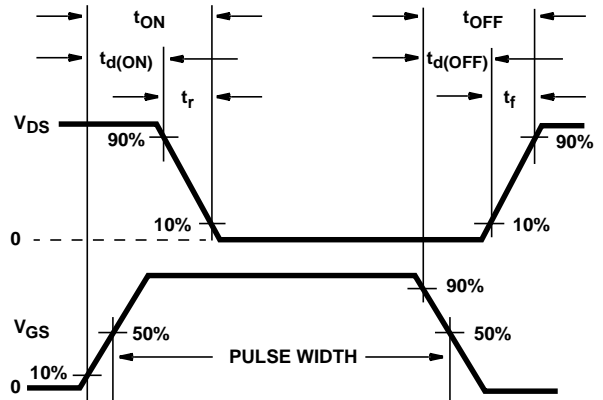


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS

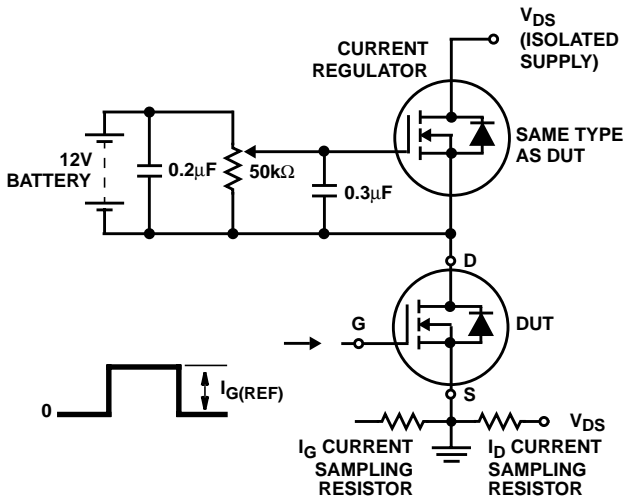


FIGURE 13. GATE CHARGE TEST CIRCUIT

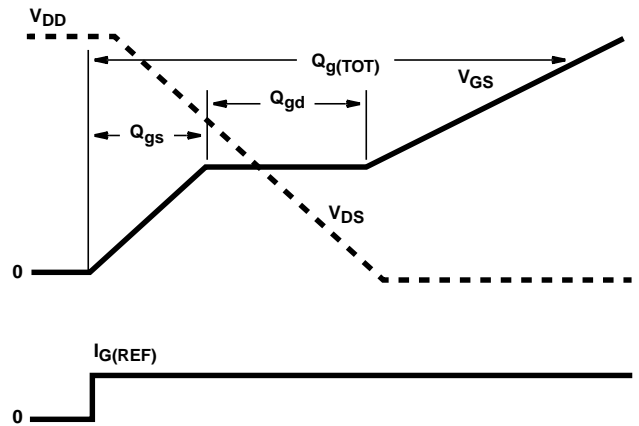


FIGURE 14. GATE CHARGE WAVEFORMS