NMOS 4-BIT MICROCONTROLLER

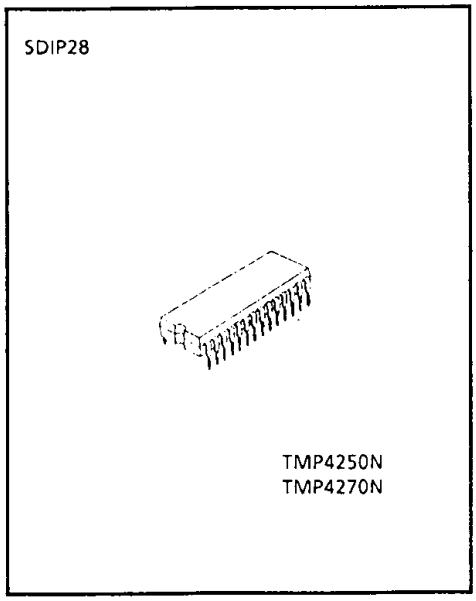
TMP4250N, TMP4270N

The 4250 / 70 are high speed, 4-bit single chip microcomputers with additional input/output ports and based on the TLCS-42 NMOS series.
The 4250 / 70 are suitable for control of home appliances (such as fans, air-conditioners, refrigerators), audio equipments, games, and toys.

PART No.	ROM	RAM	PACKAGE	PIGGYBACK BOARD
TMP4250N	512 x 8-bit	32 x 4-bit	SDIP28	BM4211B
TMP4270N	1024 x 8-bit			

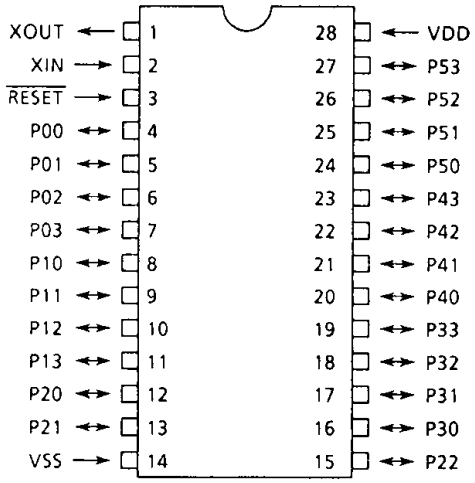
FEATURES

- ◆4-bit single chip microcomputer
- ◆Instruction execution time : 2.5μs (at 2MHz)
- ◆42 basic instructions
  - All instructions are one byte object code
  - Table look-up instructions
- ◆Stack for subroutine call : 1 level
- ◆I/O port (11 pins)
  - I/O 3ports 11pins
- ◆Interval Timer (11 stages)
- ◆High current outputs
  LED direct drive is available.
- ◆Real Time Emulator : BM4221A

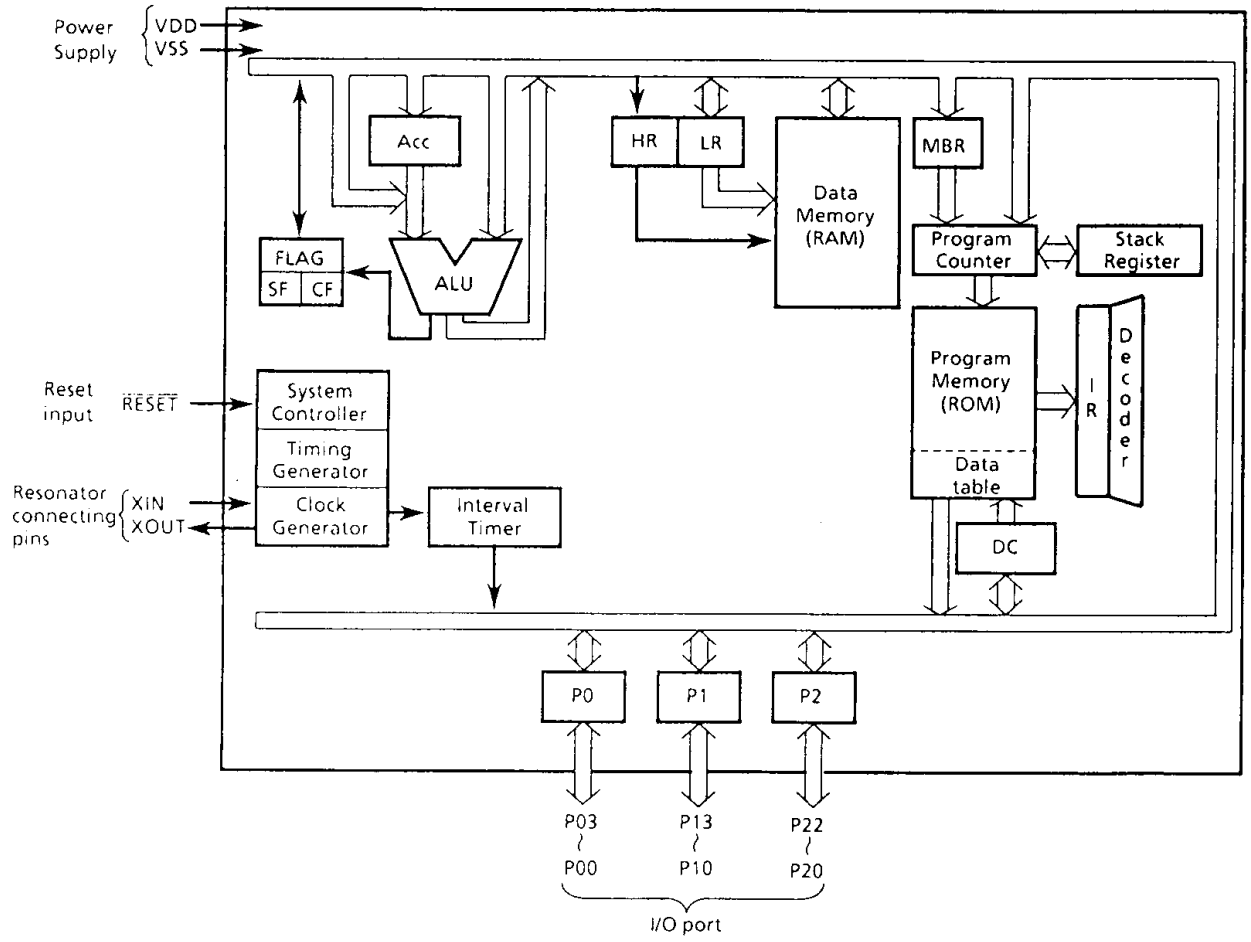


PIN ASSIGNMENT (TOP VIEW)

SDIP28



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	INPUT/OUTPUT	FUNCTION
P03 - P00	I/O	4-bit programmable I/O ports with latch. When used as input port, the latch must be set to "1".
P13 - P10		
P22 - P20		3-bit programmable I/O port with latch. When used as input port, the latch must be set to "1".
P33 - P30		4-bit programmable I/O ports with latch. When used as input port, the latch must be set to "1".
P43 - P40		
P53 - P50		
XIN	INPUT	Resonator connecting pins. For inputting external clock, XIN is used and XOUT is opened.
XOUT	OUTPUT	
$\overline{\text{RESET}}$	INPUT	Reset signal input
VDD	Power Supply	+ 5V
VSS		0V (GND)

OPERATIONAL DESCRIPTION

The 4250/70 are simular to the 4240/60, except for the addition of 3 input/output ports (12 pins) . All other operations and functions are exactly the same as those of the 4240/60 (Naturally, the 4250/70 have interval timers). Consequently, except for the input/output ports, all operations are the same as those of the 42C40/60 which are standard LSIs in the TLCS-42 CMOS series (However, the 4250/70 do not have hold functions and port registers). Refer to the 42C40/60 technical data sheets for details.

1. PERIPHERAL HARDWARE FUNCTION

1.1 I/O Ports

The 4250/70 have 3 I/O ports (11 pins) each as follows :

(1) P0, P1 ; 4-bit input/output
(2) P2 ; 3-bit input/output
(3) P3, P4, P5 ; 4-bit input/output

The following explanation covers only port (3) added to the 4240/60. All of the ports have output latches, so output data are held by the latches. There is no input latch, so external input data are either held externally until read, or are read several times before processing, when necessary.

(1) Ports P3 (P33-P30), P4 (P43-P40), P5 (P53-P50)
These are input/output ports with latch. Ports P0 and P1 have 4 bits each, and P2 has 3 bits. When used as input ports, latch should be set to "1".
Pull-up resistor can be specified for each bit by mask options.
In addition, the 4240 does not have as interval timer ; therefore, interval timer output (ITS) is permanently set to "1".

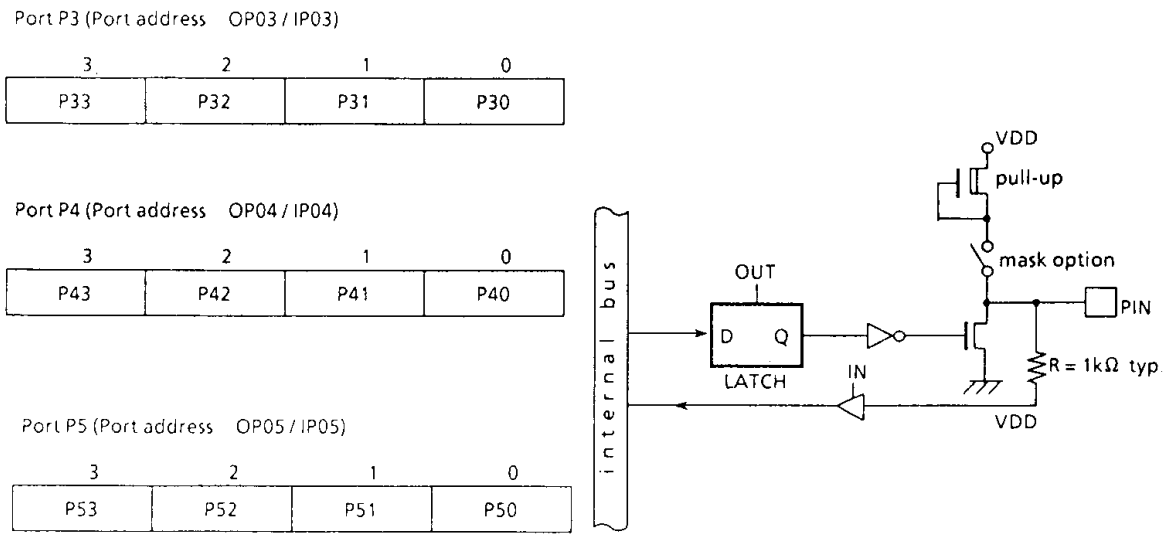


Figure 1-1 Ports P3, P4 and P5

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATINGS	UNIT
Supply Voltage	V_{DD}		− 0.5 to 7	V
Input Voltage	V_{IN}		− 0.5 to 7	V
Output Voltage	V_{OUT1}	Except sink open drain pin	− 0.5 to 7	V
	V_{OUT2}	Sink open drain pin	− 0.5 to 15	
Output Current (total)	ΣI_{OUT}		90	mA
Power Dissipation [T_{opr} = 85°C]	PD		300	mW
Soldering Temperature (time)	T_{sld}		260 (10sec)	°C
Storage Temperature	T_{stg}		− 55 to 125	°C
Operating Temperature	T_{opr}		− 40 to 85	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = − 40 to 85°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}			4.5	5.5	V
Input High Voltage	V_{IH1}	Except $\overline{RESET}$		2.2	V_{DD}	V
	V_{IH2}	$\overline{RESET}$ pin		3.0		
Input Low Voltage	V_{IL1}	Except $\overline{RESET}$ pin		0	0.8	V
	V_{IL2}	$\overline{RESET}$ pin			0.6	
Clock Frequency	fc			0.2	2.0	MHz

D.C. CHARACTERISTICS

(V_{SS} = 0V, T_{opr} = − 40 to 85°C)

PARAMETER	SYMBOL	PIN	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	$\overline{RESET}$		−	0.3	−	V
Input Current	I_{IN}	Open drain pin	V_{DD} = 5.5V, V_{IN} = 0.4V	−	− 10^{-5}	− 2.0	μA
Low Level Input Current	I_{IL1}	$\overline{RESET}$	V_{DD} = 5.5V, V_{IN} = 0.6V	−	− 50	− 100	μA
	I_{IN2}	Pin with pull-up resistor		−	−	− 360	
Output Leakage Current	I_{LO}	Open drain pin	V_{DD} = 5.5V, V_{OUT} = 5.5V	−	10^{-5}	2.0	μA
Output Level High Voltage	V_{OH}	Pin with pull-up resistor	V_{DD} = 5V, I_{OH} = − 5μA	4.7	4.9	−	V
Output Level High Current	I_{OH}		V_{DD} = 4.5V, V_{OH} = 2.4V	− 50	−	−	μA
Low Level output Current	I_{OL1}	Port P0, P1, P2	V_{DD} = 4.5V, V_{OL} = 0.4V	1.6	10.0	−	mA
	I_{OL2}		V_{DD} = 4.5V, V_{OL} = 1.2V	10	25	−	
Supply Current	I_{DD}		VDD = 5.5V	−	19	40	mA

Note1. Typ. values shows those at V_{DD} = 5V, T_{opr} = 25°C

Note2. Supply Current : $\overline{RESET}$ pin is 0V, and XOUT pin and ports are opened in the external clock operation.

A.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, T_{opr} = − 40 to 85°C)

PARAMETER	SYMBOL	CONDITIONS		Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}			2.5	−	25	μs
High level Clock pulse Width	t_{WCH}	$V_{IN} = V_{IH}$	For external clock operation	100	−	−	ns
Low level Clock pulse Width	t_{WCL}	$V_{IN} = V_{IL}$					

RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, T_{opr} = − 40 to 85°C)

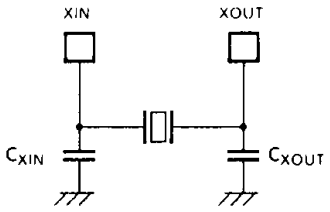
(1) Ceramic Rrsonator

2MHz

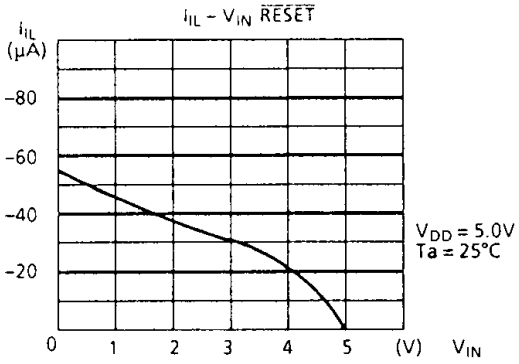
CSA2.00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 50pF

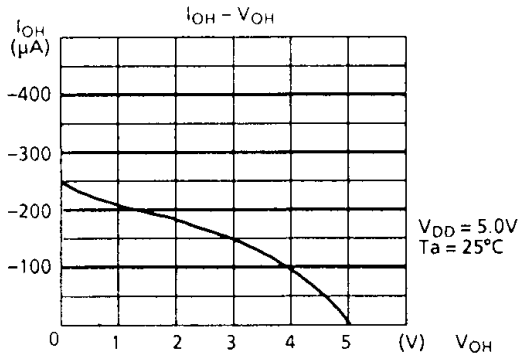
400KHz

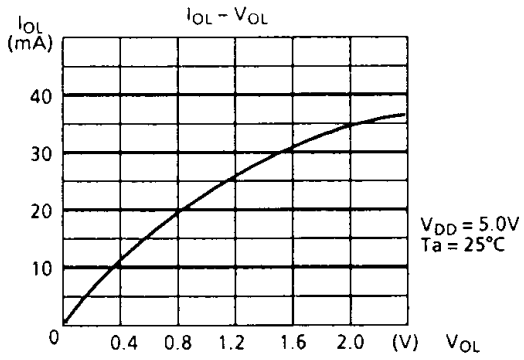
CS8400B (MURATA) $C_{XIN} = C_{XOUT}$ = 220pF

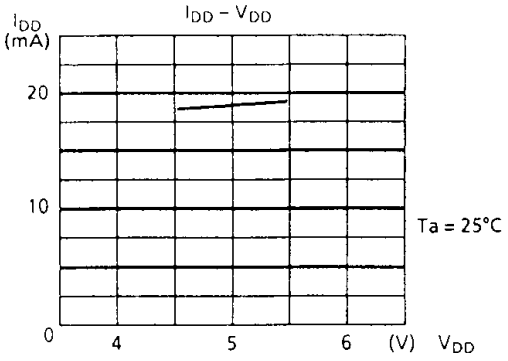


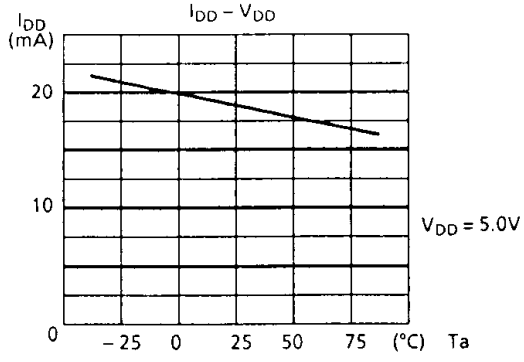
TYPICAL CHARACTERISTICS







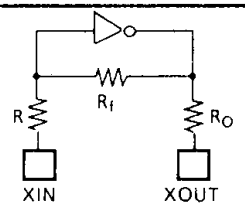
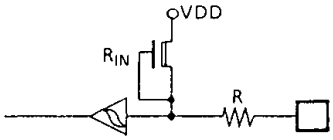




INPUT/OUTPUT CIRCUITRY

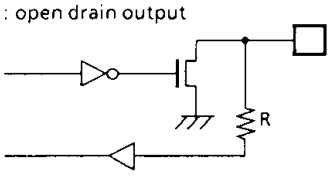
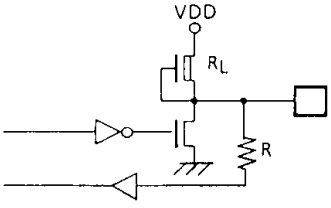
(1) Control pins

Input/Output circuitries of the 42C50/70 control pins are shown below.

CONTROL PIN	I/O	CIRCUITRY	REMARKS
XIN XOUT	INPUT OUTPUT		Resonator connecting pins R = 1KΩ (typ.) R_f = 1MΩ (typ.) R_O = 0.5KΩ (typ.)
RESET	INPUT		Hysteresis input Pull-up resistor R_{IN} = 90KΩ (typ.) R = 1KΩ (typ.)

(2) I/O ports

Input/Output circuitries of the 42C50/70 I/O ports are shown below. Pull-up resistor can be specified for each bit by mask option.

PORT	I/O	CIRCUITRY	INITIAL STATE	REMARKS
P0 P1 P2 P3 P4 P5	I/O	Option : open drain output 	Hi-Z (INPUT)	Sink open drain output R = 1KΩ (typ.)
		Option : open drain output with pull-up 	High (INPUT)	Pull-up resistor R_L = 20KΩ (typ.) R = 1KΩ (typ.)