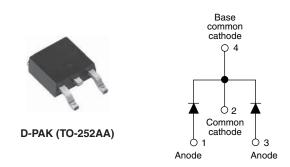
Vishay Semiconductors

Ultrafast Rectifier, 2 x 3 A FRED Pt[®]



PRODUCT SUMMARY				
Package	D-PAK (TO-252AA)			
I _{F(AV)}	2 x 3 A			
V _R	200 V			
V _F at I _F	1.0 V			
t _{rr} typ.	See Recovery table			
T _J max.	175 °C			
Diode variation	Common cathode			

FEATURES

- Ultrafast recovery time
- Low forward voltage drop
- Low leakage current
- 175 °C operating junction temperature
- Compliant to RoHS Directive 2002/95/EC
- Halogen-free according to IEC 61249-2-21
 definition
- Meets MSL level 1, per J-STD-020, LF maximum peak of 260 °C

DESCRIPTION/APPLICATIONS

Vishay Semiconductors' 200 V series are the state of the art hyperfast recovery rectifiers specifically designed with optimized performance of forward voltage drop and hyperfast recovery time.

The planar structure and the platinum doped life time control, guarantee the best overall performance, ruggedness and reliability characteristics.

These devices are intended for use in the output rectification stage of SMPS, UPS, DC/DC converters as well as freewheeling diode in low voltage inverters and chopper motor drives.

Their extremely optimized stored charge and low recovery current minimize the switching losses and reduce over dissipation in the switching element and snubbers.

ABSOLUTE MAXIMUM RATINGS						
PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS		
Peak repetitive reverse voltage	V _{RRM}		200	V		
Average rectified forward current per device	I _{F(AV)}	Total device, rated V _R , T _C = 159 °C	6			
Non-repetitive peak surge current	I _{FSM}		50	А		
Peak repetitive forward current per diode	I _{FM}	Rated V _R , square wave, 20 kHz, T _C = 159 °C	6			
Operating junction and storage temperatures	T _J , T _{Stg}		- 65 to 175	°C		

ELECTRICAL SPECIFICATIONS ($T_J = 25 \text{ °C}$ unless otherwise specified)								
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS		
Breakdown voltage, blocking voltage	V _{BR} , V _R	I _R = 100 μA	200	-	-			
		I _F = 3 A	-	-	1			
Forward voltage	V _F	I _F = 3 A, T _J = 125 °C	-	-	0.9	V		
		I _F = 6 A	-	-	1.2			
		I _F = 6 A, T _J = 125 °C	-	-	1.08			
Devenue la clue de compart		$V_{R} = V_{R}$ rated	-	-	5			
Reverse leakage current I _R		$T_J = 125 \text{ °C}, V_R = V_R \text{ rated}$	-	-	100	μA		
Junction capacitance	CT	V _R = 200 V		12	-	pF		
Series inductance	L _S	Measured lead to lead 5 mm from package body	-	8.0	-	nH		

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HALOGEN

FREE



VS-6CWH02FN-M3

Vishay Semiconductors Ultrafast Rectifier, 2 x 3 A FRED Pt®



DYNAMIC RECOVERY CHARACTERISTICS (T _J = 25 $^{\circ}$ C unless otherwise specified)								
PARAMETER	SYMBOL	TEST CON	MIN.	TYP.	MAX.	UNITS		
		$I_F = 1.0 \text{ A}, \text{ d}I_F/\text{d}t = 50 \text{ A}/1000 \text{ A}$	⁄μs, V _R = 30 V	-	-	35		
Reverse recovery time	t _{rr}	T _J = 25 °C	I _F = 3 A V _R = 160 V dI _F /dt = 200 A/μs	-	19	-	ns A	
		T _J = 125 °C		-	26	-		
Deels receiver a current		T _J = 25 °C		-	3.1	-		
Peak recovery current	I _{RRM}	T _J = 125 °C		-	4.6	-		
D	0	T _J = 25 °C		-	30	-	nC	
Reverse recovery charge	Q _{rr}	T _J = 125 °C		-	60	-	nc	

THERMAL - MECHANICAL SPECIFICATIONS						
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	
Maximum junction and storage temperature range	T _J , T _{Stg}	- 65	-	175	°C	
Thermal resistance, junction to case per leg	R _{thJC}	-	-	5		
Thermal resistance, junction to ambient per leg	R _{thJA}	-	-	80	°C/W	
Thermal resistance, case to heatsink	R _{thCS}	-	-	-		
Waisht		-	0.3	-	g	
Weight		-	0.01	-	oz.	
Mounting torque		6.0 (5.0)	-	12 (10)	kgf · cm (lbf · in)	
Marking device		Case style D-PAK 6CWH02FN		02FN		

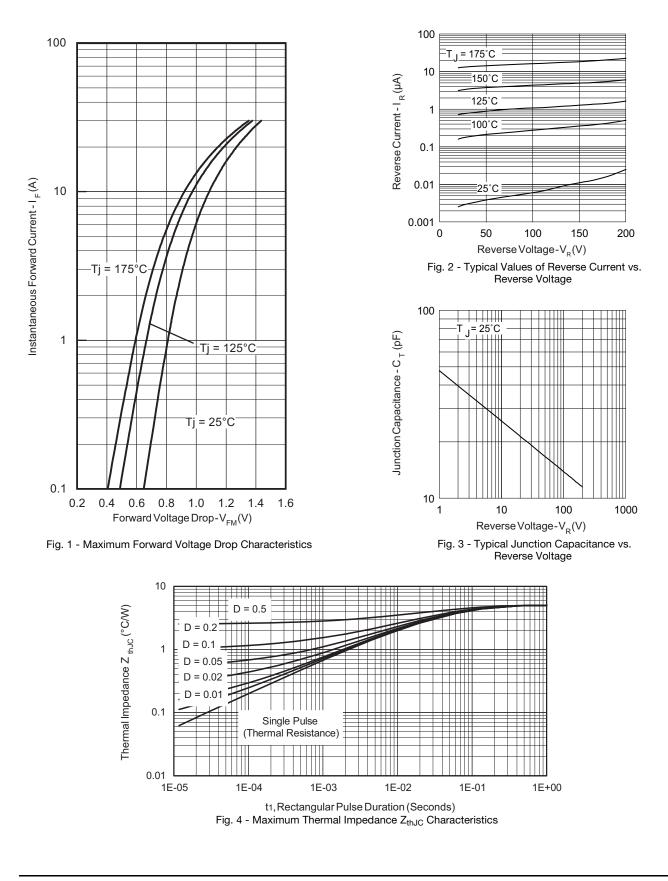
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Ultrafast Rectifier, 2 x 3 A FRED Pt® **Vishay Semiconductors**



VS-6CWH02FN-M3

Vishay Semiconductors Ultrafast Rectifier, 2 x 3 A FRED Pt®



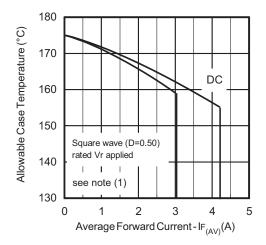


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current

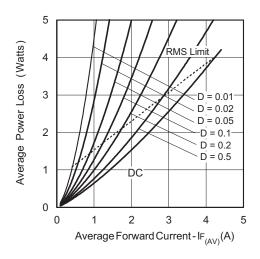
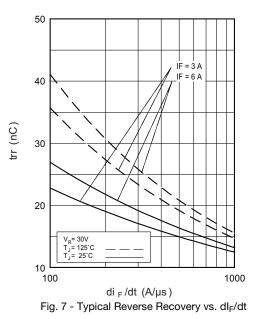


Fig. 6 - Forward Power Loss Characteristics

Note

⁽¹⁾ Formula used: $T_C = T_J - (Pd + Pd_{REV}) \times R_{thJC}$; $Pd = Forward power loss = I_{F(AV)} \times V_{FM} at (I_{F(AV)}/D)$ (see fig. 6); $Pd_{REV} = Inverse power loss = V_{R1} \times I_R (1 - D)$; $I_R at V_{R1} = Rated V_R$



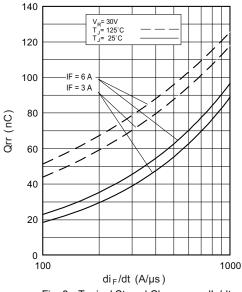


Fig. 8 - Typical Stored Charge vs. dl_F/dt

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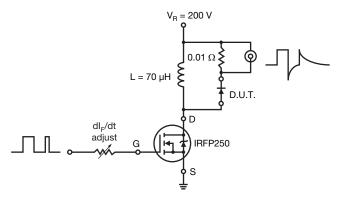


Fig. 9 - Reverse Recovery Parameter Test Circuit

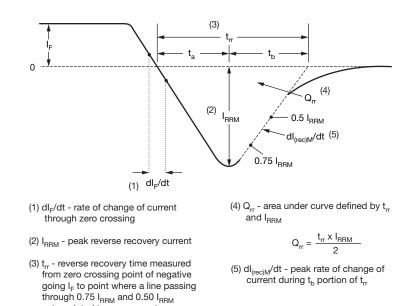


Fig. 10 - Reverse Recovery Waveform and Definitions

extrapolated to zero current.

5

VS-6CWH02FN-M3

Vishay Semiconductors Ultrafast Rectifier, 2 x 3 A FRED Pt®



ORDERING INFORMATION TABLE

Device code	VS-	6	с	w	н	02	FN	TRL	-M3
	1	2	3	4	5	6	7	8	9
	1	- Visl	hay Sem	niconduc	ctors pro	oduct			
	2	- Cur	rent rati	ng (6 =	6 A)				
	3	- Cer	nter tap	configur	ation				
	4	- Pac	Package identifier:						
		W =	D-PAK						
	5	- H=	Hyperfa	ast recov	very				
	6	- Vol	tage rati	ng (02 =	= 200 V)				
	7	- FN	= TO-25	52AA					
	8	- • N	• None = Tube (50 pieces)						
		• TI	R = Tap	e and re	el				
		• TF	RL = Ta	pe and r	eel (left	oriente	d)		
		• TF	R = Ta	pe and	reel (rigl	ht orien	ted)		
	9 -	- Env	vironmer	ntal digit	:				
		-M3	s = Halog	gen-free	, RoHS	complia	ant and	termina	tions le

ORDERING INFORMATION (Example)							
PREFERRED P/N	QUANTITY PER T/R	MINIMUM ORDER QUANTITY	PACKAGING DESCRIPTION				
VS-6CWH02FN-M3	75	3000	Antistatic plastic tube				
VS-6CWH02FNTR-M3	2000	2000	13" diameter reel				
VS-6CWH02FNTRL-M3	3000	3000	13" diameter reel				
VS-6CWH02FNTRR-M3	3000	3000	13" diameter reel				

LINKS TO RELATED DOCUMENTS				
Dimensions www.vishay.com/doc?95016				
Part marking information	www.vishay.com/doc?95176			
Packaging information	www.vishay.com/doc?95033			

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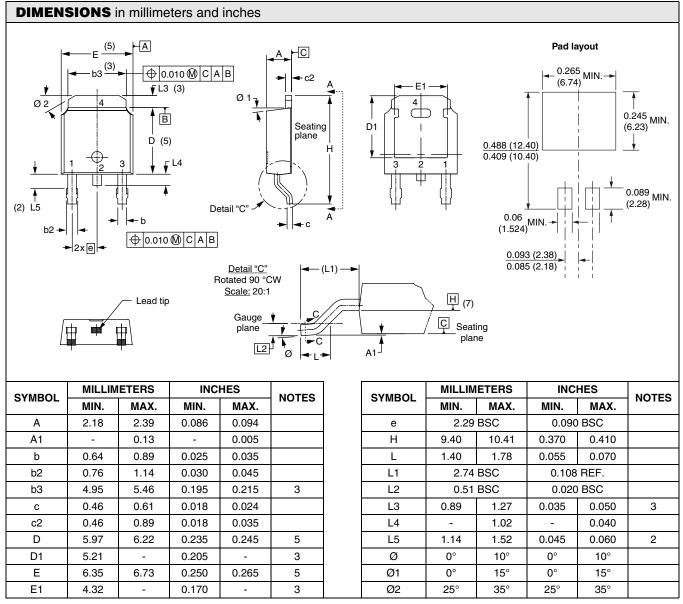
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Vishay High Power Products

D-PAK (TO-252AA)



Notes

- ⁽¹⁾ Dimensioning and tolerancing as per ASME Y14.5M-1994
- ⁽²⁾ Lead dimension uncontrolled in L5
- ⁽³⁾ Dimension D1, E1, L3 and b3 establish a minimum mounting surface for thermal pad
- (4) Section C C dimension apply to the flat section of the lead between 0.13 and 0.25 mm (0.005 and 0.10") from the lead tip
- ⁽⁵⁾ Dimension D, and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- ⁽⁶⁾ Dimension b1 and c1 applied to base metal only
- ⁽⁷⁾ Datum A and B to be determined at datum plane H
- ⁽⁸⁾ Outline conforms to JEDEC outline TO-252AA

Document Number: 95016 Revision: 04-Nov-08 For technical questions concerning discrete products, contact: <u>diodes-tech@vishay.com</u> For technical questions concerning module products, contact: <u>ind-modules@vishay.com</u>



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