SC2642
Multi-Platform Two-Phase PWM Controller

POWER MANAGEMENT

Description

The SC2642 provides microprocessor core voltage regulation solution with two paralleled PWM channels. Multi-phase buck regulator utilizes the phase-shift timing control to allow interleaved switching of the power switches. This architecture minimizes the core voltage ripple and the input current ripple, which leads to optimized voltage regulator design for power density, transient responses, and the thermal performances.

To satisfy the highly dynamic nature of the modern microprocessors, the SC2642 adopts peak current mode control topology which ensures wide control loop bandwidth and fast transient responses. The current mode control provides intrinsic phase current matching. The maximum ripple frequency is greater than 1MHz.

One of the outstanding features of the SC2642 is its voltage regulation accuracy. Not only it provides better than 1% set point accuracy, but also the accuracy to fully complaint with the stringent load line slope specifications mandated by the modern microprocessors.Lossless output current sensing ensures the regulator output voltage is accurately positioned according to the load current condition, and an internal temperature compensation technology further enhances the performance of voltage accuracy.

The patented Combi-Sense™ topology is employed by SC2642. The MOSFET $R_{ds(on)}$ and the output inductor winding resistance are used to generate the phase current information. The Combi-Sense™ MOSFET driver plus the SC2642 enables the complete solution.

The SC2642 is a multi-platform controller. It conforms to Intel VRM/VRD10.0, VRM9.X, and AMD K-8 (Opteron™) VID specifications. With very minor changes of the schematic and the layout, the SC2642 based solution can be ported form one platform to another. This greatly benefits the system manufactures for reductions of design cycle and minimize the inventory management.

The VID structure of the SC2642 supports VID-on-Fly applications for any platform. The cycle-by-cycle current limit plus the intelligent over current shut down provide the maximum versatility of the system without false tripping under all possible changes of VID and load conditions. The differential voltage feedback sense eliminates the error caused by high load current on the ground plane. External offset is easy to achieve for any platforms and the VID settings. The enable function is also provided to interface with the corresponding system signal for correct start up timing and shut down timing.

Features

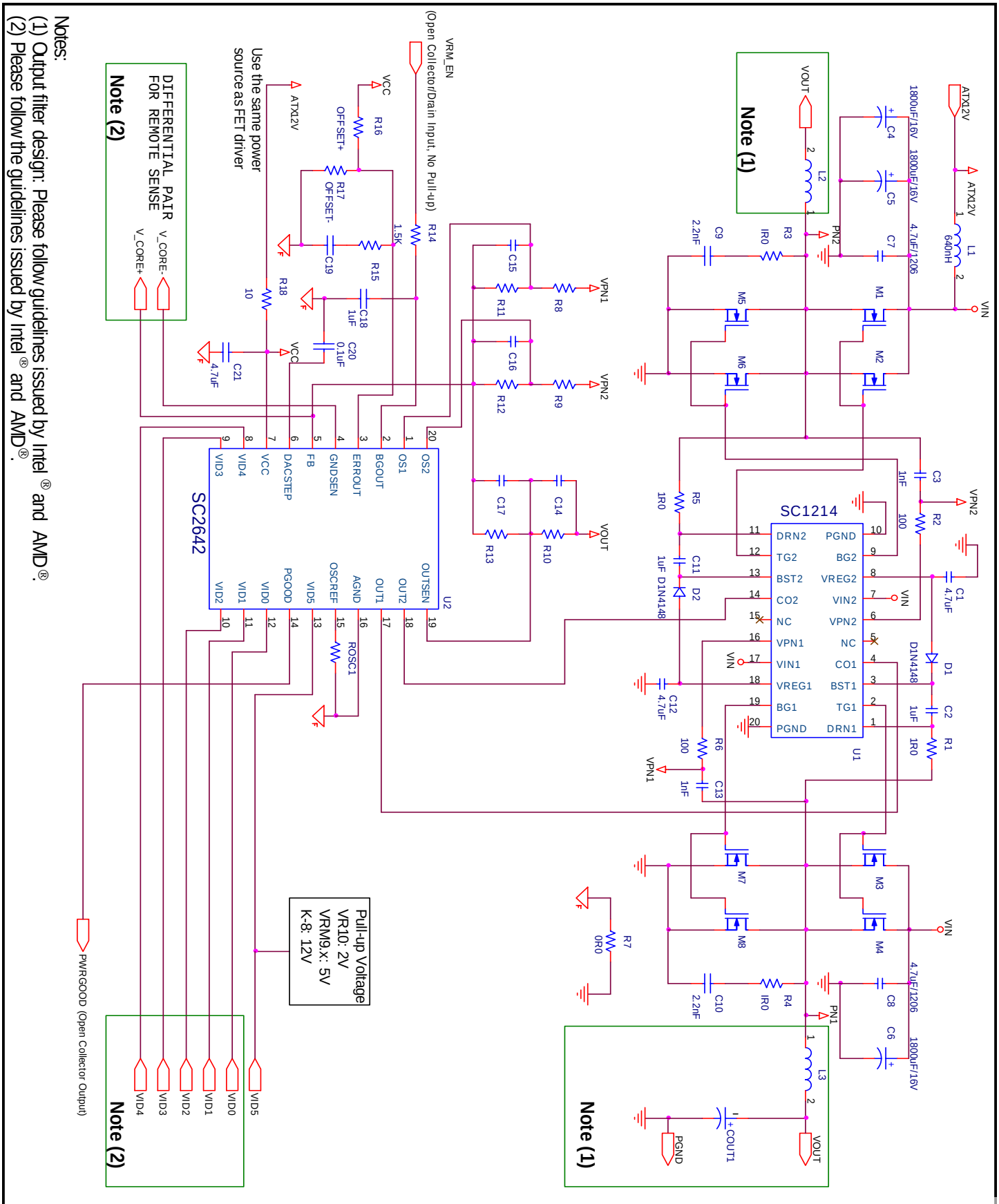
- VRD/VRM10.0, VRM9.X, and K-8 compliant
- Core Voltage Set Point Accuracy 0.5%
- Combi-Sense™ Current Mode Control
- Intrinsic Phase Current Matching
- Fast Transient Responses
- Active Droop with Temperature Compensation to Meet Load Line Slope
- Support VID-on-Fly with 5 or 6 bit VID
- Enable Function for Power Sequencing
- Cycle-by-Cycle Peak Current Limit
- Intelligent Over Current Shut Down
- Over Voltage Protection When Using Semtech Combi-Sense™ Driver SC1211
- Under Voltage Protection Built in
- External programmable Soft-Start
- Externally programmable switching frequency (up to 1MHz output ripple frequency)

Applications

- Voltage Regulator VRD10.x
- Voltage Regulator VRM9.X
- Voltage Regulator K-8
- High Current, Low Voltage Step Down DC/DC Converters

POWER MANAGEMENT

Typical Application Circuit



Notes:
(1) Output filter design: Please follow guidelines issued by Intel ® and AMD ®.
(2) Please follow the guidelines issued by Intel ® and AMD ®.

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Supply Voltage	V_{CC}	20	V
Combi-Sense/Direct Output Voltage	OS1, OS2, OUTSEN	5	V
VID pins except VID5,Frequency pin	VID0 ~ VID4,OSCREF	7	V
Ground sense	GSENSE	-0.3 to 0.3	V
All other pins		Vcc + 0.3	V
Ambient Temperature Range	T_A	0 to 105	°C
Junction Temperature Range	T_J	0 to 125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	260	°C

Electrical Characteristics

Unless specified: V_{CC} = 12V, VID=1.50V (101110,VRD10), F_{OSC} = 200kHz/phase, T_A = 27°C. See Typical Application Circuit.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Chip_Supply						
IC Supply Voltage	V_{CC}		7.5	12	14	V
IC Supply Current	I_{CC}			10	13	mA
UVLO Ramp Up				7.3	7.5	V
UVLO Ramp Down			6.4	6.6		V
Reference Section						
Bandgap Output	V_{BGOUT}	C_{BGOUT} = 4.7nF	2.945	2.990	3.035	V
Source Current			220	300	330	µA
Supply Rejection		V_{CC} = 10.0V ~ 14.0V		0.5		mV/V
Temperature Stability		0°C < T_A < 85°C		1		%
VID Step		VRM9.X, K-8, LSB		25		mV
VID Step		VRD/VRM10, LSB		12.5		mV
Voltage Accuracy	V_{OUT}	VRD10 ; Internal offset=-20mV	-0.5		+0.5	%
		VRM9.x ; Internal offset=-20mV	-1		+1	%
		K-8 ; Internal offset=+25mV	-1		+1	%
Oscillator Section						
Switching Frequency		R_{OSC} = 230K / Per phase	180	200	220	kHz
Switching Frequency Range		Per phase	100		500	kHz
Temperature Stability		0°C < T_A < 85°C		+/- 5		%

NOTE : 1) Guaranteed by design, not tested in production. Specifications subject to change without notice.

Electrical Characteristics (Cont.)

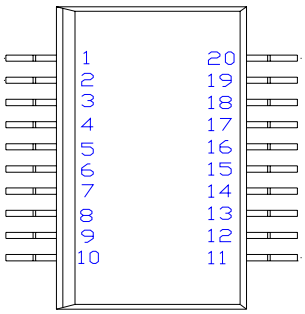
Unless specified: V_{CC} = 12V, VID=1.50V (101110,VRD10), F_{OSC} = 200kHz/phase, T_A = 27°C. See Typical Application Circuit.

Parameter	Test Conditions	Min	Typ	Max	Units
Voltage Error Amplifier					
Input Offset Voltage			+/- 3		mV
Input Bias Current			25		nA
Open Loop Gain	1V < V_{ERROUT} < 4V		80		dB
Unity Gain Bandwidth	C_{ERROUT} = 10pF		10		MHz
Slew Rate			10		V/µS
Transconductance Gain			0.5		mA/V
Clamp level for OCP			4.4		V
Clamp level Accuracy		- 8		+ 8	%
Current Sense Amplifiers					
Input Offset Voltage			+/- 3		mV
Input Bias Current			50		nA
Gain			10		V/V
CMRR	0 to 3V		80		dB
Input Common Mode Range		-0.3		3	V
Gain Match			2		%
Bandwidth			6		MHz
Droop Amplifier					
Gain			5.4		V/V
Gain Accuracy(1)			+/- 5		%
VIDs					
Input low voltage threshold	[VID0:5]			1.2	V
Input high voltage threshold	[VID0:5]	1.8			V
Bias current	[VID0:4] = 0V	120	185	250	uA
VID5 pull up voltage for VRD/VRM10	VID5	1.8		2.5	V
VID5 pull up voltage for VRM9.X	VID5	4		6	V
VID5 pull up voltage for K-8	VID5	8		VCC	V
Power Good					
Threshold Rising	VID - Power Good Threshold	250	350	400	mV
Threshold Falling	VID - Power Good Threshold		575		mV
Output High Leakage	Pwrgood = V_{CC}		100		nA
Output Low Sink	Pwrgood = 0.8V	2			mA
Current Limit Section					
Shutdown Voltage	VID - Shut Down Threshold	550	650	750	mV

NOTE : 1) Guaranteed by design, not tested in production. Specifications subject to change without notice.

Pin Configurations

Top View



(20-Pin TSSOP)

Ordering Information

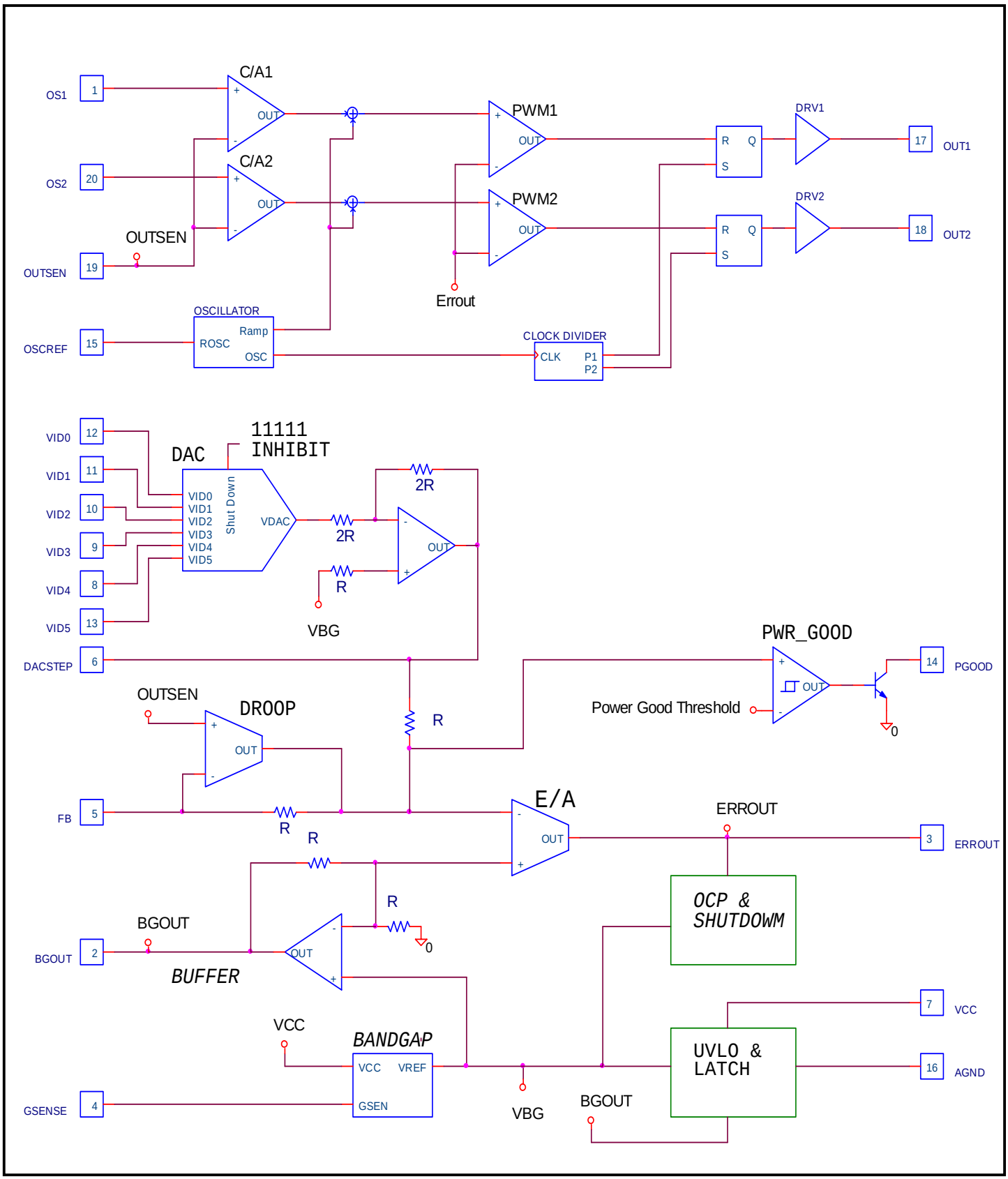
Part Number	Package	Temp. Range (T_J)
SC2642TSTR(1)	TSSOP-20	0 to 125 °C
SC2642TSTRT(1)(2)	TSSOP-20	0 to 125 °C
SC2642EVB	Evaluation Board	

Note:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free package. Device is fully WEEE and RoHS compliant.

Pin Descriptions

Pin#	Pin Name	Pin Function
1	OS1	Current sense input 1.
2	BGOUT	BG reference pin. Connect soft start cap to AGND.
3	ERROUT	Error-amplifier output. Connect compensation network to AGND.
4	GSENSE	Remote sense for GND. Rout with FB trace as a differnetial pair to the CPU socket.
5	FB	Feedback pin.
6	DACSTEP	VID step speed setting. Connect a cap to AGND to program the DAC slew rate.
7	VCC	Power supply for chip.
8	VID4	VID MSB.
9	VID3	
10	VID2	
11	VID1	
12	VID0	VID LSB.
13	VID5	12.5mV bit for VR10. VID5 pull-up to VCC for K-8; VID5 pull-up to 5V for VRM9.X.
14	PGOOD	Power good. Open Collect output.
15	OSCREF	Oscillator frequency setting. Connect a resistor to AGND.
16	AGND	Clean ground for analog signals.
17	OUT1	PWM output1.
18	OUT2	PWM output2.
19	OUTSEN	Direct output sense.
20	OS2	Current sense input 2.

Block Diagram



Applications Information- Output Voltage

VRM9.X Output Voltage					
Unless specified: 0 = GND; 1 = High (or Floating). T_A = 25°C, V_{CC} = 12V					Vout (V)
VID4	**VID3**	**VID2**	**VID1**	**VID0**	
1	1	1	1	1	OFF
1	1	1	1	0	1.1
1	1	1	0	1	1.125
1	1	1	0	0	1.15
1	1	0	1	1	1.175
1	1	0	1	0	1.2
1	1	0	0	1	1.225
1	1	0	0	0	1.25
1	0	1	1	1	1.275
1	0	1	1	0	1.3
1	0	1	0	1	1.325
1	0	1	0	0	1.35
1	0	0	1	1	1.375
1	0	0	1	0	1.4
1	0	0	0	1	1.425
1	0	0	0	0	1.45
0	1	1	1	1	1.475
0	1	1	1	0	1.5
0	1	1	0	1	1.525
0	1	1	0	0	1.55
0	1	0	1	1	1.575
0	1	0	1	0	1.6
0	1	0	0	1	1.625
0	1	0	0	0	1.65
0	0	1	1	1	1.675
0	0	1	1	0	1.7
0	0	1	0	1	1.725
0	0	1	0	0	1.75
0	0	0	1	1	1.775
0	0	0	1	0	1.8
0	0	0	0	1	1.825
0	0	0	0	0	1.85

Applications Information- Output Voltage (Cont)

VRD10 Output Voltage

Unless specified: 0 = GND; 1 = High. T_A = 25°C, V_{CC} = 12V

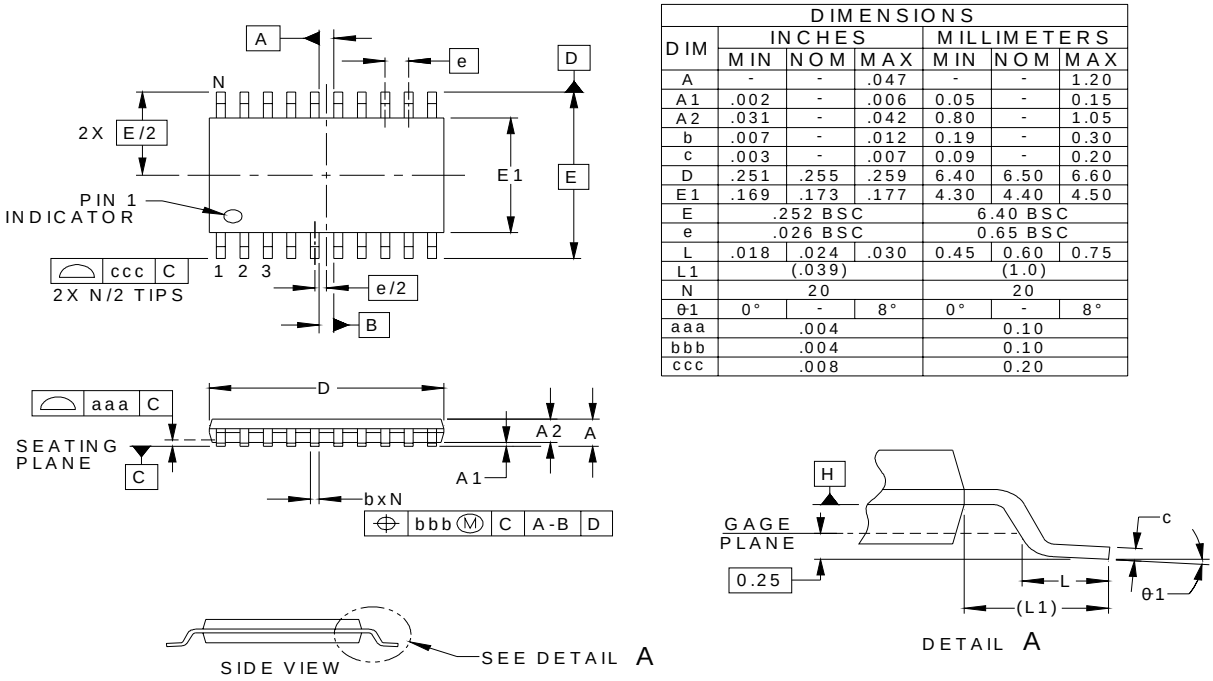
VID5	VID4	VID3	VID2	VID1	VID0	Vout (V)
0	0	1	0	1	0	0.8375
1	0	1	0	0	1	0.8500
0	0	1	0	0	1	0.8625
1	0	1	0	0	0	0.8750
0	0	1	0	0	0	0.8875
1	0	0	1	1	1	0.9000
0	0	0	1	1	1	0.9125
1	0	0	1	1	0	0.9250
0	0	0	1	1	0	0.9375
1	0	0	1	0	1	0.9500
0	0	0	1	0	1	0.9625
1	0	0	1	0	0	0.9750
0	0	0	1	0	0	0.9875
1	0	0	0	1	1	1.0000
0	0	0	0	1	1	1.0125
1	0	0	0	1	0	1.0250
0	0	0	0	1	0	1.0375
1	0	0	0	0	1	1.0500
0	0	0	0	0	1	1.0625
1	0	0	0	0	0	1.0750
0	0	0	0	0	0	1.0875
1	1	1	1	1	1	OFF
0	1	1	1	1	1	OFF
1	1	1	1	1	0	1.1000
0	1	1	1	1	0	1.1125
1	1	1	1	0	1	1.1250
0	1	1	1	0	1	1.1375
1	1	1	1	0	0	1.1500
0	1	1	1	0	0	1.1625
1	1	1	0	1	1	1.1750
0	1	1	0	1	1	1.1875
1	1	1	0	1	0	1.2000
0	1	1	0	1	0	1.2125
1	1	1	0	0	1	1.2250
0	1	1	0	0	1	1.2375
1	1	1	0	0	0	1.2500
0	1	1	0	0	0	1.2625
1	1	0	1	1	1	1.2750
0	1	0	1	1	1	1.2875
1	1	0	1	1	0	1.3000
0	1	0	1	1	0	1.3125
1	1	0	1	0	1	1.3250
0	1	0	1	0	1	1.3375
1	1	0	1	0	0	1.3500
0	1	0	1	0	0	1.3625
1	1	0	0	1	1	1.3750
0	1	0	0	1	1	1.3875
1	1	0	0	1	0	1.4000
0	1	0	0	1	0	1.4125
1	1	0	0	0	1	1.4250
0	1	0	0	0	1	1.4375
1	1	0	0	0	0	1.4500
0	1	0	0	0	0	1.4625
1	0	1	1	1	1	1.4750
0	0	1	1	1	1	1.4875
1	0	1	1	1	0	1.5000
0	0	1	1	1	0	1.5125
1	0	1	1	0	1	1.5250
0	0	1	1	0	1	1.5375
1	0	1	1	0	0	1.5500
0	0	1	1	0	0	1.5625
1	0	1	0	1	1	1.5750
0	0	1	0	1	1	1.5875
1	0	1	0	1	0	1.6000

Applications Information- Output Voltage (Cont)

K-8 Output Voltage					
Unless specified: 0 = GND; 1 = High (or Floating). T_A = 25°C, V_{CC} = 12V					
VID4	**VID3**	**VID2**	**VID1**	**VID0**	**V_{OUT} (V)**
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	OFF

POWER MANAGEMENT

Outline Drawing - TSSOP-20

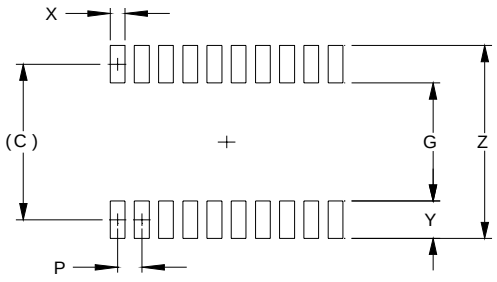


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.047	-	-	1.20
A1	.002	-	.006	0.05	-	0.15
A2	.031	-	.042	0.80	-	1.05
b	.007	-	.012	0.19	-	0.30
c	.003	-	.007	0.09	-	0.20
D	.251	.255	.259	6.40	6.50	6.60
E1	.169	.173	.177	4.30	4.40	4.50
E	.252 BSC			6.40 BSC		
e	.026 BSC			0.65 BSC		
L	.018	.024	.030	0.45	0.60	0.75
L1	(.039)			(1.0)		
N	20			20		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.004			0.10		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-153, VARIATION AC.

Land Pattern - TSSOP-20



DIM	INCHES	MILLIMETERS
C	(.222)	(5.65)
G	.161	4.10
P	.026	0.65
X	.016	0.40
Y	.061	1.55
Z	.283	7.20

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Contact Information

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