SC2620
Dual 2A, 30V Step-down Regulator with Programmable Frequency up to 1.4MHz

Description

The SC2620 is a constant frequency dual current-mode switching regulator with integrated 2.3A, 30V switches. Its switching frequency can be programmed up to 1.4MHz per channel. Due to the SC2620's high frequency operation, small inductors and ceramic capacitors can be used, resulting in very compact power supplies. The two channels of the SC2620 operate at 180° out of phase for reduced input voltage ripples.

Separate soft start/enable pins allow independent control of each channel. Channel 1 power good indicator can be used for output start up sequencing to prevent latch-up.

Current-mode PWM control achieves fast transient response with simple loop compensation. Cycle-by-cycle current limiting and hiccup overload protection reduce power dissipation during overload.

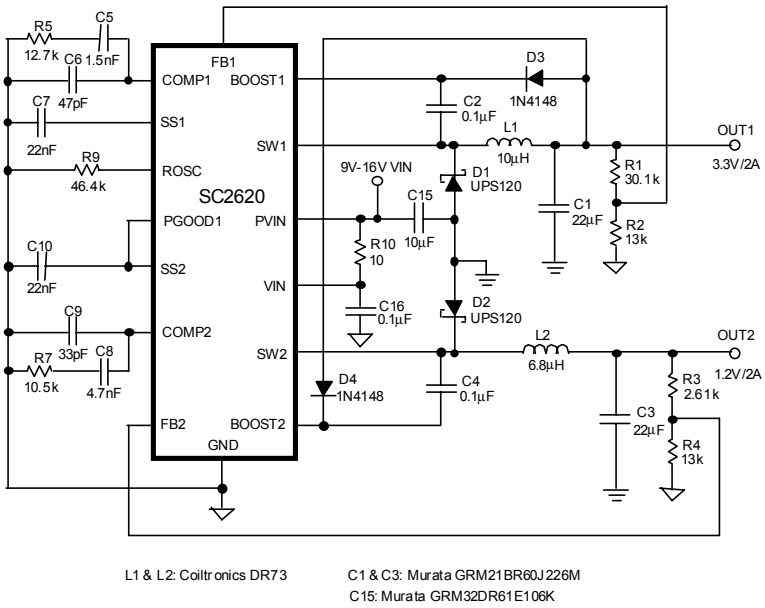
Features

- Wide Input Voltage Range 2.8V to 30V
- Up to 1.4MHz/Channel Programmable Switching Frequency
- Current-mode Control
- Out of Phase Switching Reduces Ripple
- Cycle-by-cycle Current-limiting
- Independent Shutdown/soft-start Pins
- Independent Hiccup Overload Protection
- Channel 1 Power Good Indicator
- Two 2.3A Integrated Switches
- Thermal Shutdown
- Thermally Enhanced SO-16 Lead Free Package
- Fully WEEE and RoHS Compliant

Applications

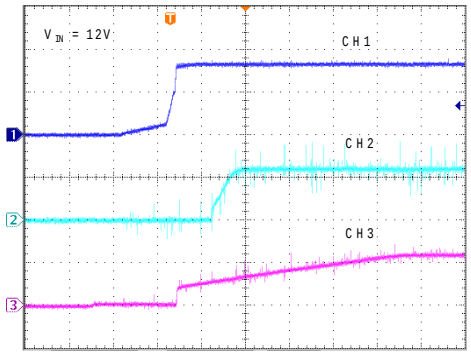
- XDSL and Cable Modems
- Set-top Boxes
- Point of Load Applications
- CPE Equipment
- DSP Power Supplies

Typical Application Circuit



L1 & L2: Coiltronics DR73 C1 & C3: Murata GRM21BR60J226M
C15: Murata GRM32DR61E106K

Figure 1(a). 550kHz 9V-16V V_{IN} to 3.3V and 1.2V Step-down Converter.



4ms/div

CH1 : OUT1 Voltage, 2V/div
CH2 : OUT2 Voltage, 1V/div
CH3 : SS2 Voltage, 2V/div

Figure 1(b). V_{IN} Start-up Transient (I_{OUT1}= 1.5A, I_{OUT2}= 0.8A). Channel 2 start is delayed until Channel 1 reaches regulation.

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Max	Units
Input Voltage	V_{IN}	-0.3 to 32	V
Boost Pin	V_{BST}	42	V
Boost Pin Above SW	V_{BST}-V_{SW}	24	V
PGOOD1 Pin Voltage	V_{PGOOD1}	V_{IN}	V
SS Pins	V_{SS}	3	V
FB Pins	V_{FB}	-0.3 to V_{IN}	V
SW Voltage	V_{SW}	-0.6 to V_{IN}	V
Thermal Resistance Junction to Ambient	θ_{JA}	31	°C/W
Thermal Resistance Junction to Case	θ_{JC}	3.9	°C/W
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering)10 sec	T_{LEAD}	300	°C
ESD Rating (Human Body Model) (Note 1)	ESD	1.5	kV

Note 1: This device is ESD sensitive. Standard ESD handling precaution is required.

Recommended Operating Conditions

The Performance is not guaranteed if exceeding the specifications below

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage Range	V_{IN}		2.8		30	V
Ambient Temperature Range	T_A		-40		105	°C
Junction Temperature	T_J		-40		125	°C

Electrical Characteristics

Unless specified: -40°C < T_J< 125°C, R_{OSC} = 12.1kΩ, V_{IN} = 5V, V_{BOOST} = 8V

Parameter	Conditions	Min	Typ	Max	Units
V_{IN} Start Voltage		2.45	2.62	2.78	V
V_{IN} Start Hysteresis			75		mV
Quiescent Current	Not switching, PGOOD1 Open		3.5	5	mA
Shutdown Current	V_{SS1}=V_{SS2}=0, PGOOD1 Open		40	60	µA
Feedback Voltage		0.980	1.000	1.020	V
Feedback Voltage Lin Regulation	Vin=3V to 30V		0.005		%/V
FB Pin Input Bias Current	V_{FB}=1V, V_{COMP}=1.5V		-15	-30	nA

Electrical Characteristics (Cont.)

Unless specified: -40°C < T_J < 125°C, R_{OSC} = 12.1kΩ, V_{IN} = 5V, V_{BOOST} = 8V

Parameter	Conditions	Min	Typ	Max	Units
Error Amplifier Transconductance			280		$\mu\Omega^{-1}$
Error Amplifier Open-Loop Gain			53		dB
COMP Source Current	V_{FB} = 0.8V, V_{COMP} = 1.5V		20		µA
COMP Sink Current	V_{FB} = 1.2V, V_{COMP} = 1.5V		20		µA
COMP Pin to Switch Current Gain			8		A/V
COMP Switching Threshold		0.7	1.1	1.3	V
COMP Maximum Voltage	V_{FB} = 0.9V		2.4		V
Channel Switching Frequency		1.2	1.4	1.6	MHz
Maximum Duty Cycle	(Note 3)	80	90		%
Switch Current Limit	(Notes 2 and 4)	2.3	3.2		A
Switch Saturation Voltage	I_{SW} = -2A		0.3		V
Switch Leakage Current				10	µA
Minimum Boost Voltage	I_{SW} = -2A (Note 2)		1.8	2.5	V
Boost Pin Current	I_{SW} = -0.5A		20		mA
	I_{SW} = -2A		60		mA
Minimum Soft-Start Voltage to Exit Shutdown	SS1 Tied to SS2	0.2	0.4	0.7	V
Soft-start Charging Current	V_{SS} = 0V		2		µA
	V_{SS} = 1.5V		1.8		µA
Soft-start Discharging Current	V_{SS} = 1.5V		0.8		µA
Minimum Soft-start Voltage to Enable Overload Shutoff	V_{SS} Rising		2		V
FB Overload Threshold	V_{SS} = 2.3V, V_{FB} Falling		0.7		V
Soft-start Voltage to Restart Switching After Overload Shutoff	V_{SS} Falling	0.7	1	1.3	V
Power Good Threshold Below FB1	V_{FB1} Rising	80	100	120	mV
Power Good Output Low Voltage	V_{FB1} = 0.8V, I_{PGOOD1} = 250µA		0.2	0.4	V
Power Good Pin Leakage Current	V_{PGOOD1} = 5V		0.1	1	µA
Thermal Shutdown Temperature			155		°C
Thermal Shutdown Hysteresis			10		°C

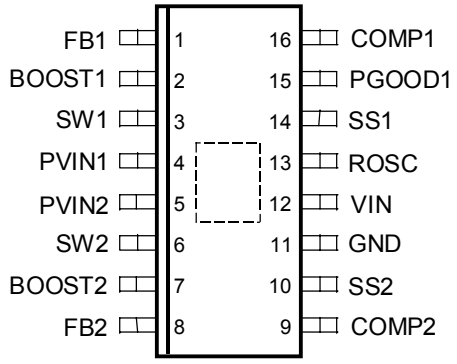
Note 2: Guaranteed by design, not 100% tested in production.

Note 3: The maximum duty cycle specified corresponds to 1.4MHz switching frequency. Duty cycles higher than those specified can be achieved by lowering the operating frequency.

Note 4: Switch current limit does not vary with duty cycle.

Pin Configuration

TOP VIEW



(16 Pin SOIC-EDP)
Underside metal must be soldered to ground.

Ordering Information

Part Number	Package
SC2620SETRT[1][2]	SOIC-16 EDP
SC2620EVB	Evaluation Board

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin #	Pin Name	Pin Function
1, 8	FB1, FB2	The inverting inputs of the error amplifiers. Each FB pin is tied to a resistive divider between its output and ground to set the channel output voltage.
2, 7	BOOST1, BOOST2	Supply pins to the power transistor drivers. Tie to external diode-capacitor charge pumps to generate drive voltages higher than V_{IN} in order to fully enhance the internal NPN power switches.
3, 6	SW1, SW2	Emitters of the internal power NPN transistors. Each SW pin is connected to the corresponding inductor, freewheeling diode and bootstrap capacitor.
4, 5	PVIN1, PVIN2	Collectors of the internal power transistors and the power supplies to the corresponding current sensing circuits. Pins 4 and 5 are not internally connected. They must be joined on the PCB and closely bypassed to the power ground plane.
9, 16	COMP1, COMP2	Outputs of the internal error amplifiers. The voltages at these pins control the peak switch currents. RC networks at these pins stabilize the control loops. Pulling either pin below 0.7V stops the corresponding switching regulator.
10, 14	SS1, SS2	A capacitor from either SS pin to ground provides soft-start and overload hiccup functions for that channel. Pulling either SS pin below 0.8V with an open drain or collector transistor shuts off the corresponding regulator. To completely shut off the SC2620 to low-current state, pull both SS pins to ground. Soft-start is recommended for all applications.
11	GND	Analog ground. Connect to the PCB power ground plane at a single point.
12	VIN	Power supply to the analog control section of the SC2620. Connect to the PVIN pins through an optional RC filter.
13	ROSC	An external resistor between this pin and the analog ground sets the channel switching frequency.
15	PGOOD1	Open collector output of Channel 1 power good comparator. Tie to an external pull-up resistor from the input or the output of the converter. PGOOD1 output becomes valid as soon as V_{IN} rises above 1 V_{BE} during power-up. PGOOD1 is actively pulled low until FB1 voltage rises to within 10% of its final regulation voltage.
Underside Metal		The exposed pad at the bottom of the package is electrically connected to the ground pin of the SC2620. It also serves as a thermal contact to the circuit board. It is to be soldered to the analog ground plane of the PC board.

Block Diagrams

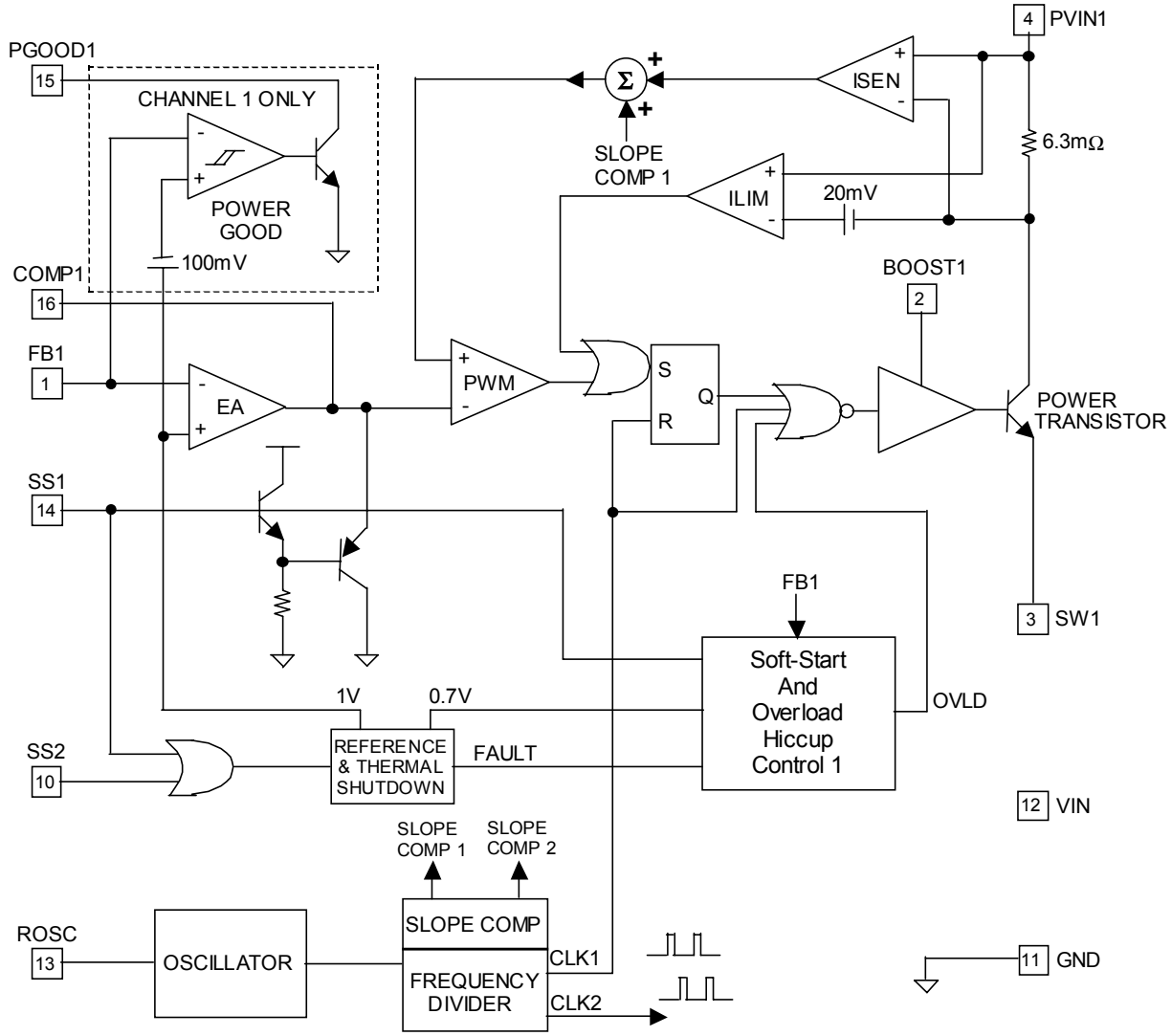


Figure 2. SC2620 Block Diagram (Channel 1)

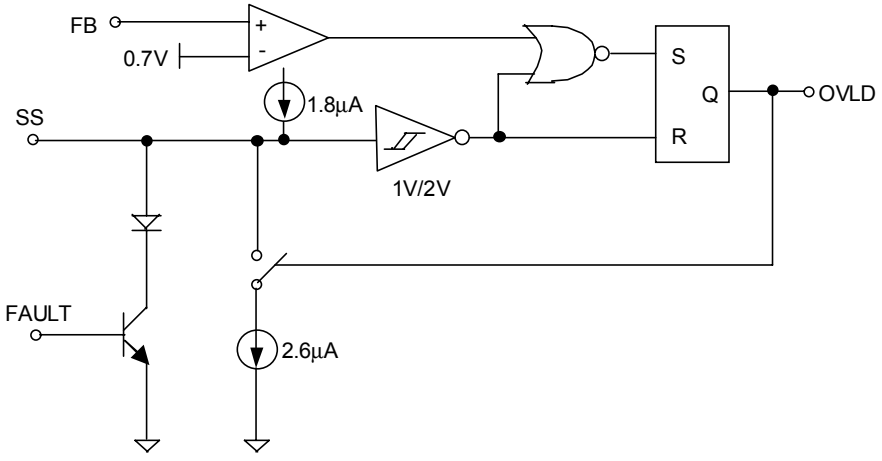
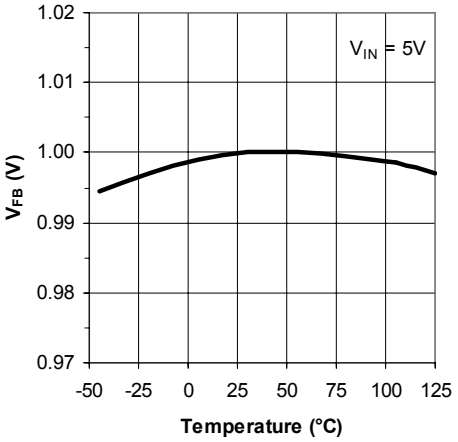


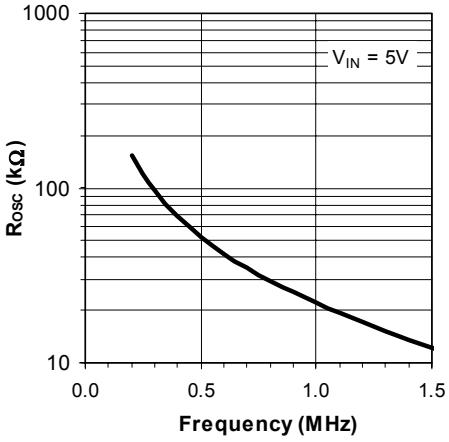
Figure 3. Details of the Soft-Start and Overload Hiccup Control Circuit

Typical Characteristics

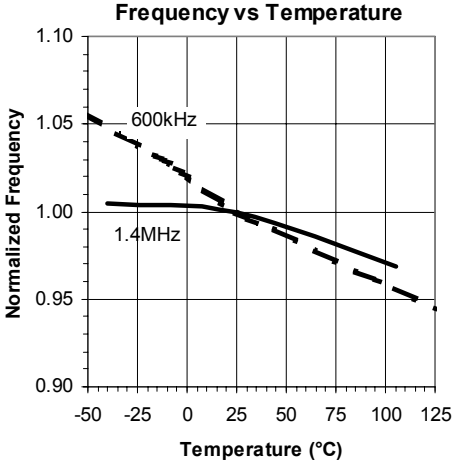
Feedback Voltage vs Temperature



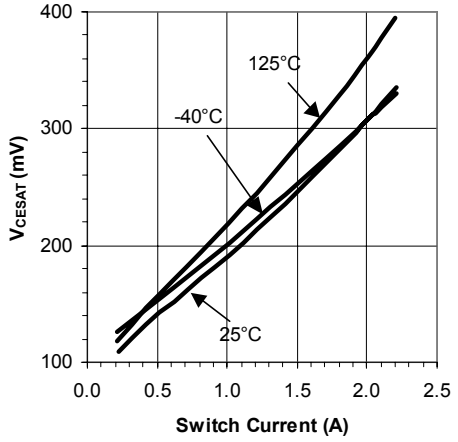
Frequency Setting Resistor vs Channel Frequency



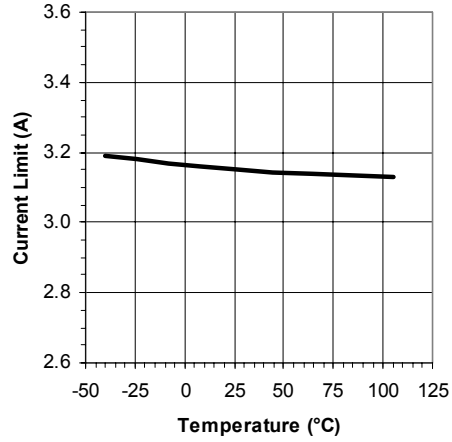
Normalized Channel Frequency vs Temperature



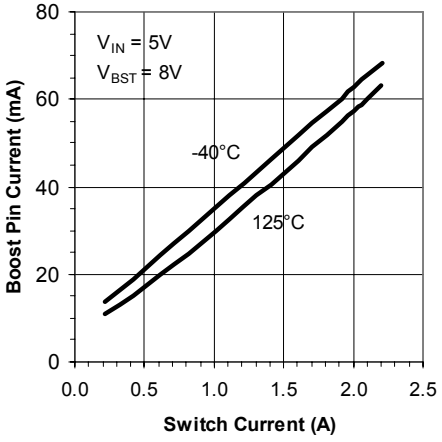
Switch Saturation Voltage vs Switch Current



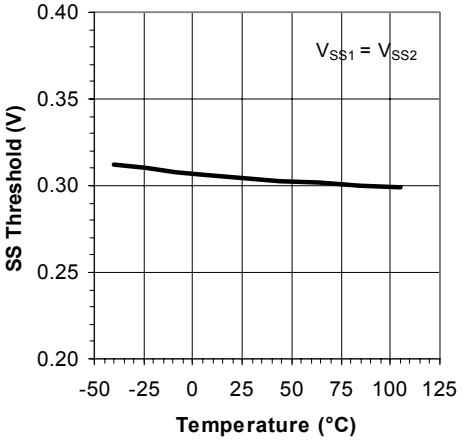
Switch Current Limit vs Temperature



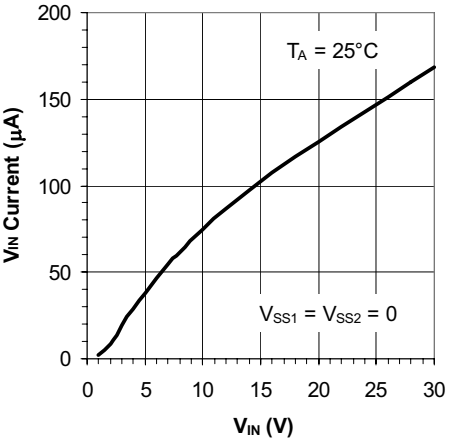
Boost Pin Current vs Switch Current



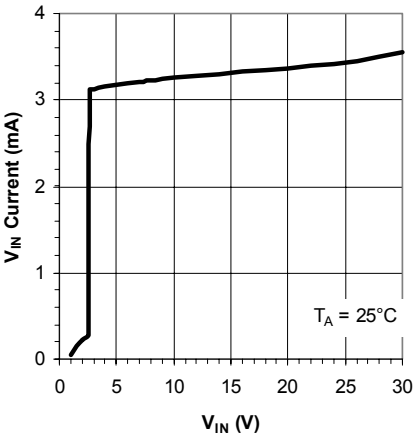
SS Shutdown Threshold vs Temperature



V_{IN} Shutdown Current vs V_{IN}

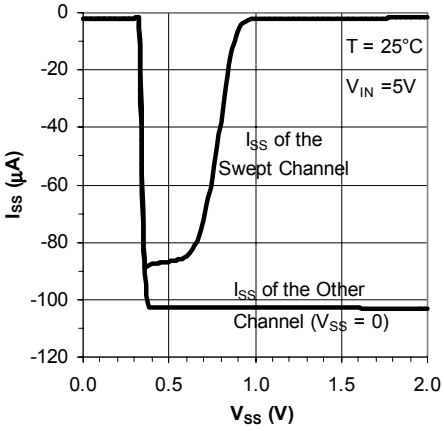


V_{IN} Quiescent Current vs V_{IN}

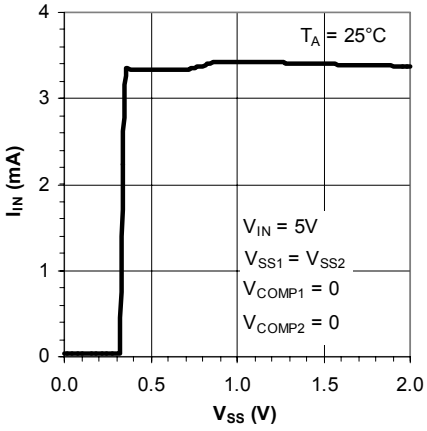


Typical Characteristics

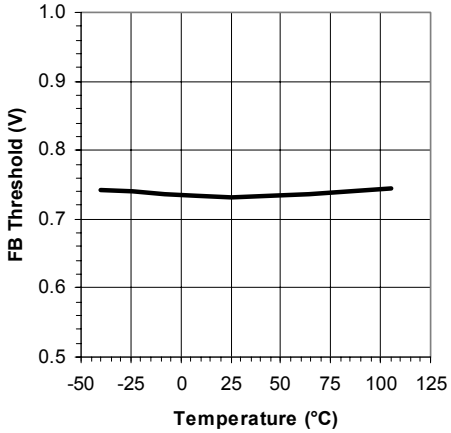
Soft-Start Pin Current vs Soft-Start Voltage



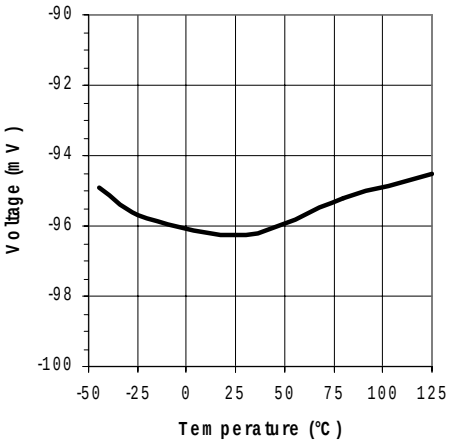
V_{IN} Supply Current vs Soft-Start Voltage



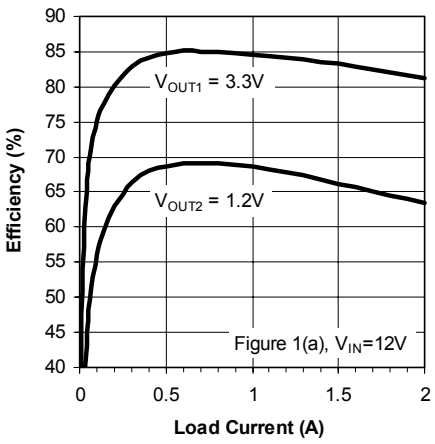
FB Overload Threshold vs Temperature



PGOOD1 Threshold to V_{FB} Difference Voltage vs Temperature



Efficiency vs Load Current



Operation

The SC2620 is a 30V 2-channel constant-frequency peak current-mode step-down switching regulator with integrated 2.3A power transistors. Both regulators in the SC2620 operate from a common input power supply and share the same voltage reference and the master oscillator. Turn-on of the power transistors is phase-shifted by 180°. The two regulator cores are otherwise completely identical, independent and are capable of producing two separate outputs from the same input.

The channel frequency can be programmed with an external resistor from the ROSC pin to ground. This allows the designer to set the switching frequency according to the input to the output voltage conversion ratio.

Peak current-mode control is utilized for the SC2620. The double reactive poles of the output LC filter are reduced to a single real pole by the inner current loop, easing loop compensation. Fast transient response can be achieved with a simple Type-2 compensation network. Switch collector current is sensed with an integrated 6.3mΩ sense resistor. The sensed current is summed with slope-compensating ramp before it is compared with the transconductance error amplifier output. The PWM comparator tripping point determines the switch turn-on pulse width (Figure 2). The current-limit comparator ILIM turns off the power switch when the sensed-signal exceeds the 20mV current-limit threshold. ILIM therefore provides cycle-by-cycle limit. Current-limit does not vary with duty-cycle.

An external charge pump (formed by the capacitor C_2 and the diode D_3 in Figure 1(a)) generates a voltage higher than the input rail at the BOOST pin. The bootstrapped voltage generated becomes the supply voltage for the power transistor driver. Driving the base of the power transistor above the input power supply rail minimizes the power transistor turn-on voltage and maximizes efficiency.

The SS pin is a multiple-function pin. An external capacitor connected from the SS pin to ground together with the internal 1.8µA and 2.6µA current sources set the soft-start and overload shutoff times of the regulator (Figure 3). The SS pin can also be used to shut off the corresponding regulator. When either SS pin is pulled below 0.8V, that regulator is turned off. If both SS pins are pulled below 0.2V, then the SC2620 undergoes overall shutdown. The current drawn from the input power supply reduces to 40µA. When either SS pin is released, the corresponding soft-start capacitor is charged with a 2µA current source (not shown in Figure 3). As either SS voltage exceeds 0.3V, the internal bias circuit of the SC2620 is enabled. The SC2620 draws 3.5mA from V_{IN}. An internal fast charge circuit quickly charges the soft-start capacitor to 1V. At this juncture, the fast charge circuit turns off and the 1.8µA current source slowly charges the soft-start capacitor. The output of the error amplifier is forced to track the slow soft-start ramp at the SS pin. When the COMP voltage exceeds 1.1V, the switching regulator starts to switch. During soft-start, the current limit of the converter is gradually increased until the converter output comes into regulation.

Hiccup overload protection is utilized in the SC2620. Overload shutdown is disabled during soft-start (V_{SS} < 2V). In Figure 3 the reset input of the overload latch will remain high if the SS voltage is below 2V. Once the soft-start capacitor is charged above 2V, the overload shutdown latch is enabled. As the load draws more current from the regulator, the current-limit comparator will limit the peak inductor current. This is cycle-by-cycle current limiting. Further increase in load current will cause the output voltage to decrease. If the output voltage falls below 70% of its set point, then the overload latch will be set and the soft-start capacitor will be discharged with a net current of 0.8µA. The switching regulator is shut off until the soft-start capacitor is discharged below 1V. At this moment, the overload latch is reset. The soft-start capacitor is recharged and the converter again undergoes soft-start. The regulator will go through soft-start, overload shutdown and restart until it is no longer overloaded.

The power good comparator indicates that the channel 1 regulator output has risen to within 10% of its set value. The open collector output of the power good comparator will be actively pulled low if its feedback voltage is below 0.9V.

Applications Information

Setting the Output Voltage

The regulator output voltage is set with an external resistive divider (Figure 4) with its center tap tied to the FB pin.

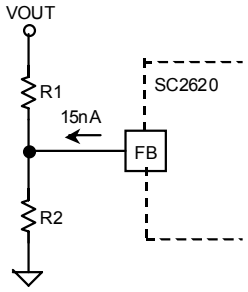


Figure 4. V_{OUT} is set with a Resistive Divider

$$R_1 = R_2(V_{OUT} - 1) \quad (1)$$

The percentage error due the input bias current of the error amplifier is

$$\frac{\Delta V_{OUT}}{V_{OUT}} = \frac{-15nA \cdot 100 \cdot (R_1 || R_2)}{1V}.$$

Example: Determine the output voltage error of a $V_{OUT} = 5V$ converter with $R_2 = 51.1k\Omega$.

From (1),

$$R_1 = 51.1k\Omega \cdot (5 - 1) = 205k\Omega$$

$$\frac{\Delta V_{OUT}}{V_{OUT}} = \frac{-15nA \cdot 100 \cdot (51.1k || 205k)}{1V} = -0.061\%.$$

This error is at least an order of magnitude lower than the ratio tolerance resulting from the use of 1% resistors in the divider string.

Setting the Channel Frequency

The switching frequency of the master oscillator is set with an external resistor from the ROSC pin to ground. Channel frequency is one-half of that of the master oscillator. A graph of channel frequency against R_{OSC} is shown in the "Typical Performance Characteristics". Channel frequency is programmable up to 1.4MHz.

Channel switching frequency is limited by the minimum controllable on time at low duty cycles. For V_{IN} > 20V, setting the switching frequency below 500kHz makes converter output short circuit operation more robust. These will be described in more details later.

Minimum On Time Consideration

The operating duty cycle of a non-synchronous step-down switching regulator in continuous-conduction mode (CCM) is given by

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_{CESAT}} \quad (2)$$

where V_{CESAT} is the switch saturation voltage and V_D is voltage drop across the rectifying diode.

Duty cycle decreases with increasing $\frac{V_{IN}}{V_{OUT}}$ ratio. In peak current-mode control, the PWM modulating ramp is the sensed current ramp of the power switch. This current ramp is absent unless the switch is turned on. The intersection of this ramp with the output of the voltage feedback error amplifier determines the switch pulse width. The propagation delay time required to immediately turn off the switch after it is turned on is the minimum controllable switch on time ($T_{ON(MIN)}$). Closed-loop measurement of the SC2620 with low $\frac{V_{OUT}}{V_{IN}}$ ratios shows

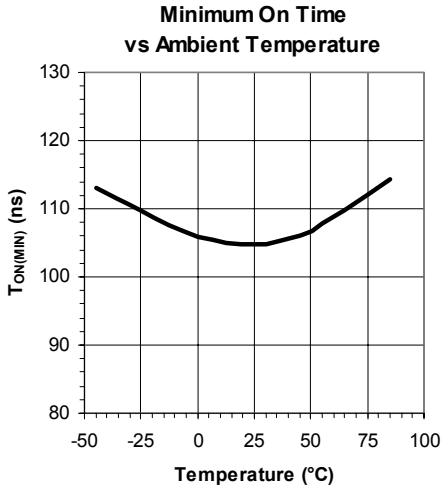


Figure 5. Variation of Minimum On Time with Ambient Temperature.

that the minimum on time is about 105ns at room temperature (Figure 5). The power switch in the SC2620 is either not turned on at all or for at least $T_{ON(MIN)}$. If the required switch on time ($=\frac{D}{f}$) is shorter than the minimum on time, the regulator will either skip cycles or it will jitter.

Example: Determine the maximum operating frequency of a dual 24V to 1.2V and 24V to 3.3V switching regulator using the SC2620.

Assuming that V_D = 0.45V, V_{CESAT} = 0.25V and V_{IN} = 26.4V (10% high line), the corresponding duty ratios, D_1 and D_2, of the 1.2V and 3.3V converters can be calculated using (2).

$$D_1 = \frac{1.2 + 0.45}{26.4 + 0.45 - 0.25} = 0.062$$

$$D_2 = \frac{3.3 + 0.45}{26.4 + 0.45 - 0.25} = 0.14$$

To allow for transient headroom, the minimum operating switch on time should be at least 30% higher than the worst-case minimum on time exhibited in Figure 5. Designing for a switch on time of 150ns at $V_{IN} = 26.4V$, the maximum operating frequency of the 24V to 1.2V and 3.3V converter is $\frac{D_1}{150ns} = 410kHz$.

Minimum Off Time Limitation

The PWM latch in Figure 2 is reset every period by the clock. The clock also turns off the power transistor to refresh the bootstrap capacitor. This minimum off time limits the attainable duty cycle of the regulator at a given switching frequency. The measured minimum off time is 120ns. For a step-down converter, D increases with increasing $\frac{V_{OUT}}{V_{IN}}$ ratio. If the required duty cycle is higher than the attainable maximum, then the output voltage will not be able to reach its set value in continuous-conduction mode.

Example: Determine the maximum operating frequency of a dual 5V to 1.5V and 5V to 4V switching regulator using the SC2620.

Assuming that V_D = 0.45V, V_{CESAT} = 0.25V and V_{IN} = 4.5V (10% low line), the duty ratios D_1 and D_2 of the 1.5V and 4V converters can be calculated using (2).

$$D_1 = \frac{1.5 + 0.45}{4.5 + 0.45 - 0.25} = 0.42$$

$$D_2 = \frac{4 + 0.45}{4.5 + 0.45 - 0.25} = 0.95.$$

The maximum operating channel frequency of the dual 1.5V and the 4V converter is therefore $\frac{1 - D_2}{120ns} = 410kHz$.

Transient headroom requires that channel frequency be lower than 410kHz.

Inductor Selection

The inductor ripple current ΔI_L for a non-synchronous step-down converter in continuous-conduction mode is

$$\Delta I_L = \frac{(V_{OUT} + V_D)(1 - D)}{fL} = \frac{(V_{OUT} + V_D)(V_{IN} - V_{OUT} - V_{CESAT})}{(V_{IN} + V_D - V_{CESAT})fL} \quad (3)$$

where f is the switching frequency and L is the inductance.

In current-mode control, the slope of the modulating (sensed switch current) ramp should be steep enough to lessen jittery tendency but not so steep that large flux swing decreases efficiency. Inductor ripple current ΔI_L between 25-40% of the peak inductor current limit is a good compromise. Inductors so chosen are optimized in size and DCR. Setting $\Delta I_L = 0.3(2.3) = 0.69A$, $V_D = 0.45V$ and $V_{CESAT} = 0.25V$ in (3),

$$L = \frac{(V_{OUT} + 0.45)(V_{In} - V_{OUT} - 0.25)}{(V_{IN} + 0.2)(0.69)f} \quad (4)$$

where L is in µH and f is in MHz.

Equation (3) shows that for a given V_{OUT}, ΔI_L increases as D decreases. If V_{IN} varies over a wide range, then choose L based on the nominal input voltage. Always verify converter operation at the input voltage extremes.

The peak current limits of both SC2620 power transistors are internally set at 3.2A. The peak current limits are duty-cycle invariant and are guaranteed higher than 2.3A. The maximum load current is therefore conservatively:

$$I_{OUT(MAX)} = I_{LM} - \frac{\Delta I_L}{2} = 2.3A - \frac{\Delta I_L}{2} \quad (5)$$

If $\Delta I_L = 0.3 \cdot I_{LM}$, then

$$I_{OUT(MAX)} = I_{LM} - \frac{\Delta I_L}{2} = I_{LM} - \frac{0.3 I_{LM}}{2} = 0.85 \cdot I_{LM}.$$

The saturation current of the inductor should be 20-30% higher than the peak current limit (2.3A). Low-cost powder iron cores are not suitable for high-frequency switching power supplies due to their high core losses. Inductors with ferrite cores should be used.

Power Line Input Capacitor

A buck converter draws pulse current with peak-to-peak amplitude equal to its output current I_{OUT} from its input supply. An input capacitor placed between the supply and the buck converter filters the AC current and keeps the current drawn from the supply to a DC constant. The input capacitance C_{IN} should be high enough to filter the pulse input current. Its equivalent series resistance (ESR) should be low so that power dissipated in the capacitor does not result in significant temperature rise and degrade reliability. For a single channel buck converter, the RMS ripple current in the input capacitor is

$$I_{RMS(CIN)} = I_{OUT}\sqrt{D(1-D)}. \quad (6)$$

Power dissipated in the input capacitor is $I^2_{RMS(CIN)} \cdot (ESR)$.

Equation (6) has a maximum value of $\frac{I_{OUT}}{2}$ (at $D = \frac{1}{2}$), corresponding to the worst-case power dissipation $\frac{I^2_{OUT} \cdot ESR}{4}$ in C_{IN}.

A dual-channel step-down converter with interleaved switching reduces the RMS ripple current in the input capacitor to a fraction of that of a single-phase buck converter. If both power transistors in the SC2620 were to switch on in phase, the current drawn by the SC2620 would consist of current pulses with amplitude equal to the sum of the channel output currents. If each channel were delivering I_{OUT} and operating at 50% duty cycle, then the input current would switch from zero to $2I_{OUT}$. The RMS ripple current in the input capacitor would then be I_{OUT}. Power dissipated in C_{IN} would be $I^2_{OUT} \cdot ESR$, 4 times that of a single-channel converter. The SC2620 produces the highest RMS ripple current in C_{IN} when only one channel is running and delivering the maximum output current (2A). The input capacitor therefore should have a RMS ripple current rating of at least 1A.

Multi-layer ceramic capacitors, which have very low ESR (a few mΩ) and can easily handle high RMS ripple current, are the ideal choice for input filtering. A single 4.7µF or 10µF X5R ceramic capacitor is adequate. For high voltage applications, a small ceramic (1µF or 2.2µF) can be placed in parallel with a low ESR electrolytic capacitor to satisfy both the ESR and bulk capacitance requirements.

Output Capacitor

The output ripple voltage ΔV_{OUT} of a buck converter can be expressed as

$$\Delta V_{OUT} = \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right) \quad (7)$$

where C_{OUT} is the output capacitance.

Inductor ripple current ΔI_L increases as D decreases (Equation (3)). The output ripple voltage is therefore the highest when V_{IN} is at its maximum. The first term in (7) results from the ESR of the output capacitor while the

second term is due to the charging and discharging of C_{OUT} by the inductor ripple current. Substituting ΔI_L = 0.69A, f = 500kHz and C_{OUT} = 22µF ceramic with ESR = 2mΩ in (7),

$$\Delta V_{OUT} = 0.69A \cdot (2m\Omega + 11.4m\Omega)$$
$$= 1.4mV + 7.8mV = 9.2mV$$

Depending on operating frequency and the type of capacitor, ripple voltage resulting from charging and discharging of C_{OUT} may be higer than that due to ESR. A 10µF to 47µF X5R ceramic capacitor is found adequate for output filtering in most applications. Ripple current in the output capacitor is not a concern because the inductor current of a buck converter directly feeds C_{OUT}, resulting in very low ripple current. Avoid using Z5U and Y5V ceramic capacitors for output filtering because these types of capacitors have high temperature and high voltage coefficients.

Freewheeling Diode

Use of Schottky barrier diodes as freewheeling rectifiers reduces diode reverse recovery input current spikes, easing high-side current sensing in the SC2620. These diodes should have an average forward current rating between 1A and 2A and a reverse blocking voltage of at least a few volts higher than the input voltage. For switching regulators operating at low duty cycles (i.e. low output voltage to input voltage conversion ratios), it is beneficial to use freewheeling diodes with somewhat higher average current ratings (thus lower forward voltages). This is because the diode conduction interval is much longer than that of the transistor. Converter efficiency will be improved if the voltage drop across the diode is lower.

The freewheeling diodes should be placed close to the SW pins of the SC2620 to minimize ringing due to trace inductance. 10BQ015, 20BQ030 (International Rectifier), MBRM120LT3 (ON Semi), UPS120 and UPS140 (Micro-Semi) are all suitable.

Bootstrapping the Power Transistors

To maximize efficiency, the turn-on voltage across the internal power NPN transistors should be minimized. If these transistors are to be driven into saturation, then their bases will have to be driven from a power supply higher in voltage than V_{IN}. The required driver supply voltage (at least 2.5V higher than the SW voltage over the industrial temperature range) is generated with a bootstrap circuit (the diode D_{BST} and the capacitor C_{BST} in Figure 7). The bootstrapped output (the common node between D_{BST} and C_{BST}) is connected to the BOOST pin of the SC2620. The power transistor in the SC2620 is first switched on to build up current in the inductor. When the transistor is switched off, the inductor current pulls the SW node low, allowing C_{BST} to be charged through D_{BST}. When the power switch is again turned on, the SW voltage goes high. This brings the BOOST voltage to $V_{SW} + V_{C_{BST}}$, thus back-biasing D_{BST}. C_{BST} voltage increases with each subsequent switching cycle, as does the bootstrapped voltage at the BOOST pin. After a number of switching cycles, C_{BST} will be fully charged to a voltage approximately equal to that applied to the anode of D_{BST}. Figure 6 shows the typical minimum BOOST to SW voltage required to fully saturate the power transistor. This differential voltage ($= V_{C_{BST}}$) must be at least 1.8V at room temperature. This is also specified in the "Electrical Characteristics" as "Minimum Bootstrap Voltage". The minimum required $V_{C_{BST}}$ increases as temperature decreases. The bootstrap circuit reaches equilibrium when the base charge drawn from C_{BST} during transistor on time is equal to the charge replenished during the off interval.

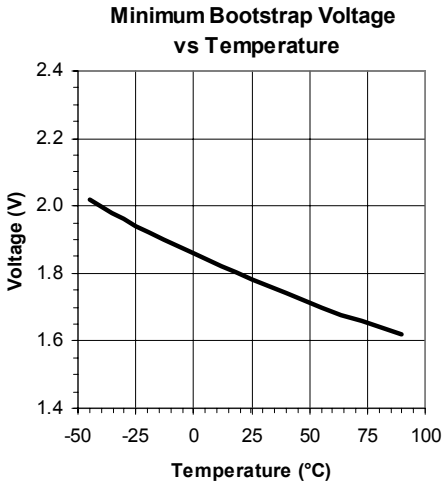


Figure 6. Typical Minimum Bootstrap Voltage Required to Maintain Saturation at I_{SW} = 2A.

Applications Information

The switch base current $= \frac{I_{SW}}{\beta+1} \approx \frac{I_{SW}}{\beta}$, where I_{SW} and β are the switch emitter current and current gain respectively, is drawn from the bootstrap capacitor C_{BST}. Charge $\frac{I_{SW}T_{ON}}{\beta}$ is drawn from C_{BST} during the switch on time, resulting in a voltage droop of $\frac{I_{SW}T_{ON}}{\beta C_{BST}}$. If I_{SW} = 2A, T_{ON} = 1µs, $\beta = 35$ and C_{BST} = 0.1µF, then the $V_{C_{BST}}$ droop will be 0.57V. C_{BST} is refreshed to $V_A - V_{D_{BST}} + V_{D_{RECT}}$ every cycle, where V_A is the applied D_{BST} anode voltage. Switch base current discharges the bootstrap capacitor to $V_A - V_{D_{BST}} + V_{D_{RECT}} - \frac{I_{SW}T_{ON}}{\beta C_{BST}}$ at the end of conduction. This voltage must be higher than the minimum shown in Figure 6 to ensure full switch enhancement. D_{BST} can be tied either to the input or to the output of the DC/DC converter.

If D_{BST} is tied to the input, then the charge drawn from the

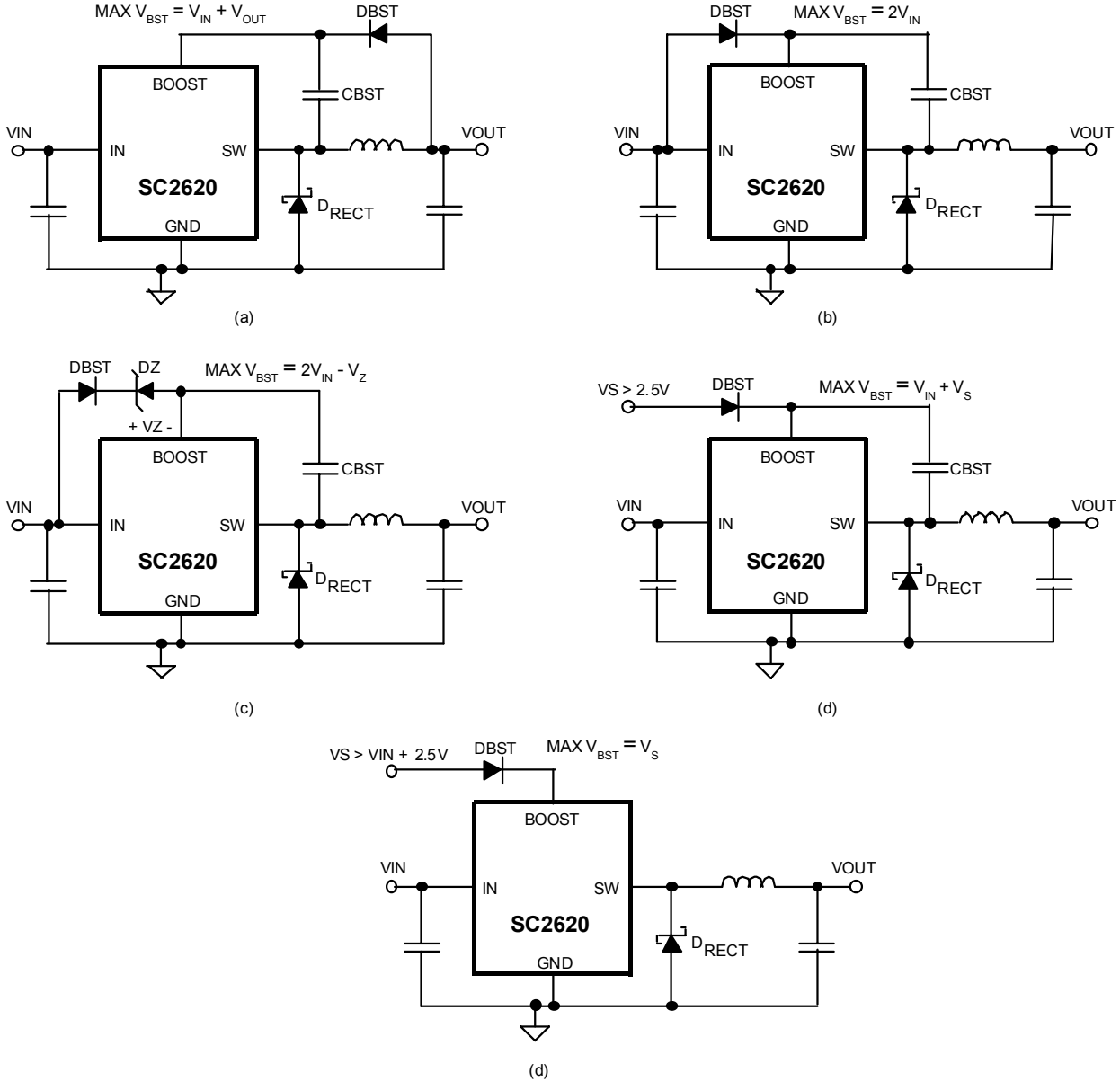


Figure 7. Methods of Bootstrapping the SC2620.

input power supply will be $\frac{I_{SW}T_{ON}}{\beta}$ (the base charge of the switch). The energy loss due to base charge per cycle is $\frac{I_{SW}V_{IN}T_{ON}}{\beta}$ for a power loss of $\frac{DI_{SW}V_{IN}}{\beta} \approx \frac{I_{SW}V_{OUT}}{\beta}$.

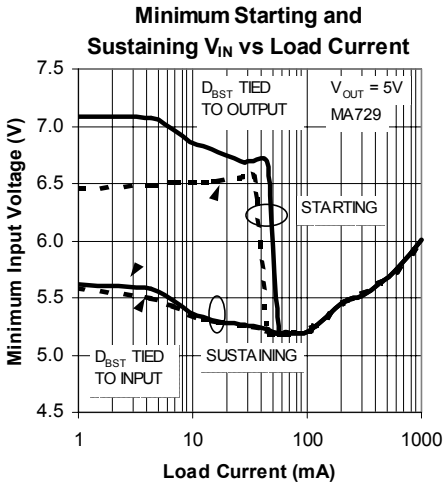
If D_{BST} is tied to the output, then the charge drawn from the output capacitor will still be $\frac{I_{SW}T_{ON}}{\beta}$. The energy loss due to base charge per cycle is $\frac{I_{SW}V_{OUT}T_{ON}}{\beta}$ for a power loss of $\frac{DI_{SW}V_{OUT}}{\beta}$.

Since $V_{OUT} < V_{IN}$, D_{BST} should always be tied to V_{OUT} (if >2.5V) to maximize efficiency. In general efficiency penalty increases as D decreases.

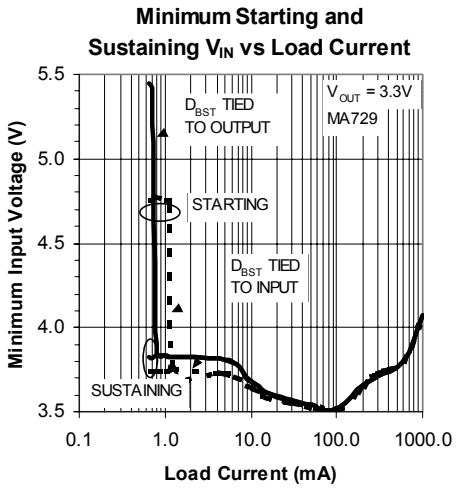
Figure 7 summarizes various ways of bootstrapping the SC2620. A fast switching PN diode (such as 1N4148 or 1N914) and a small (0.1µF – 0.47µF) ceramic capacitor can be used. In Figure 7(a) the power switch is bootstrapped from the output. This is the most efficient configuration and it also results in the least voltage stress at the BOOST pin. The maximum BOOST pin voltage is about $V_{IN}+V_{OUT}$. If the output is below 2.8V, then D_{BST} will preferably be a small Schottky diode (such as BAT-54) to maximize bootstrap voltage. A 0.33-0.47µF bootstrap capacitor may be needed to reduce droop. Bench measurement shows that using Schottky bootstrapping diode has no noticeable efficiency benefit.

The SC2620 can also be bootstrapped from the input (Figure 7(b)). This configuration is not as efficient as Figure 7(a). However this may be only option if the output voltage is less than 2.5V and there is no other supply with voltage higher than 2.5V. Voltage stress at the BOOST pin can be somewhat higher than $2V_{IN}$. The Zener diode in Figure 7(c) reduces the maximum BOOST pin voltage. The BOOST pin voltage should not exceed its absolute maximum rating of 42V.

Figures 7(d) and (e) show how to bootstrap the SC2620 from a second power supply V_S with voltage > 2.5V. V_S in Figure 7(d) can be the output of the other channel. Figures 1(a), 17(a) and 18(a) show this bootstrapping method. If Channel 1 fails in these converters, Channel 2 will be shut off (See **Sequencing the Outputs**). Proper bootstrapping of Channel 2 therefore depends on the readiness of V_{OUT1}. This may be a drawback in some applications. D_{BST} in Figure 7(e) prevents start up difficulty if V_{IN} comes up before V_S.



(a)



(b)

Figure 8. Minimum Input Voltage Required to Start and to Maintain Bootstrap.(T_A = 25°C).

Since the inductor current charges C_{BST}, the bootstrap circuit requires some minimum load current to get going. Figures 8(a) and 8(b) show the dependence of the minimum input voltage required to properly bootstrap a 5V and a 3.3V converters on the load current. Once started the bootstrap circuit is able to sustain itself down to zero load.

Shutdown and Soft-Start

Each regulating channel of the SC2620 has its own soft-start circuit. Pulling its soft-start pin below 0.8V with an open-collector NPN or an open-drain NMOS transistor turns off the corresponding regulator. The other regulator continues to operate. With one channel turned off, the internal bias circuit is kept alive. In the "Typical Characteristics", the soft-start pin current is plotted against the soft-start voltage with V_{IN} = 5V. When one of the soft-start pins is pulled low, 105µA flows out of that pin. Pulling both soft-start pins below 0.2V shuts off the internal bias circuit of the SC2620. The total V_{IN} current decreases to 40µA. In shutdown either SS pin sources only 2µA. A fast charging circuit (enabled by the internal bias circuit), which charges the soft-start capacitor below 1V, causes the difference in the soft-start pin currents.

If either SS pin is released in shutdown, the internal current source pulls up on the SS pin. When this SS voltage reaches 0.3V, the SC2620 turns on and the V_{IN} quiescent current

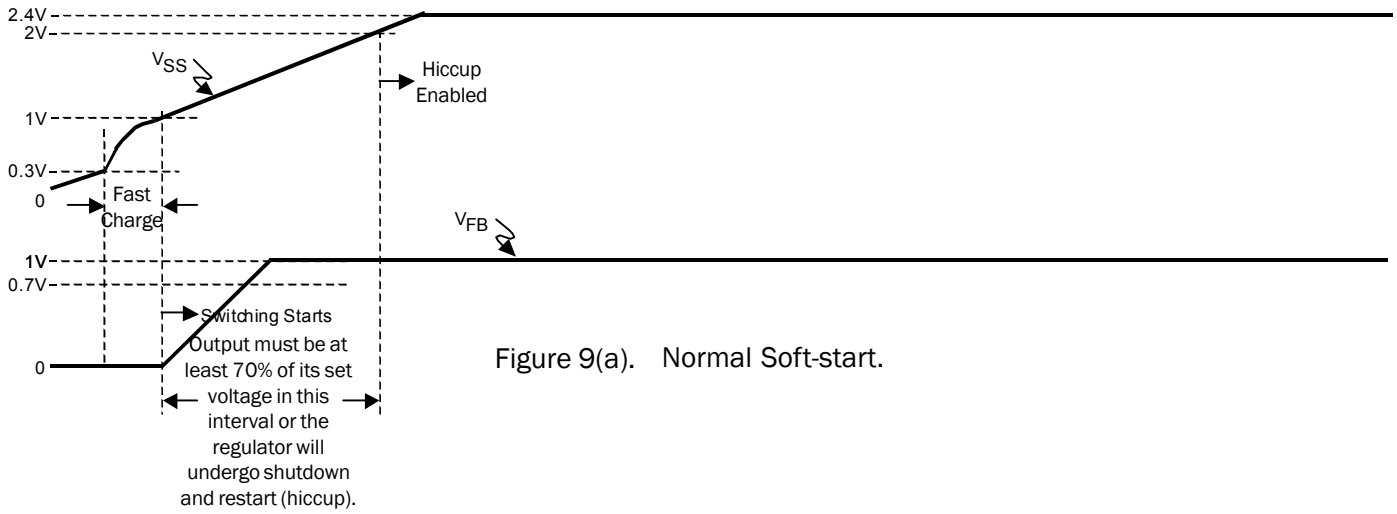


Figure 9(a). Normal Soft-start.

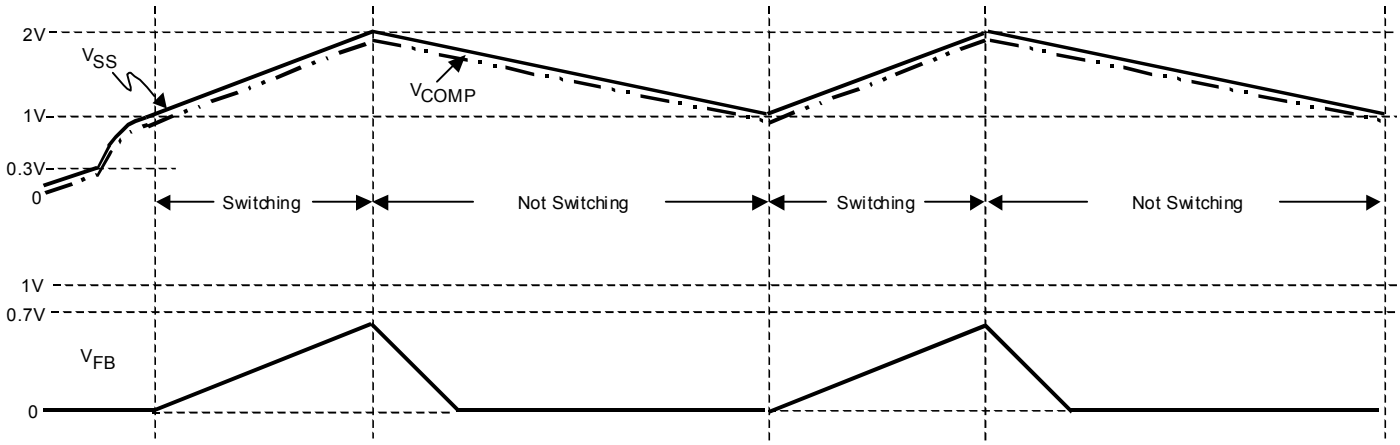


Figure 9(b). Start-up Fails due to (i) Short Soft-start Duration or (ii) Output Overload or (iii) Output Short-circuited.

increases to 3.3mA. The current flowing out of the other SS pin (which is still pulled low) increases to 105µA. The fast charging circuit quickly pulls the released soft-start capacitor to 1V (slightly below the switching threshold). The fast charging circuit is then disabled. A 1.8µA current source continues to charge the soft-start capacitor (Figure 3). The soft-start voltage ramp at the SS pin clamps the error amplifier output (Figure 2). During regulator start-up, COMP voltage follows the SS voltage. The converter starts to switch when its COMP voltage exceeds 1.1V. The peak inductor current gradually increases until the converter output comes into regulation. Proper soft-start prevents output overshoot during start-up. Current drawn from the input supply is also well controlled. Notice that the inductor current, not the converter output voltage, is ramped during soft-start.

Both soft-start capacitors are charged to a final voltage of about 2.4V.

Overload / Short-Circuit Protection

Each current limit comparator in the SC2620 limits the peak inductor current to 3.2A (typical). The regulator output voltage will fall if the load is increased above the current limit. If overload is detected (the output voltage falls below 70% of the set voltage), then the regulator will be shut off. An internal 0.8µA current sink starts to discharge the soft-start capacitor. As the soft-start capacitor is discharged below 1V, the discharge current source turns off and the soft-start capacitor is recharged with a 1.8µA current source. The regulator undergoes soft-start. During soft-start ($1V < V_{SS} < 2V$), the overload shutdown latch in Figure 3 cannot be set. When V_{SS} exceeds 2V, the set input of the overload latch is no longer blanked. If V_{FB} is still below 0.7V, then the regulator will undergo shutdown and restart. The soft-start process should allow the output voltage to reach 70% of its final value before C_{SS} is charged above 2V. Figures 9(a) and 9(b) show the timing diagrams of successful and failed start-up waveforms respectively. The soft-start interval should also be made sufficiently long so that the output voltage rises monotonically and it does not overshoot its final voltage by more than 5%.

During normal soft-start, both the COMP voltage and the switch current limit gradually increase until the converter becomes regulated. If the regulator output is shorted to

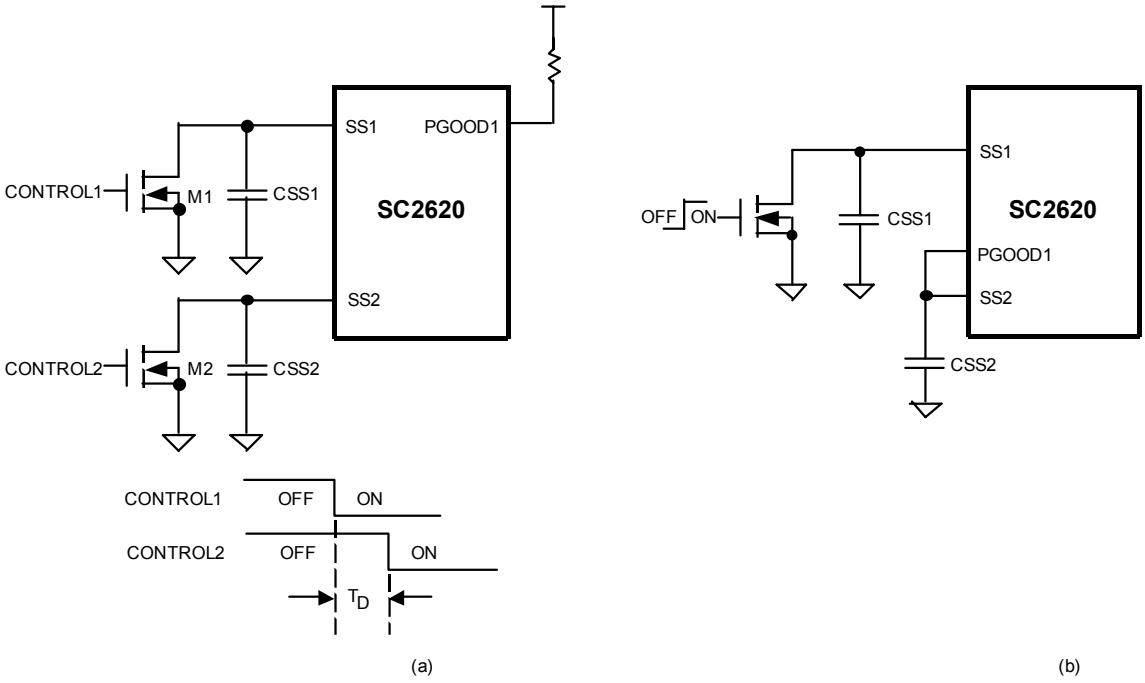


Figure 10. Sequencing the Outputs by (a) Delaying Release of one Channel Relative to the Other and (b) Using PGOOD1 to Control Channel 2.

ground, then the COMP voltage will continue to rise to its 2.4V upper limit. The SC2620 will reach its cycle-by-cycle current limit sometime during the soft-start charging phase (see Figure 17(c)). As described previously, the switches in the SC2620 either do not turn on at all or for at least 105ns. With the output shorted, the error amplifier will command the regulator to operate at full duty cycle. The current limit comparator will turn off the switch if the switch current exceeds 3.2A. However, this happens only after the switch is turned on for 105ns. During switch off time, the inductor current ramps down at a slow rate determined by the forward voltage of the freewheeling diode and the resistance of the short. If the resulting reverse volt-second is insufficient to reset the inductor before the start of the next cycle, then the inductor current will keep increasing until the diode forward voltage becomes high enough to achieve volt-second balance. This makes the current limit comparator ineffective. Short circuit robustness will be enhanced if the switching frequency is set below 500kHz at high V_{IN} (> 20V). This increases the off time and keeps the inductor current within bounds. The regulator is to be checked under realistic short circuit condition as the residual resistance of the short can significantly influence circuit behavior. Shortening the soft-start interval from the onset of switching to hiccup enable also makes short circuit operation more robust. A 22-47nF soft-start capacitor is found adequate for most applications.

In Figure 17(c), Channel 2 undergoes repeated shutdown and restart ("hiccup") with its output shorted. V_{SS} appears as an asymmetrical triangular wave. The resistance of the short appears to be 17mΩ.

Power Good Indicator

The PGOOD1 pin (Pin 15) is the open-collector output of Channel 1 power good comparator. This slow comparator is incorporated with a small amount of hysteresis. The FB low-to-high trip voltage of the power good comparator is 90% of the final regulation voltage. A pull-up resistor from the PGOOD1 pin to the input supply or the regulator output sets the logic high level of the comparator.

The power good comparator output becomes valid provided that V_{IN} is above 0.9V. In shutdown the power good output is actively pulled low. A power good pull-up resistor tied to the input will therefore increase current drain during shutdown. Tying the power good pull-up resistor to the regulator output is preferred, as this will minimize the shutdown supply current. In shutdown there is no voltage at the switching regulator output or current in the PGOOD1 pull-up resistor. If the PGOOD1 output high level (= V_{OUT}) is unacceptably low, then power good pull-up from the input or a separate power supply will be the only choice.

Sequencing the Outputs

As mentioned above, pulling either soft-start pin low with an external transistor shuts off the corresponding regulator (Figure 10). Releasing the soft-start pin enables that channel and allows it to start. Delaying the release of the soft-start pin of one channel with respect to the other is a straightforward way of sequencing the outputs. Figure 10(a) shows this method using two external transistors M_1 and M_2. M_1 is turned off first, allowing channel 1 to start. Channel 2 is then enabled after time T_D.

PGOOD1 can also be used in conjunction with Channel 2 soft-start to delay start of that regulator. This method is depicted in Figure 10(b). SS2 is pulled low and channel 2 is kept off until channel 1 output rises to 90% of its set voltage.

Loop Compensation

Figure 11 shows a simplified equivalent circuit of a step-down converter. The power stage, which consists of the current-mode PWM comparator, the power switch, the freewheeling diode and the inductor, feeds the output network. The power stage can be modeled as a voltage-controlled current source, producing an output current proportional to its controlling input V_{COMP}. Its transconductance G_{MP} is $8\Omega^{-1}$. With the current loop closed, the control-to-output transfer function $\frac{V_{OUT}}{V_{COMP}}$ has a dominant-pole p_2 located at a frequency slightly higher than that of the output filter pole.

$$\omega_{p2} \approx -\frac{nI_{OUT}}{V_{OUT}C_1} = -\frac{n}{R_{OUT}C_1} \quad (8)$$

where C_1 is the output capacitor, R_{OUT} is the equivalent load resistance and n (depending on duty ratio, slope compensation, frequency and passive components) is usually between 1 and 2.

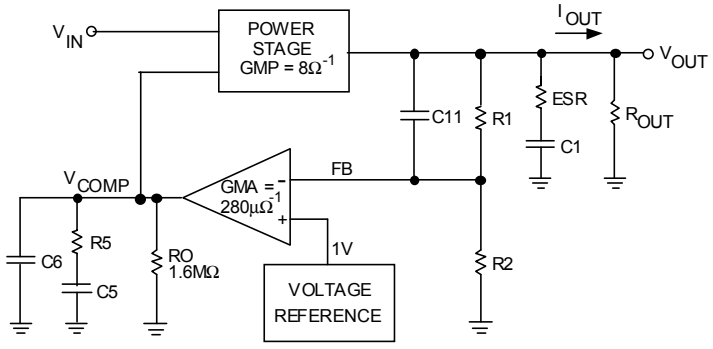


Figure 11. Simplified Control Loop Equivalent Circuit

If C_1 is ceramic, then its ESR zero can be neglected as it situates well beyond half the switching frequency. The low frequency gain of the control-to-output transfer function is simply the product of power stage transconductance and the equivalent load resistance (Figure 12).

The transfer functions of the feedback network and the error amplifier are:

$$\frac{v_{FB}}{v_{OUT}} = \left(\frac{R_2}{R_1+R_2}\right)\left[\frac{1+sC_{11}R_1}{1+s\left(R_1 \| R_2\right)C_{11}}\right] \quad (9)$$

and

$$\frac{v_{COMP}}{v_{FB}} \approx \frac{G_{MA}R_0\left(1+sC_5R_5\right)}{\left(1+sC_5R_0\right)\cdot\left(1+sC_6R_5\right)} \quad (10)$$

provided that $C_5 >> C_6$ and $R_0 >> R_5$.

In Equation (10), C_5 forms a low frequency pole p_1 with the output resistance R_0 of the error amplifier and C_6 forms a high frequency pole p_3 with R_5:

$$R_0 = \frac{\text{Amplifier Open Loop Gain}}{\text{Transconductance}} = \frac{53\text{dB}}{280\mu\Omega^{-1}} = 1.6\text{M}\Omega$$

$$\omega_{p1} = -\frac{1}{R_0C_5}$$

$$\omega_{p3} = -\frac{1}{R_5C_6}$$

In addition C_5 and R_5 form a zero with angular frequency:

$$\omega_{z1} = -\frac{1}{R_5C_5}$$

The output-to-control transfer function $\frac{v_{COMP}}{v_{OUT}} = \frac{v_{COMP}}{v_{FB}} \cdot \frac{v_{FB}}{v_{OUT}}$ is also shown in Figure 12. Its mid-band gain (between z_1 and p_3) is $G_{MA}R_5\left(\frac{R_2}{R_1+R_2}\right)$. The overall loop gain T(s) is the product of the control-to-output and the output-to-control transfer functions. To simplify $|T(j\omega)|$ Bode plot, the feedback network is assumed to be resistive. If the overall loop gain is to cross 0dB at one tenth of the switching frequency ($\omega_C = \frac{\omega_S}{10} = \frac{\pi f}{5}$) at –20dB/ decade, then its mid-band gain (between z_1 and p_2) will be

$$\frac{\omega_C}{\omega_{p2}} = \frac{\frac{\omega_S}{10}}{\frac{n}{C_1R_{OUT}}} = \frac{\omega_SC_1R_{OUT}}{10n}$$

This is also equal to $G_{MP}R_{OUT}G_{MA}R_5\left(\frac{R_2}{R_1+R_2}\right)$. Therefore

$$G_{MP}R_{OUT}G_{MA}R_5\left(\frac{R_2}{R_1+R_2}\right)=\frac{\omega_S C_1 R_{OUT}}{10n}.$$

Re-arranging,

$$R_5=\left(1+\frac{R_1}{R_2}\right)\frac{\omega_S C_1}{10nG_{MP}G_{MA}} \quad (11)$$

ω_{z1} is shown to be less than ω_{p2} in Figure 12. Making $\omega_{z1}=\frac{\omega_C}{6}=\frac{\omega_S}{60}$ gives a first-order estimate of C_5:

$$C_5 \approx \frac{60}{\omega_S R_5} \quad (12)$$

Notice that R_5 determines the mid-band loop gain of the converter. Increasing R_5 increases the mid-band gain and the crossover frequency. However it reduces the phase margin. C_6 is a small ceramic capacitor to roll off the loop

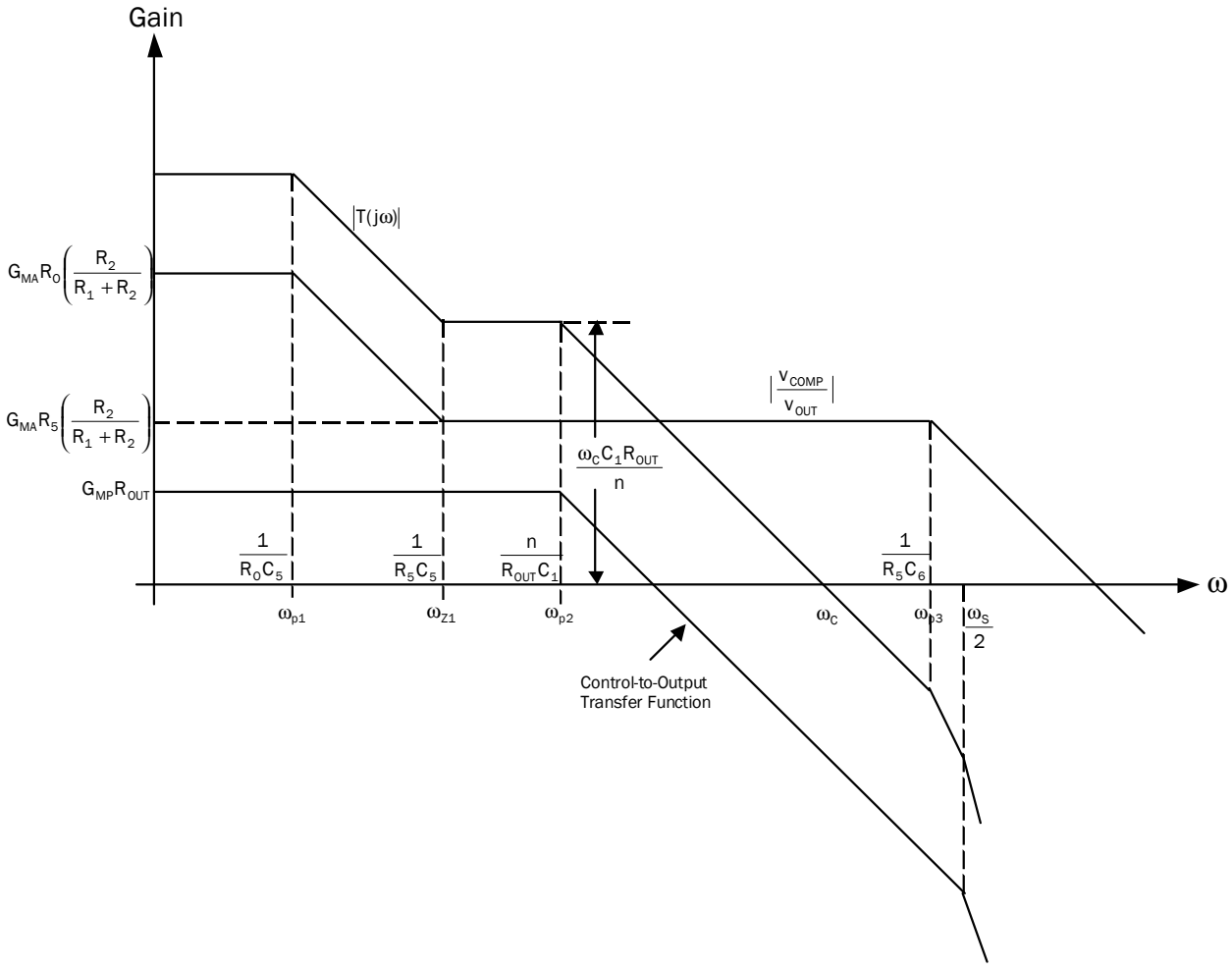


Figure 12. Bode Plots of Control-to-Ouput, Output-to-Control and the Overall Loop Gain. Control-to-output transfer function is shown with two poles near half the switching frequency ω_S.

gain at high frequency. Placing p_3 at about $\frac{\omega_S}{2}$ gives:

$$C_6 \approx \frac{1}{\pi f R_5} \quad (13)$$

Computed R_5, C_5 and C_6 can indeed result in near optimal load transient responses in over half of the applications. However in other cases empirically determined compensation networks based on optimized load transient responses may differ from those calculated by a factor of 3. Therefore checking the transient response of the converter is imperative. Starting with calculated R_5, C_5 and C_6 (using n=1 in Equations (11)-(13)), apply the largest expected load step to the converter at the maximum operating V_{IN}. Observe the load transient response of the converter while adjusting R_5, C_5 and C_6. Choose the largest R_5, the smallest C_5 and C_6 so that the inductor current waveform does not show excessive ringing or overshoot (see Figures 13(a), 13(b), 16(b) and 16(c)).

Feedforward capacitor C_{11} boosts phase margin over a limited frequency range and is sometimes used to improve loop response. C_{11} will be more effective if $R_1 >> R_1 || R_2$.

Example: Determine the compensation components for the 550kHz 9V-16V to 3.3V and 1.2V converter in Figure 1(a).

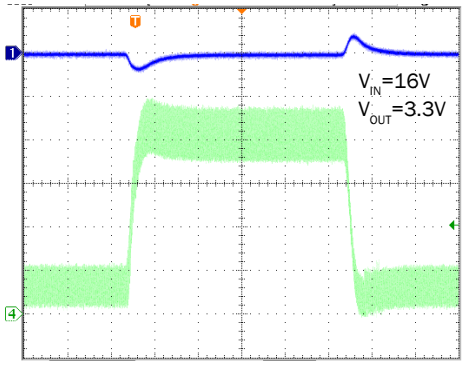
For both channels, $\omega_S = 3.5\,\text{Mrads}^{-1}$, $I_{OUT(MAX)} = 2\text{A}$ and $C_1 = 22\mu\text{F}$. n is assumed to be 1 in (11) and (12).

For the 3.3V output:

$$R_5 = \left(1 + \frac{30.1\text{k}}{13\text{k}}\right)\frac{3.5\times10^6 \cdot 22\times10^{-6}}{10\cdot(1)\cdot(8)\cdot(2.8\times10^{-4})} = 11.3\,\text{k}\Omega$$

$$C_5 \approx \frac{60}{11.3\text{k}\cdot 2\pi\cdot 5.5\times10^5} = 1.5\,\text{nF}$$

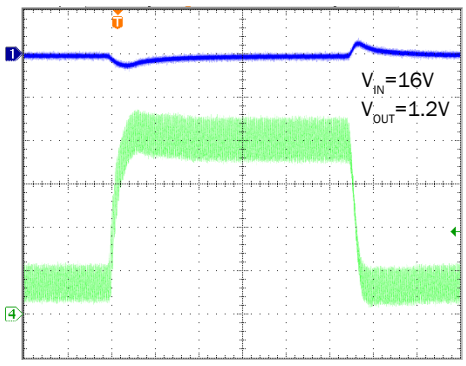
$$C_6 \approx \frac{1}{\pi\cdot(550\times10^3)\cdot(11.3\times10^3)} \approx 47\,\text{pF}$$



40µs/div

Upper Trace : OUT1 Voltage, AC Coupled, 0.5V/div
Lower Trace : L_1 Inductor Current, 0.5A/div

(a)



40µs/div

Upper Trace : OUT2 Voltage, AC Coupled, 0.5V/div
Lower Trace : L_2 Inductor Current, 0.5A/div

(b)

Figure 13. Load Transient Response of the Dual DC-DC Converter in Figure 1(a). I_{OUT1} and I_{OUT2} are switched between 0.3A and 2A.

For the 1.2V channel:

$$R_7 = \left(1 + \frac{2.61k}{13k}\right)\frac{3.5\times10^{6}\cdot22\times10^{-6}}{10\cdot(1)\cdot(8)\cdot(2.8\times10^{-4})} = 4.12k\Omega$$

$$C_8 \approx \frac{60}{4.12k\cdot2\pi\cdot5.5\times10^{5}} = 3.9nF$$

$$C_9 \approx \frac{1}{\pi\cdot(550\times10^{3})\cdot(4.12\times10^{3})} \approx 150pF$$

Bench measurement shows that compensation components computed from our simplified linear model give very good load transient response for Channel 1 (Figure 13(a)). However, optimizing load transient for Channel 2 will require a set of compensation component values different from those calculated above. Loop compensation networks shown in Figure 1(a) are empirically optimized for load transients. Figures 13(a) and 13(b) show the corresponding load transient responses.

Board Layout Considerations

In a step-down switching regulator, the input bypass capacitor, the main power switch and the freewheeling diode carry discontinuous currents with high $\frac{di}{dt}$ (Figure 14). For jitter-free operation, the size of the loop formed by these components should be minimized. Since the power switches are already integrated within the SC2620, connecting the anodes of both freewheeling diodes close to the negative terminal of the input bypass capacitor minimizes size of the switched current loop. The input bypass capacitors should be placed close to the PVIN pins. Shortening the traces of the SW and BOOST nodes reduces the parasitic trace inductance at these nodes. This not only reduces EMI but also decreases switching voltage spikes at these nodes.

The PVIN bypass capacitor C_{15}, the output filtering capacitors and the freewheeling diodes are to be grounded on the power ground plane (Figure 15). The feedback resistive dividers, the compensation networks, the soft-

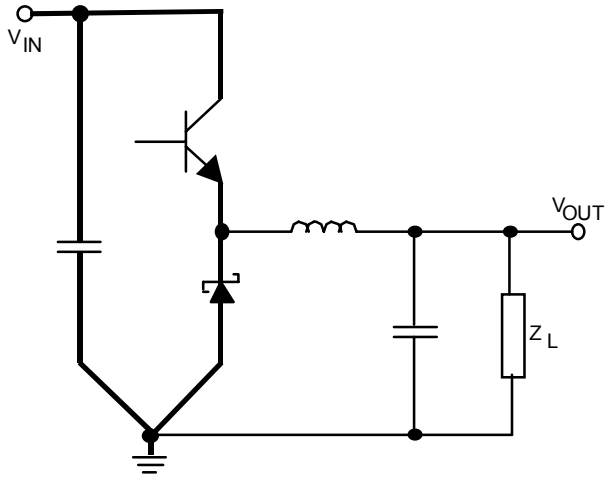


Figure 14. Fast Switching Current Paths in a Buck Regulator. Minimize the size of this loop to reduce parasitic trace inductance.

start capacitors and the VIN filtering capacitor C_{16} are to be tied to the analog ground. The frequency-setting resistor R_9 is placed next to the ROSC pin and is also connected to the analog ground. R_{20} is a 0Ω resistor that connects the analog ground to the power ground at a single point.

The exposed pad should be soldered to a large analog ground plane as the analog ground copper acts as a heat sink for the device. To ensure proper adhesion to the ground plane, avoid using vias directly under the device. In figure 15 two 12mil vias are placed at the edge of the underside pad.

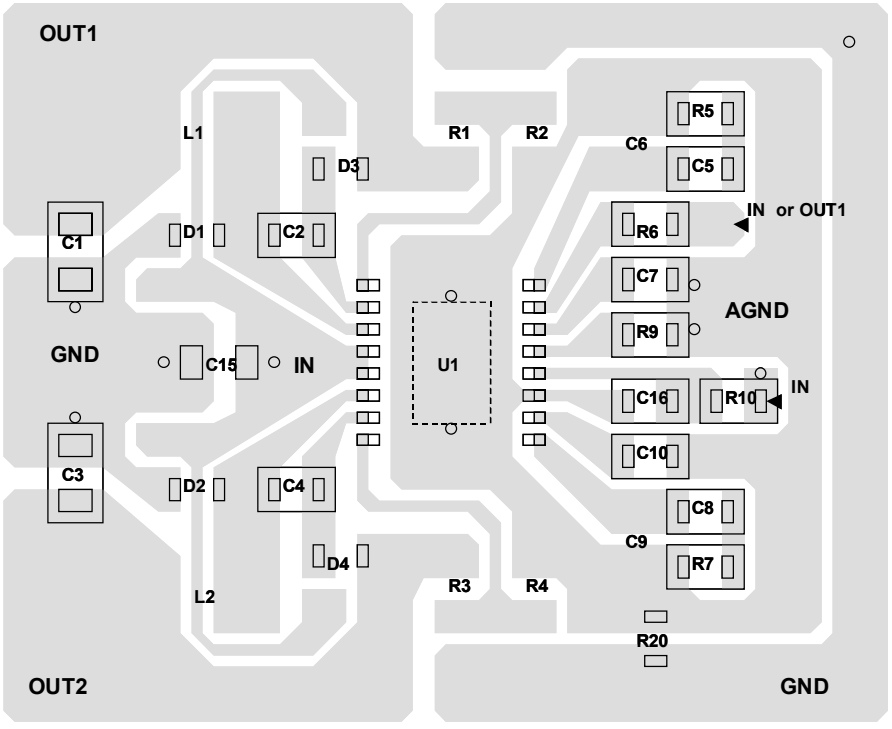
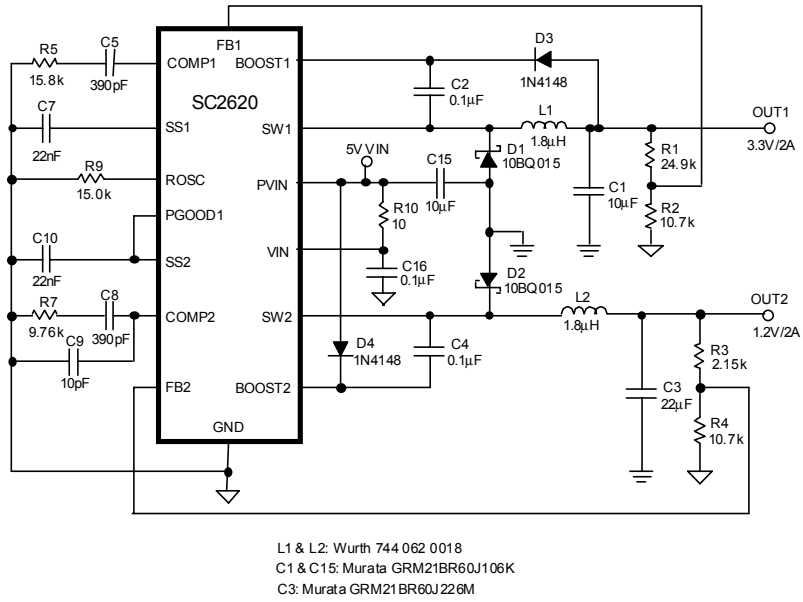


Figure 15. Suggested PCB Layout for the SC2620.



L1 & L2: Wurth 744 062 0018
C1 & C15: Murata GRM21BR60J106K
C3: Murata GRM21BR60J226M

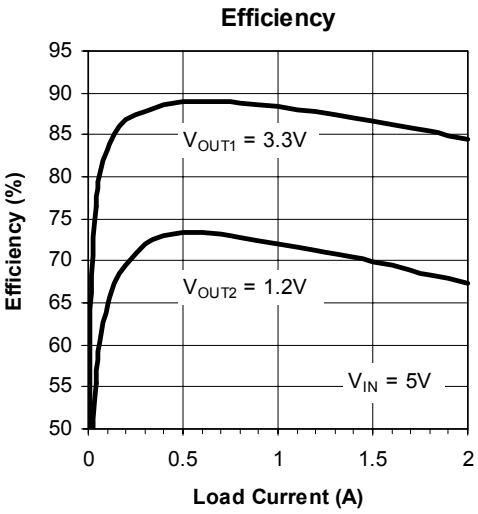
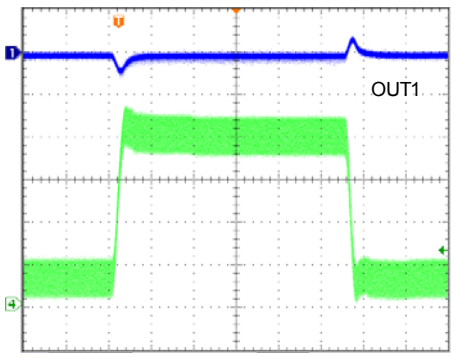


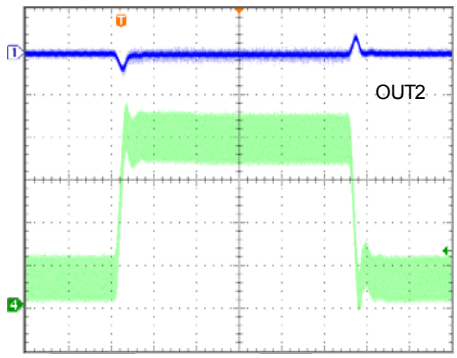
Figure 16(a). 1.2MHz 5V to 3.3V and 1.2V xDSL Power Supply. Channel 2 does not start until Channel 1 output voltage becomes regulated.



40µs/div

Upper Trace : OUT1 Voltage, AC Coupled, 0.5V/div
Lower Trace : L_1 Inductor Current, 0.5A/div

(b)

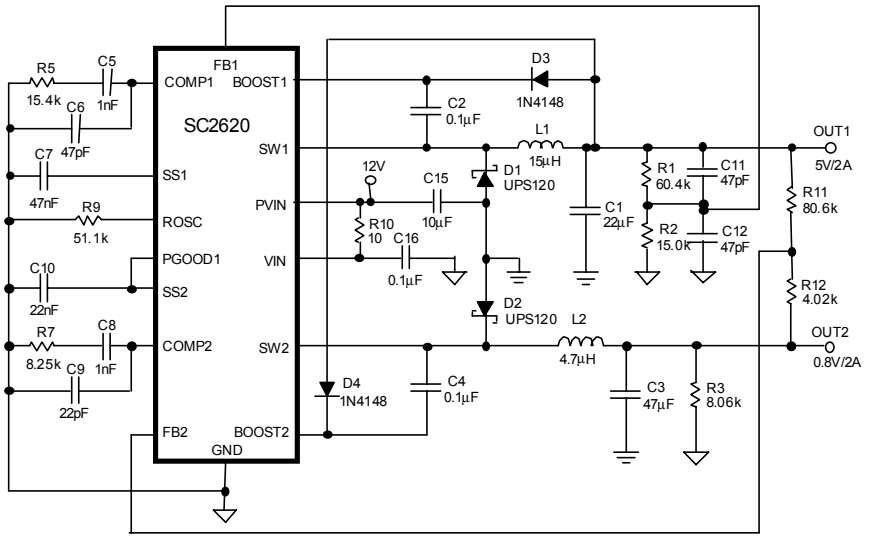


40µs/div

Upper Trace : OUT2 Voltage, AC Coupled, 0.2V/div
Lower Trace : L_2 Inductor Current, 0.5A/div

(c)

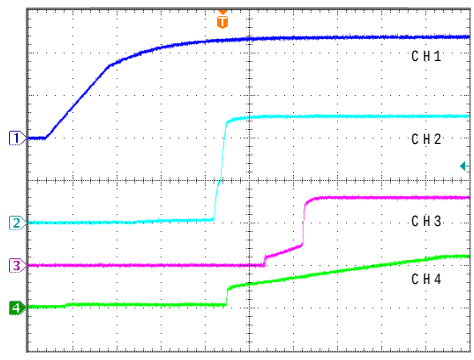
Figures 16(b) and 16(c). Load Transient Response. I_{OUT} is switched between 0.3A and 2A.



L1 : Coiltronics DR74
L2 : Coiltronics DR73

C1: Murata GRM21BR60J226M
C3: Murata GRM31CR60J476M
C15: Murata GRM32DR61E106K

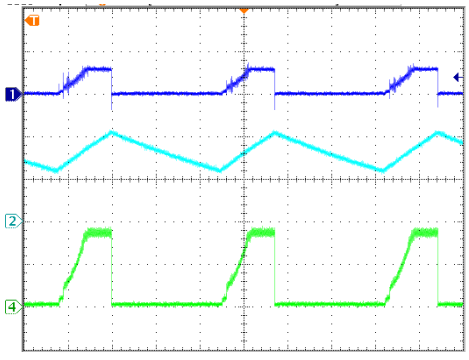
Figure 17(a). 500kHz 12V to 5V and 0.8V step-down converter. Notice that V_{OUT2} is lower than the nominal FB voltage. R_{11} and R_{12} constitute the feedback voltage divider for Channel 2.



4ms/div

CH1 : V_{IN}, 5V/div
CH2 : OUT1 Voltage, 2V/div
CH3 : OUT2 Voltage, 0.5V/div
CH4 : SS2 Voltage, 2V/div

Figure 17(b). V_{IN} Start-up Transient (I_{OUT1} = I_{OUT2} = 1.5A).



10ms/div

Upper Trace : OUT2 Voltage, 0.1V/div
Middle Trace : SS2 Voltage, 1V/div
Lower Trace : I_{L2}, 2A/div

Figure 17(c). Channel 2 Output Short-circuit Hiccup.

Typical Application Circuits

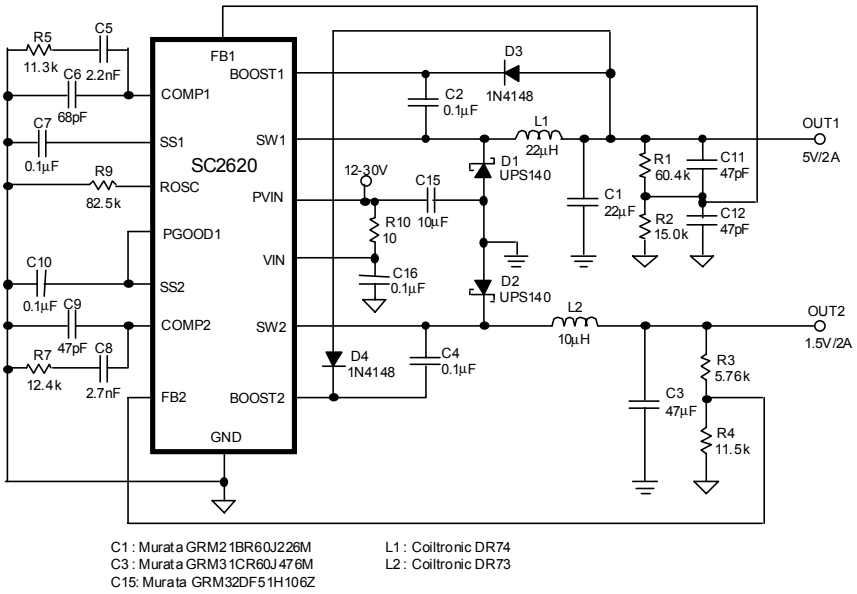
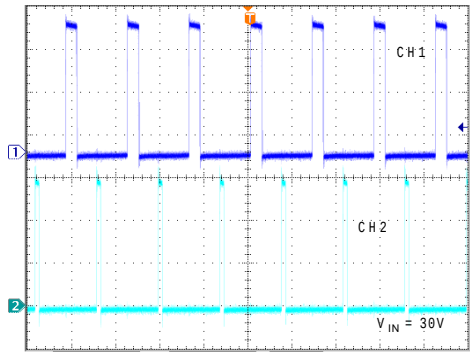


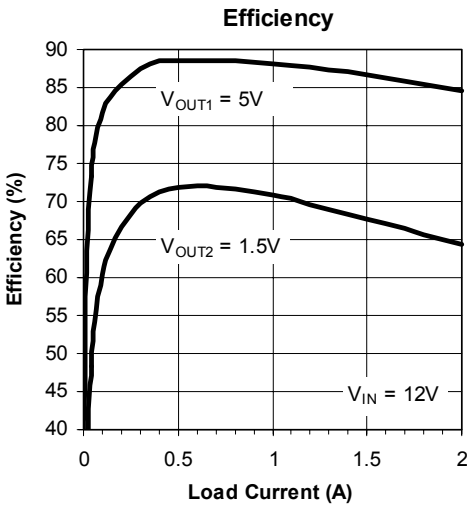
Figure 18(a). 350kHz 12V-30V Input to 5V and 1.5V Step-down Converter. Notice that Channel 2 is bootstrapped from OUT1. Channel 2 will be held off if OUT1 voltage is below 90% of its set value.

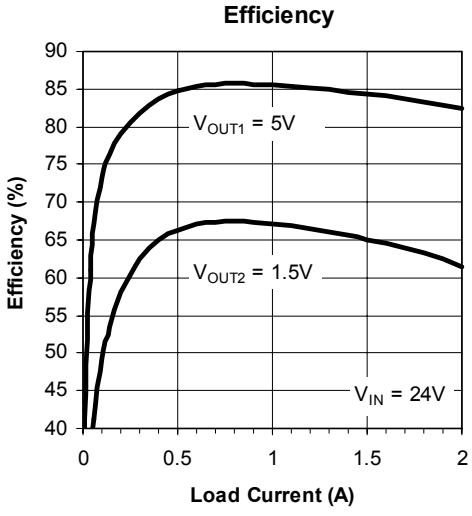


CH1 : SW1 Voltage, 10V/div
CH2 : SW2 Voltage, 10V/div

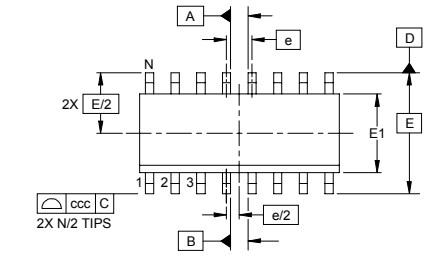
2µs/div

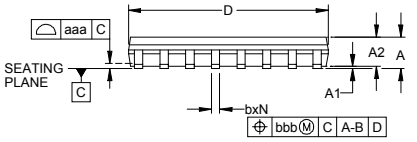
Figure 18(b). Switching Waveforms. I_{OUT1}= I_{OUT2}= 1A.

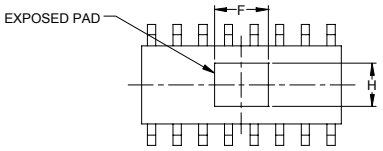


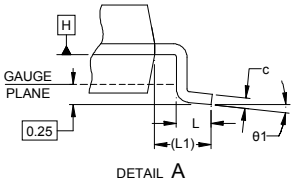


Outline Drawing - SOIC-16 EDP

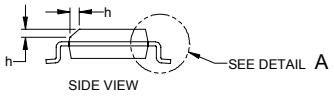








DETAIL A



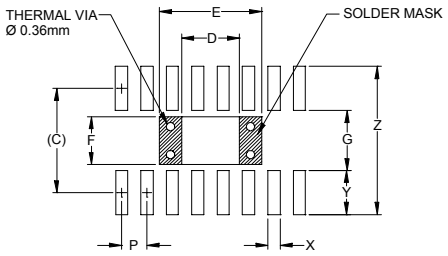
SIDE VIEW

DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.000	-	.005	0.00	-	0.13
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.386	.390	.394	9.80	9.90	10.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
F	.100	.105	.110	2.54	2.67	2.79
H	.080	.085	.090	2.03	2.16	2.29
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.04)		
N	16			16		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AC.

Land Pattern - SOIC-16 EDP



DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
D	.114	2.90
E	.201	5.10
F	.094	2.40
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

Contact Information

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