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TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

DESCRIPTION

The SC2422A biphase, current mode controller is designed to work with Semtech smart synchronous drivers, such as the SC1205, SC1305 or the SC1405 to provide the DC/DC converter solution for the most demanding Micro-processor applications. Input current rather than output current sensing is used to guarantee precision phase to phase current matching using a single sense resistor on the input power line. Accurate current sharing and pulse by pulse current limit are implemented without the power loss and transient response degradation associated with output current sense methods. Two phase operation allows significant reduction in input/output ripple while enhancing transient response.

The DAC step size and range are programmable with external components thus allowing compliance with new and emerging VID ranges.

A novel approach implements active droop, minimizing output capacitor requirements during load transients. This avoids the pitfalls of the passive droop implementation. This feature also allows easy implementation of N+1 redundancy and current sharing among modules.

Programmable Under Voltage Lockout assures proper start-up and shutdown by synchronizing the controller to the driver supply. Wide PWM frequency range allows use of low profile, surface mount components.

TYPICAL APPLICATION SCHEMATIC

FEATURES

- **Precision, pulse by pulse phase current matching**
- Active drooping allows for best transient response
- **Input Sensing Current mode control**
- **Programmable DAC step size/offset allows Compliance with VRM9.0, VRM8.3 or VRM8.4**
- Externally programmable soft-start
- 5V or 12V input for next generation processors
- 0% minimum duty cycle improves transient response
- Externally Programmable UVLO with hysteresis
- Cycle by cycle current limiting
- Programmable Internal Oscillator to 1 MHz
- VID IIIII Inhibit (No CPU)

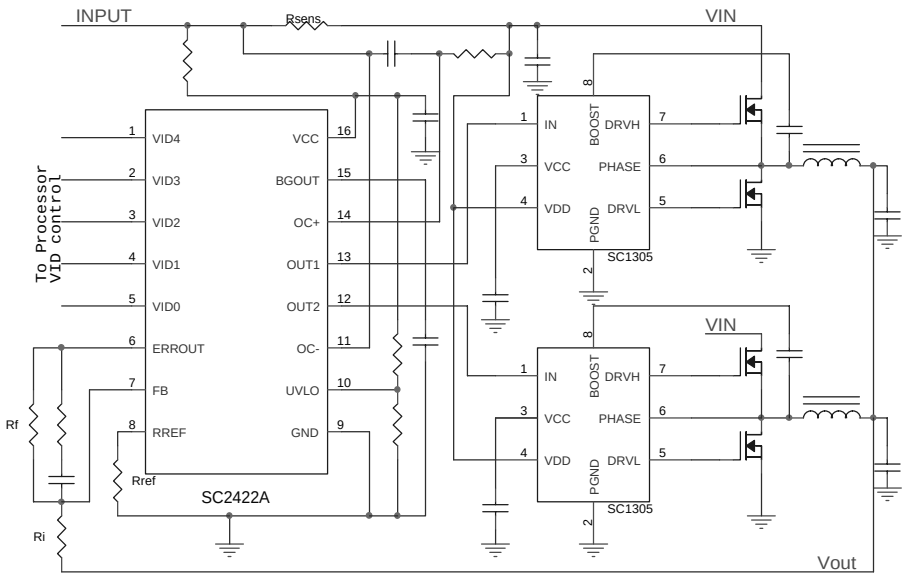
APPLICATIONS

- Intel Advanced Microprocessors
- AMD Athlon™ power supplies
- Servers/Workstations, high density power supplies

ORDERING INFORMATION

DEVICE(1)	PACKAGE	TEMP. RANGE (T_J)
SC2422ACS.TR	SO-16	0 - 125°C
SC2422A.EVB	Evaluation Board	

Note:
(1) Only available in tape and reel packaging. A reel contains 1000 devices.



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Maximum	Units
Input DC Rail Voltage to GND	V_{IN}	15	V
PGND to GND		±1	V
Operating Temperature Range	T_A	-20 to 125	°C
Junction Temperature	T_J	0 to 125	°C
Thermal Resistance Junction to Case	θ_{JC}	20	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}	60	°C/W
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 sec	T_{LEAD}	300	°C

ELECTRICAL CHARACTERISTICS

Unless specified: V_{CC} = +5V, T_{AMB} = 25°C, R_{REF} = 11.5kΩ. See Typical Application Circuit

Parameter	Conditions	Min	Typ	Max	Units
Chip_Supply					
IC Supply Voltage		4.5	5	14	V
IC Supply Current	V_{CC} = 5.0 ~ 12.0V		9		mA
Reference Section					
Bandgap Output	C_{BG} = 4.7nF		1.5		V
Source Impedance			3		kΩ
Supply Rejection	V_{CC} = 5.0V ~ 12.0V		2		mV/V
VID Step	R_I = 6.49kΩ, R_{REF} = 11.5kΩ		25		mV
Voltage Accuracy		-1		1	%
Temperature Stability	0°C < T_{AMB} < 70°C		5		%
Voltage Accuracy	0°C < T_{AMB} < 70°C		+/-1		%
Oscillator Section					
Frequency Range		400		1000	kHz
Frequency Accuracy	V_{IN} = 12.0V, R_{REF} = 13kΩ or V_{IN} = 5.0V, R_{REF} =11.5kΩ	450	500	550	kHz
Temperature Stability	0°C < T_{AMB} < 70°C		+/-5		%
Voltage Error Amplifier					
Input Offset Voltage			+/-5		mV
Input Offset Current			0.1		µA
Open Loop Gain	1V < V_{ERROUT} < 4V		90		dB
PSRR	V_{CC} = 5 - 12V		80		dB
Output Sink Current	V_{ERROUT} = 1V		2.5		mA
Output Source Current	V_{ERROUT} = 4V		2		mA
Unity Gain Bandwidth	I_O < 100µA		5		MHz
Slew Rate	I_O < 100µA		10		V/uS

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ELECTRICAL CHARACTERISTICS (Cont)

Unless specified: V_{CC} = +5V, T_{AMB} = 25°C, R_{REF} = 11.5kΩ.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Current Sense Amplifier					
Amplifier Gain	(V_{OC-} - V_{OC+}) < 100mV		26		dB
Input Offset Voltage, Input Referred	(V_{OC-} - V_{OC+}) < 100mV		4		mV
CMRR	V_{ICM} = 9 ~ 14V @ DC		80		dB
PSRR	V_{CC} = 9 ~ 14V @ DC		80		dB
Input Common Mode Range			V_{CC} +/- 0.3		
Max Differential Signal/ Current Limit Threshold	V_{OC-} - V_{OC+}		100		mV
I-Limit Delay	Current limit activation to OUT 1 & OUT 2 switching off		60		ns
Protection					
UVLO Ramp-up Threshold	R_{SOURCE} UVLO pin = 20kΩ		1.475		V
UVLO Ramp-down Threshold	R_{SOURCE} UVLO pin = 20kΩ		1.375		V
Outputs (OUT 1, OUT 2)					
Max Duty Cycle	Per phase, F_{OSC} = 500kHz		47		%
Duty Match	F_{OSC} = 500kHz	-.5		.5	%
Typical Output Voltage Swing	R_L = 10kΩ	.8		2.5	V
	R_L = 100kΩ	.2		3.3	V
VID Logic Threshold		0.8		2	V
VID Logic Pin Bias Current	V_{IN} = 0		12		µA

Note:

1. If the VID pins are driven high by an external source (in contrast to being left open), then all VIDs input will need to be externally pulled high. If VIDs are left open, no external pull-up is required.
2. This device is ESD sensitive. Use of standard ESD handling precautions is required.

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PIN DESCRIPTION

Pin 1: VID4 , MSB

Pin 2: VID3

Pin 3: VID2

Pin 4: VID 1

Pin 5: VID0 , LSB

Pin 6: ERROUT Error-amplifier output.

Pin 7: FB Error-amplifier inverting input.

Pin 8: RREF Frequency setting resistor pin. Also programs the DAC current step size. (see application information for programming the frequency)

Pin 9: GND Chip ground.

Pin 10: UVLO Programmable Under Voltage Lock-Out. This pin may be connected to the MOSFET driver supply through a voltage divider to inhibit the SC2422A until the drivers are on. The UVLO comparator trip point is 1.5V.

Pin 11: OC- Input current sense, negative input. This pin is connected to the input supply side of the current sense resistor.

Pin 12: OUT2 PWM output for phase 2. Drives external Power MOSFET driver.

Pin 13: OUT1 PWM output for phase 1. Drives external Power MOSFET driver.

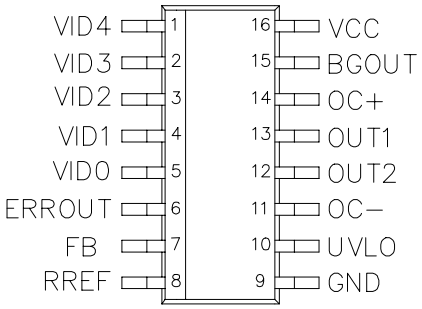
Pin 14: OC+ Input current sense positive input. This pin is connected to MOSFET side of the current sense resistor.

Pin 15: BGOUT Soft start and reference. Bypass to ground (GSEN) with a .022µF - 0.1µF capacitor to implement soft start in conjunction with internal 3KΩ resistor. To ensure output voltage accuracy, the maximum current source/sink from this pin should be limited to 0.5 uA.

Pin 16: VCC Chip positive supply.

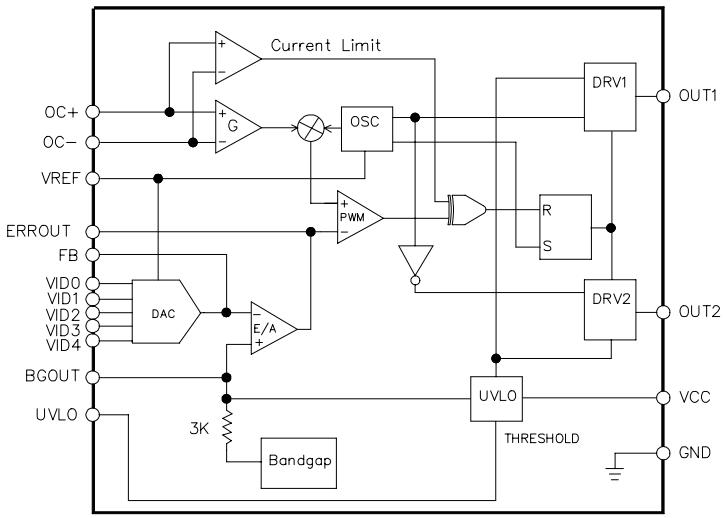
PIN CONFIGURATION

Top View



(16-Pin SOIC)

FUNCTIONAL BLOCK DIAGRAM



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OUTPUT VOLTAGE (VRM 9.0) Unless specified: 0 = GND; 1 = High (or Floating). T_A = 25°C, V_{CC} = 5V, 2-Phase operation					V_{CCCORE}
VID4	**VID3**	**VID2**	**VID1**	**VID0**	**(VDC)**
1	1	1	1	1	Output Off
1	1	1	1	0	1.1
1	1	1	0	1	1.125
1	1	1	0	0	1.15
1	1	0	1	1	1.175
1	1	0	1	0	1.2
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.3
1	0	1	0	1	1.325
1	0	1	0	0	1.35
1	0	0	1	1	1.375
1	0	0	1	0	1.4
1	0	0	0	1	1.425
1	0	0	0	0	1.45
0	1	1	1	1	1.475
0	1	1	1	0	1.5
0	1	1	0	1	1.525
0	1	1	0	0	1.55
0	1	0	1	1	1.575
0	1	0	1	0	1.6
0	1	0	0	1	1.625
0	1	0	0	0	1.65
0	0	1	1	1	1.675
0	0	1	1	0	1.7
0	0	1	0	1	1.725
0	0	1	0	0	1.75
0	0	0	1	1	1.775
0	0	0	1	0	1.8
0	0	0	0	1	1.825
0	0	0	0	0	1.85

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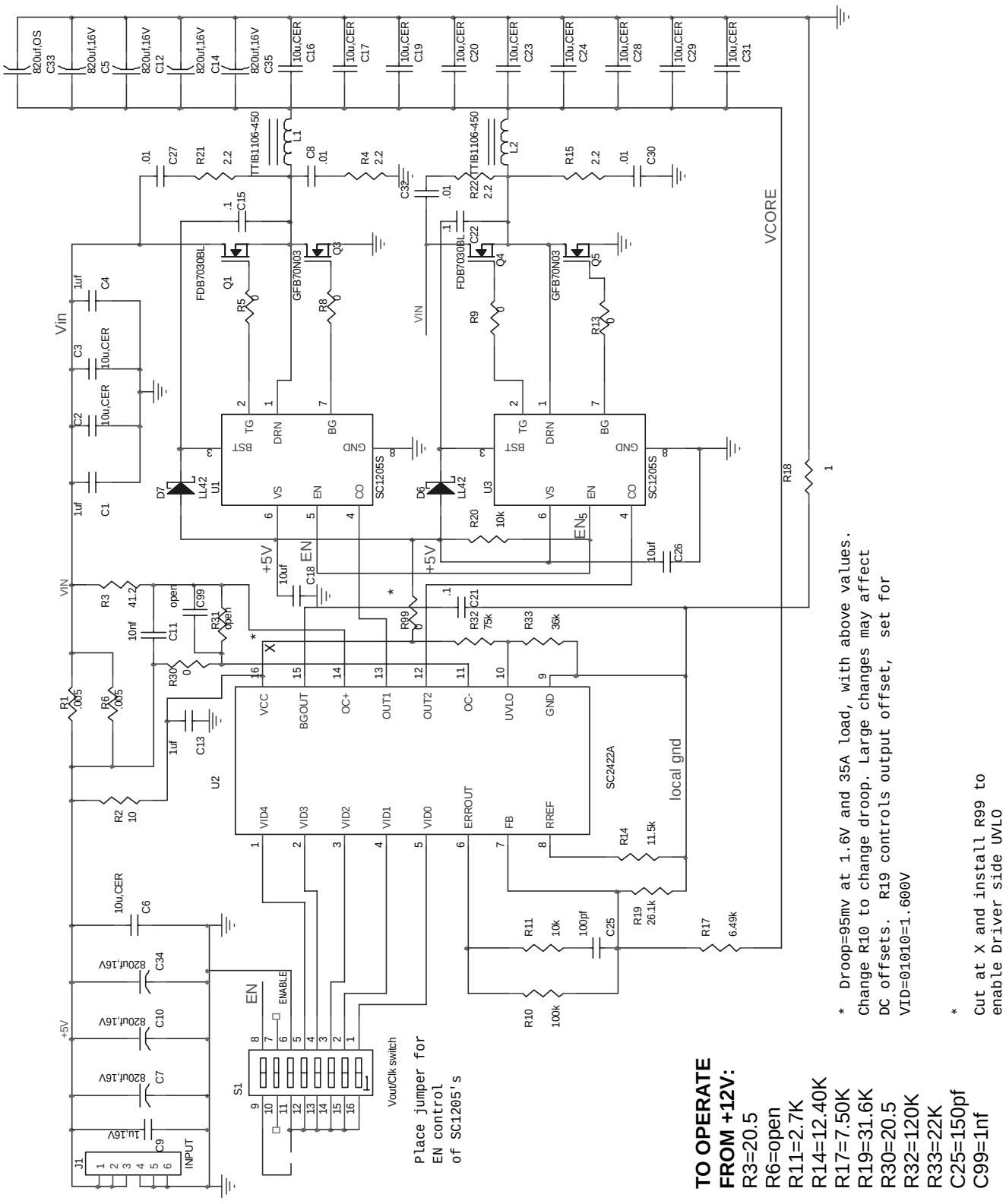
Figure 1:
SC2422A SCHEMATIC WITH +5V INPUT FOR THE AMD ATHLON™ PROCESSOR



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Applications Information

The SC2422A is an Input Current Mode Controller designed for High Current, High performance two phase DC/DC converters. The Current mode control is implemented by generating the PWM ramp from the Input Current, rather than the output current. This has the advantage of eliminating the output current sense resistors, and the power loss associated with output current sensing. Eliminating the output current sense resistors has the added advantage of improving the transient response by reducing the output impedance.

The output voltage is programmed via a 5-bit DAC in 32 steps. A novel technique allows programmable DAC step size and output offset, allowing the SC2422A based DC/DC converters to work in VRM9.0, VRM 8.3, VRM8.4, VRM8.5 or future specified voltage ranges.

Theory of Operation

Pulse by Pulse Current Matching

The operation of the Input Current Mode, ICM, is as follows:

The SC2422A Oscillator generates the OUT1 and OUT2 logic output drives. OUT1 and OUT2 are non-overlapping and sequentially command an external, power MOSFET driver to turn on the Top MOSFETs. When the Top MOSFET is enhanced (each phase), the input voltage is impressed across the MOSFET and the output Inductor. The AC current in the inductor is:

$$IL = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{L} = \frac{(V_{IN} - V_{OUT}) \times D}{FxL}$$

Where F is the frequency (per phase) and L is the output inductor. D is the duty cycle and is approximately equal to V_O/V_{IN}. The approximation arises from the fact that the Duty cycle extends slightly to compensate for losses in the current path. These losses include RDS_ON of the MOSFET, the Equivalent Series Resistance of the Inductors and the PCB trace resistances.

The inductor current flows in the input current sense resistor, generating a PWM ramp, same as in all current mode controllers. The ramp is compared with an amplified, level shifted and filtered version of the output voltage at the PWM comparator. The comparator then outputs a gate drive pulse that terminates when the ramp voltage equals the error amplifier output signal. The current mode control is inherently immune to input voltage changes because the ramp amplitude reflects the input voltage changes.

Since the input current sense resistor is the same for both phases, the inherent inaccuracy due to mismatch between output current sense resistors is avoided. Also, since the comparator threshold is the same for both phases, accurate current matching is achieved between phases. This implements a pulse by pulse current matching with a faster response to changes in output current by monitoring the input current for each phase.

Programming the SC2422A

Figure 2 below, is the connection schematic for the Internal Error Amplifier.

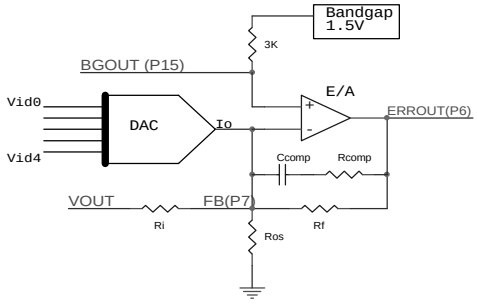

Figure 2: Error amplifier connections

The external components, R_I, R_{OS} and R_F set the DAC step size, output voltage offset and droop, accordingly. A resistor from R_{REF} (pin 8) to ground programs the frequency as well as the DAC *current* step size.

Programming the Switching Frequency

The oscillator frequency can be selected first by setting the value of R_{REF} resistor (pin 8) to ground.

$$f_{OSC} = \frac{13k\Omega * 500kHz}{R_{REF}}$$

$$V_{IN} = 12V$$

The switching frequency per phase is 1/2 of the above oscillator frequency.

Programming the DAC Step Size

The SC2422A allows programming the output voltage and the DAC step size by selecting external resistors. The DAC *current* step size, for one MSB is:

$$I_{DAC\_MSB} = \frac{V_{BG}}{R_{REF}}$$

where R_{REF} is the resistor from R_{REF} pin to Ground.

The DAC MSB *voltage* step size is calculated as follows:

$V_{DAC\_MSB} = I_{DAC\_MSB} * R_I$

$$V_{DAC\_LSB} = \frac{V_{DAC\_MSB}}{32}$$

or

$$V_{DAC\_LSB} = \frac{V_{BG}}{R_{REF}} * \frac{R_I}{32}$$

Note that changing R_{REF} affects both frequency and DAC step size. R_I must be proportionally adjusted to keep the same step size at different frequencies. The advantage of this method is that all new VID specifications can be accommodated by modifying external components while maintaining the required precision without the need for converter redesign.

Programming the DAC Offset Voltage

Kirchoff's current law can be applied to the error amplifier's Inverting node (see figure 2) to calculate R_{OS}, the DAC offset setting resistor. The output Offset at zero DAC current (VID=00000), is set as follows:

$$R_{OS} = \frac{V_{BG}}{\frac{V_O - V_{BG}}{R_I} + \frac{V_{EO} - V_{BG}}{R_F}}$$

Where V_{EO} is the error amplifier output voltage and as a first approximation is equal to 1.75V.

Where V_{BG} = Precision Reference Voltage = 1.50V. The value of R_{OS} can be fine trimmed using a potentiometer connected from the FB pin to ground.

Programming the Dynamic (Active) Droop

The SC2422A employs a novel approach to active drooping for optimum transient response. The output voltage is regulated as a function of output current. At zero current the output is regulated to the upper limit of the output voltage specification. As the load is increased, the output "droops" towards the lower limit. This makes optimum use of the output voltage error band, yielding minimum output capacitor size and cost. Active drooping, does not compromise the converter response time as does passive droop techniques. The active droop also allows for an accurate Inter-Module current sharing scheme, where multiple DC/DC converters are required to share the current required by a DC bus. As one module supplies more current, that modules output voltage "droops", allowing other modules to provide the balance of the required current.Any changes in the output voltage is instantaneously reflected to the error amplifier, which has a high Slew Rate and wide Gain-Bandwidth product to recover the output voltage to its nominal level with minimal delay.

The droop is adjusted by setting the feedback resistor, Rf. While the optimum value of R_F may be derived experimentally, the following equation can provide the droop at a given output current:

$$V_{DROOP} = \frac{G_{CA} * R_I * R_S * I_{OUT}}{2_{RF}}$$

The Gain of the current amplifier is set to 20 (26dB), while R_S is the input sense resistor.

The effective inductance of the sense resistor must be minimized to achieve accurate correlation between the above equation and actual droop achieved. This is because the inductive spike, which may also be caused by layout inductance's, will alter the PWM comparator trip point. The value of R_F may have to be adjusted to compensate for such parasitic effects.

Since Rf also sets the DC gain of the system, changing the value of Rf affects the offset voltage, which is set via Ros. The value of Ros can be modified to achieve exact offset after the droop resistor has been chosen.It must be noted that the Current Amplifier gain is quite precise, with greater than 80dB of Common Mode Rejection Ratio (CMRR). Thus the droop's accuracy is limited primarily by external components tolerances and the external parasitic effects.

Loop Gain Considerations

The Modulator gain in Input Current Mode control is equal to:

$$K_{MOD} = \frac{V_{IN}}{V_{RAMP}}$$

$$V_{RAMP} = 0.3V + R_{SENSE} \text{ X } T_{OSC} \text{ X } G_{CA} \text{ X } \frac{V_{IN} - V_O}{L}$$

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Where:

R_S = Input current sense resistor
T_{OSC} = Oscillator period
G_{CA} = Current Amplifier Gain
0.3V is the ramp added for slope compensation when the output current is near zero.

The DC loop gain is the product of the modulator gain and the error amplifier gain and is calculated as follows:

$$G_{LOOP} = \frac{V_{IN} * R_F}{V_{RAMP} * R_I}$$

Refer to Application note AN00-1 for detailed treatment of frequency compensation component selection as well as programming the SC2422A. The application note is available on the Semtech website or by contacting the factory.

Programming the Under Voltage Lockout

The SC2422A may be operated from any supply in +5V to +12V range. A pin has been dedicated to externally selecting the voltage at which the SC2422A outputs are active. A good typical turn-on threshold value is 4.5V for a +5V input supply and 9V for a +12V supply. A voltage divider connected to the UVLO pin selects this threshold. The UVLO comparator trip point is approximately 1.475V. Sufficient hysterisis is provided to ensure proper DC/DC converter shutdown.

The UVLO setting should consider external MOSFET driver's UVLO threshold. Ideally, the external MOSFET driver should turn on before the SC2422 controller and turn off before the controller. This assures the converter output will rise and fall slowly using the soft start feature and that the output voltage will not go negative at turn-off.

PCB layout

Care must be excercised when laying out the PC board for SC2422 or other input current mode DC/DC converters. SInce the current is delivered and sensed in pulse packets, the inductance of the current carrying traces and thus their length must be minimized. Ceramic bypass capacitors must be located near the sense resistor. For a detailed treatment and circuit parasitic models, consult application note:

AN00-7:"Component Selection and PC Board layout Considerations in Input Current Mode DC/DC Converters". This application note is available by contacting the factory.

Remote Sensing Capability

The SC2422 has a single ground for error amplifier and DAC reference and for the internal biasing of the chip. Since the chip uses approximately 10ma of quiescent current, the ground pin may be connected to a remote location without fear of ground loops. When used as a microprocessor power supply, connecting the ground pin directly to the ground plane may result in undesirable voltage drops in the plane at high output current. This is not entirely predictable since the error amplifier is correcting for the DC error with reference with the ground plane and not the processor "feedback ground". Thus any voltage difference between the two ground will result in a DC error. This error will obviously consume valuable static error band tolerance. To avoid this DC error, the SC2422 ground pin (pin 9) can be connected to a copper "Island", to which Rref (frequency setting resistor) and Ros (offset setting resistor) will also be connected. This "Island" in turn will only be connected to the "Processor Feedback" ground via a trace. While the trace may be long, it should not be routed through or near the switching sections or noisy components. This method of remote sensing will alleviate the need for a differential amplifier to sense the output voltage/output return pair and the design effort and costs associated with it.

SC2422A Evaluation Board

The SC2422A based DC/DC converter utilizes the SC1205 High Speed MOSFET drivers to achieve VRM 9.0 output Voltage Specifications. SC2422A Evaluation Board Schematic (Figure 1) shows the circuit for a 40A, BiPhase DC/DC converter. The Evaluation board is available by contacting the factory or Semtech website at WWW.Semtech.com.

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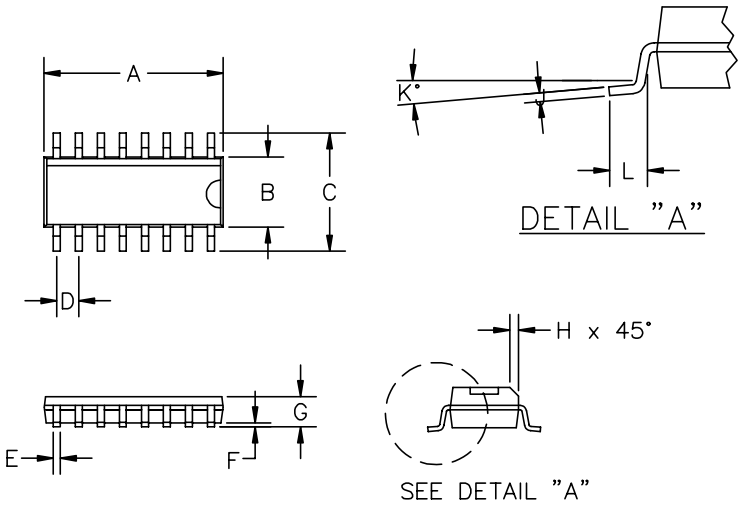
OUTLINE DRAWING SO-16

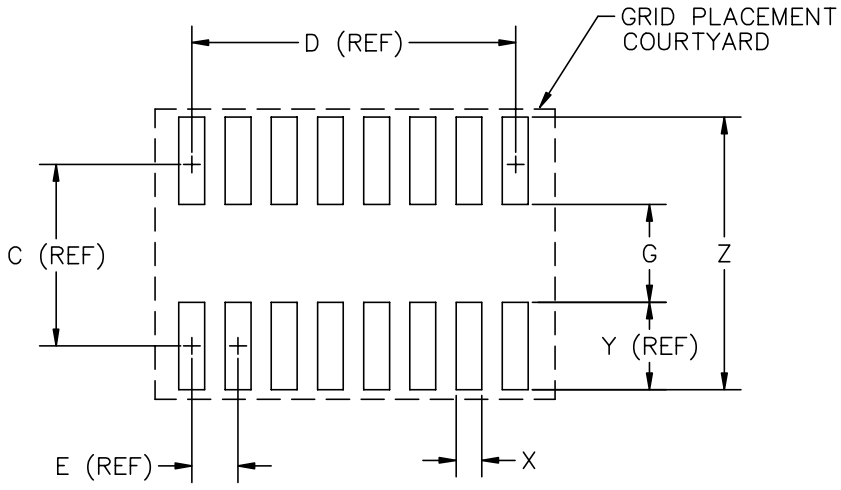


DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.386	.393	9.80	10.0	[2]
B	.150	.158	3.80	4.00	[2]
C	.228	.244	5.80	6.20	–
D	.050 BSC		1.27 BSC		–
E	.013	.020	0.33	0.51	–
F	.004	.010	.10	.25	–
G	.053	.069	1.35	1.75	–
H	.010	.020	.25	.50	–
J	.007	.010	.19	.25	–
K	0°	8°	0°	8°	–
L	.016	.050	.40	1.27	–

Jedec MS-012AC

[2] DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTUSIONS

LAND PATTERN SO-16



DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	–	.197	–	5.00	–
D	–	.35	–	8.89	–
E	–	.05	–	1.27	–
G	.102	.110	2.60	2.80	–
X	.02	.03	.60	.80	–
Y	–	.095	–	2.40	–
Z	.28	.29	7.20	7.40	–

[1] GRID PLACEMENT COURTYARD IS 22 X 16 ELEMENTS (11mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN IEC PUBLICATION 97.

ECN00-1242