TOSHIBA

TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.

Preliminary

TC160G and TC163G CMOS Gate Arrays for Low Voltage Operation

0.8 micron 3V/3.3V

Description

The TC160G and TC163G 0.8 micron gate array series operate at 3V±0.3V or 3.3V±0.3V (low voltage). They have a typical gate speed of 0.4ns and up to 210K(2) usable gates. Low voltage operation reduces power consumption by about 50%, compared to 5V operation, making these products ideal for low power or battery-operated applications, including laptops, notebooks, pen-based computers, and handheld devices. Low power operation may allow the use of more cost-effective packaging.

The TC160G series uses the same power supply for both the core and I/O circuits. The TC163G series uses two power rings for I/O circuitry. One ring is set to operate at low voltage and the other at 5V. There are no restrictions on low voltage and 5V I/O circuit placement.

The TC163G series provides an effective ASIC interface between 5V and low voltage components. When mixed voltage operation is not required, the TC160G offers a more economical solution.

Both gate array series use a sea-of-gates architecture with two or three layers of metal interconnect. The products are members of the Toshiba Digital System Arrays™ family. Libraries are compatible with the TC110G, TC140G and TC160G.

Both products are supported by the Toshiba Design Environment which embraces popular CAE tools. Toshiba has design centers around the United States and Canada to provide in-depth support.

Features

- Process: 0.8 micron (drawn) CMOS Si-gate double or triple layer metal
- Raw gates: from 6K up to 302K
- Usable gates: from 2.4K up to 210K
- I/O pads: up to 416 wire bond, up to 50% more with TAB
- Power supply: from 2.7V up to 5.25V
- Reduced power consumption: up to 50%
- Mixed low voltage/5V operation with TC163G
- Gate speed: 0.4ns (3.3V, 2-input NAND gate, fanout: 2)
- Output drive: up to 24mA at 5V, up to 12mA at 3V/3.3V
- Slew rate control buffers (5V only)
- Building-block memory, megacells and megafunctions
- Advanced packaging including TAB

Specifications and information herein are subject to change without notice.

TC160G Options				TC163G Options			
Part Number	Gate (1) Complexity	Estimated (2) Usable Gates	Maximum I/O Pads (3) (4)	Part Number	Gate (1) Complexity	Estimated (2) Usable Gates	Maximum I/O Pads (3) (4)
TC160G T1	302,000	210,000	416	TC163G T1	280,000	196,000	400
TC160G T2	235,000	164,000	368	TC163G T2	216,000	151,000	352
TC160G U2	302,000	120,000	416	TC163G S0	280,000	112,000	400
TC160G N5	235,000	94,000	368	TC163G L6	216,000	86,400	352
TC160G H7	177,000	71,000	320	TC163G G0	160,000	64,000	304
TC160G D2	132,000	53,000	280	TC163G B7	117,000	46,800	264
TC160G A8	108,000	43,000	256	TC163G 95	95,000	38,000	240
TC160G 70	70,000	28,000	208	TC163G 59	59,000	23,000	192
TC160G 54	54,000	22,000	184	TC163G 45	45,000	18,000	168
TC160G 41	41,000	17,000	160	TC163G 33	33,000	13,200	144
TC160G 33	33,000	13,000	144	TC163G 26	26,000	10,400	128
TC160G 22	22,000	8,800	120	TC163G 16	16,000	6,800	104
TC160G 16	16,000	6,400	102	TC163G 11	11,000	4,400	86
TC160G 11	11,000	4,400	84	TC163G 06	6,000	2,400	68

Notes: (1) Total gates.
(2) Based on 40% array utilization for double-layer metal and 70% for triple-layer metal. Actual utilization may vary, depending on circuit configuration.
(3) Additional I/O pads may be configured as V_{DD}/V_{SS}, subject to number and drive of output buffers.
(4) Special test methodologies are required for greater than 256 I/O signals.

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Absolute Maximum Ratings (V_{SS} = 0V)

Symbol	Parameter	Rating	Unit
V_{DD}	DC supply voltage	– 0.3 to +7.0	V
V_{IN}	DC input voltage	– 0.3 to V_{DD} +0.3	V
I_{IN}	DC input current	± 10	mA
T_{stg}	Storage temperature	– 40 to +125	°C

Recommended Commercial Operating Conditions (V_{SS} = 0V)

Symbol	Parameter	Rating	Unit
V_{DDB}	DC supply voltage	2.7 to 3.6	V
V_{DDA}	DC supply voltage	4.75 to 5.25	V
T_a	Ambient temperature	0 to +70	°C

DC Electrical Characteristics

Specified at ambient temperature 0 to +70°C

		TC160G/TC163G $V_{DDB\ I/O}$ = 3V/3.3V ± 0.3V			TC163G $V_{DDA\ I/O}$ = 5V ± 5%			
Symbol	Parameter	Condition	Value		Condition	Value		Unit
V_{IH}	High level input voltage							
	TTL level		NA	Min		2.2	Min	V
	TTL level SCHMITT trigger		NA			2.2		
	CMOS level		0.8V_{DDB}			3.5		
	CMOS level SCHMITT trigger		0.8V_{DDB}			4.0		
V_{IL}	Low level input voltage							
	TTL level		NA			0.8		
	TTL level SCHMITT trigger		NA	Max		0.8	Max	V
	CMOS level		0.2V_{DDB}			1.5		
	CMOS level SCHMITT trigger		0.2V_{DDB}			1.0		
I_{IH}	High level input current	V_{IN} = V_{DDB}	–10/10	Min/Max	V_{IN} = V_{DDA}	–10/10	Min/Max	µA
	Input buffer with pull-down	V_{IN} = V_{DDB}	10/200		V_{IN} = V_{DDA}	10/200		
I_{IL}	Low level input current	V_{IN} = V_{SS}	–10/10	Min/Max	V_{IN} = V_{SS}	–10/10	Min/Max	µA
	Input buffer with pull-up	V_{IN} = V_{SS}	200/10		V_{IN} = V_{SS}	–200/10		
V_{OH}	High level output voltage							
	Type B4	I_{OH} = –2mA	2.4		I_{OH} = –4mA	2.4		
	Type B8	I_{OH} = –4mA	2.4	Min	I_{OH} = –8mA	2.4	Min	V
	Type B16	I_{OH} = –8mA	2.4		I_{OH} = –16mA	2.4		
	Type B24	I_{OH} = –12mA	2.4		I_{OH} = –24mA	2.4		
		I_{OH} = –1µA	V_{DDB}–0.05		I_{OH} = –1µA	V_{DDA}–0.05		
V_{OL}	Low level output voltage							
	Type B4	I_{OL} = 2mA	0.4		I_{OL} = 4mA	0.4		
	Type B8	I_{OL} = 4mA	0.4	Max	I_{OL} = 8mA	0.4	Max	V
	Type B16	I_{OL} = 8mA	0.4		I_{OL} = 16mA	0.4		
	Type B24	I_{OL} = 12mA	0.4		I_{OL} = 24mA	0.4		
		I_{OL} = 1µA	V_{SS}+0.05		I_{OL} = 1µA	V_{SS}+0.05		
I_{OZ}	High impedance leakage current		–10/10			–10/10		
	Output buffer with pull-up	V_{OUT} = V_{DDB} or V_{SS}	–200/–10	Min/Max	V_{OUT} = V_{DDA} or V_{SS}	–200/–10	Min/Max	µA
	Output buffer with pull-down	V_{OUT} = V_{DDB} or V_{SS}	10/200		V_{OUT} = V_{DDA} or V_{SS}	10/200		
VH	SCHMITT trigger hysteresis voltage							
	TTL level		NA	Typ		0.5	Typ	V
	CMOS level		1.0			1.5		
I_{DDS}	Quiescent supply current	V_{IN} = V_{DDB} or V_{SS}	60(1)	Max	V_{IN} = V_{DDA} or V_{SS}	100(1)	Max	µA

Note: (1) Design dependent.

TC160G/TC163G Series Library

The cells are compatible with TC110G, TC140G and TC160G series macrocells and macrofunctions. Some cells cannot be used for low voltage TC160G operation. These cells include all TTL level input macrocells and slew rate control buffers.

Macrocells

- Macrocell performance optimization (standard/high drive)
- Macrocells equivalent to SSI/MSI

Megafunctions

- Multiplier, Barrelshifter, ALU
- LSI/VLSI CPU peripheral

Building-block memory (32 to 16K bit)

- RAM cell
- Customer-defined architecture

Macrocells

Two drive options—standard and power—are available

Function	Types
Logic gate	62
Inverter/internal buffer	24
Tri-state internal buffer	6
Delay buffer	6
Latch	21
Flip-flop	36
Scan flip-flop	14
Decoder	8
Multiplexer	14
Adder	6
Oscillator	8
Total	**205**

I/O Macrocells

TC160G/TC163G Low Voltage

Function	Types
Input buffer	21
Output buffer	24
Bidirectional buffer	56

TC163G, 5V

Function	Types
Input buffer	27
Output buffer	24
Bidirectional buffer	112

Memory

RAM-C single port RAM

- Asynchronous
- Separated I/O, 3 state output
- Max. 4608 bit/block (8 ~ 256 word x 4 ~ 36 bit)
- Read access time (t_{ACC}) 10ns typ.

RAM-I dual port RAM

- Asynchronous
- 1 read 1 write
- Max 9216 bit/block (8 ~ 256 word x 4 ~ 36 bit)
- Read access time (t_{ACC}) 10ns typ.

RAM-E triple port RAM

- Asynchronous
- 2 read 1 write
- Max. 2304 bit/block (16 ~ 64 word x 4 ~ 36 bit)
- Read access time (t_{ACC}) 8ns typ.

ROM

- Contact Toshiba

Macrofunctions

Functions	Types	
	74HC Series Compatible	Other
Adders	1	4
Comparators	2	6
Counters	11	19
Decoders	4	10
Flip-Flops	6	–
Gates	16	–
Multiplexes	10	11
Registers	16	19
Others	7	8
JTAG Cells	–	12
Total	**73**	**89**

Megafunctions

XADD32
- 32-bit binary full adder
- 830 gates (max.)

XALU32
- 32-bit ALU
- 1090 gates (max.)

XMPY8
- 8 x 8 bit parallel multiplier
- 980 gates (max.)

XMPY16
- 16 x 16 bit parallel multiplier
- 3020 gates (max.)

XBRL16
- 16-bit barrel shifter
- 320 gates (max.)

XBRL32
- 32-bit barrel shifter
- 630 gates (max.)

XFIxxyy
- First-in, first-out memory
- 16K gates (max.)

XPIT (under development)
- Programmable internal timer
- 3300 gates (max.)

XPPI8 (under development)
- Programmable peripheral interface
- 1300 gates (max.)

XUART (under development)
- Universal async receiver transmitter
- 2100 gates (max.)

Range of packages available or in development include:

- Ceramic PGA: 68 to 224
- Ceramic cavity down PGA: 155 to 391 (TC160G only)
- PLCC: 68 to 84
- Plastic flat pack: 44 to 304
- Ceramic flat pack cavity up: 100 to 304
- Ceramic flat pack cavity down: 120 to 304
- Tape carrier package (TCP): 92 to 432
- Thin flat pack: 144 to 176

New package combinations are being added—so for the latest on package availability ask for our packaging data sheet.

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