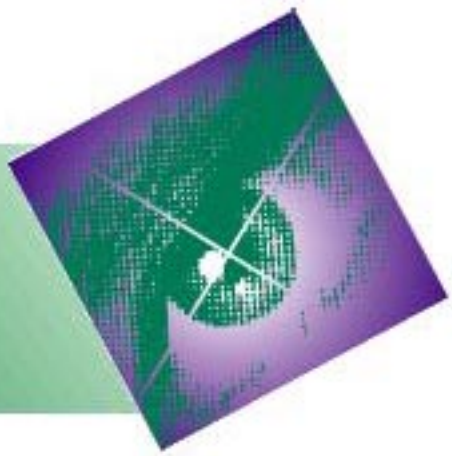
Bt261

30 MHz Pixel Clock Monolithic CMOS HSYNC Line Lock Controller



The Bt261 HSYNC Line Lock Controller is designed specifically for image capture applications.

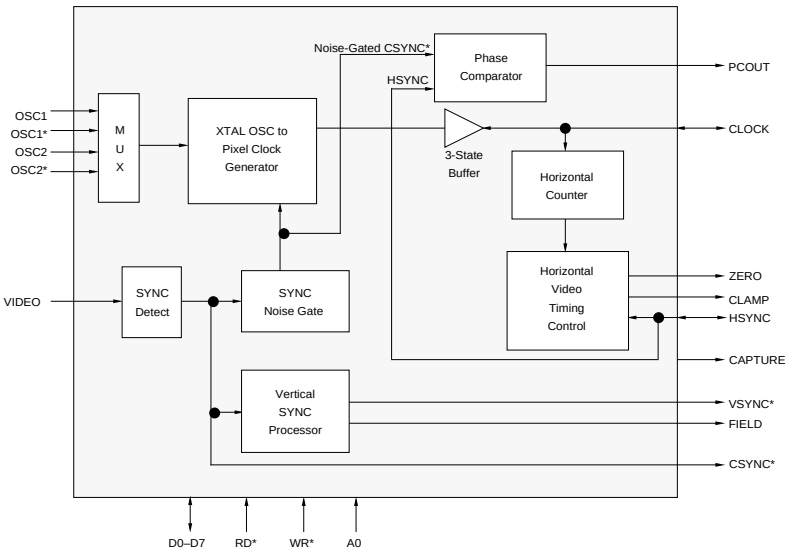
Either composite video or TTL composite sync information is input via VIDEO. An internal sync separator separates horizontal and vertical sync information. Programmable horizontal and vertical video timing enables recovery of both standard and nonstandard timing information.

An external VCO may be used in conjunction with the on-chip phase comparator for implementation of clocks locked to the horizontal frequency.

Alternately, a high-speed clock (OSC) may be divided down to generate the pixel clock. The phase of the generated pixel clock is adjusted to align with the noise-gated CSYNC. The higher the OSC clock rate, the lower the pixel clock jitter (the maximum being one half the OSC clock period). The OSC inputs may be configured to be either TTL or ECL compatible. Thus, four TTL clocks, two TTL clocks and one differential ECL clock, or two differential ECL clocks may be used. The ECL clock inputs are designed to be driven by 10KH ECL using a single +5 V supply.

The CLAMP and ZERO outputs are programmed by the MPU to DC restore the video signal and to zero the Image Digitizer or A/D converter at the appropriate time.

Functional Block Diagram



Distinguishing Features

- Programmable 12-bit Video Timing
- Bidirectional HSYNC and CLOCK Pins
- Horizontal Sync Noise Gating
- External VCO Support
- Standard MPU Interface
- TTL Compatible
- + 5 V Monolithic CMOS
- 28-pin PLCC Package
- Typical Power Dissipation: 300˙mW

Applications

- Image Processing
- Video Digitizing
- Desktop Publishing
- Graphic Art Systems

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Ordering Information

Model Number	Package	Ambient Temperature Range
Bt261KPJ	28-pin Plastic J-lead	0° to +70°C

Print date: September 1993

PRINTED IN THE UNITED STATES OF AMERICA

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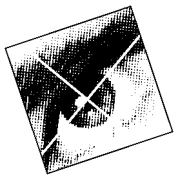


CIRCUIT DESCRIPTION

MPU Interface

As seen in the functional block diagram, the Bt261 supports an MPU interface via (D0–D7, RD*, WR*, and A0). MPU operations are asynchronous to the clocks. Refer to the Timing Waveforms section for further information.

A0 is used to select either the internal 5-bit address register (A0 = logical zero) or the control register specified by the address register (A0 = logical one). ADDR5–ADDR7 are ignored during MPU write cycles, and are in an unknown state when read by the MPU. ADDR0 corresponds to D0 and is the least significant bit. ADDR0–ADDR4 increment following any MPU read or write cycle to a control register other than the address register. MPU write cycles to reserved addresses are ignored and MPU read cycles from reserved addresses return invalid data.

Table 1 shows the internal register addressing.

Table 1. Internal Register Addressing

ADDRO - ADDR4	Addressed by MPU
$00	command register_0
$01	command register_1
$02	command register_2
$03	command register_3
$04	VSYNC sample register
$05	OSC count low register
$06	OSC count high register
$07	status register
$08	HSYNC start low register
$09	HSYNC start high register
$0A	HSYNC stop low register
$0B	HSYNC stop high register
$0C	CLAMP start low register

Table 1. Internal Register Addressing

ADDRO - ADDR4	Addressed by MPU
$0D	CLAMP start high register
$0E	CLAMP stop low register
$0F	CLAMP stop high register
$10	ZERO start low register
$11	ZERO start high register
$12	ZERO stop low register
$13	ZERO stop high register
$14	FIELD gate start low register
$15	FIELD gate start high register
$16	FIELD gate stop low register
$17	FIELD gate stop high register
$18	noise gate start low register
$19	noise gate start high register
$1A	noise gate stop low register
$1B	noise gate stop high register
$1C	HCOUNT low register
$1D	HCOUNT high register
$1E	reserved
$1F	reserved

Video Input / Sync Detector

Either an AC-coupled video signal or a DC-coupled TTL-compatible composite sync signal may be input via the VIDEO input pin (negative-going sync polarity). When AC coupled, the clamping circuitry attempts to force the VIDEO pin voltage during sync tips to VCC/2.

Command register_0 specifies the threshold above the sync tip to use for sync detection. If the sync tip on VIDEO is below the selected threshold, composite sync information is detected and output onto CSYNC* with no pipeline delay and asynchronous to the pixel clock.

Typically, the VIDEO input will be connected to the TTL-compatible CSYNC* output of the Bt252/254 Image Digitizer, and the highest sync slicing level will be selected.

Horizontal Counter

The rising edge of pixel clock (CLOCK) increments a 12-bit horizontal counter used to generate horizontal video timing information. The value of the counter is compared to various registers to determine when signals are to be asserted (set high) and negated (set low). $000 corresponds to the falling edge of CSYNC*. When the part is used with an external high-speed oscillator and divided down to generate the pixel clock, there is no pipeline delay between CSYNC* and count zero. However, when the part is used in phase locked loop mode with an external VCO, there is a three-pixel-clock pipeline delay between CSYNC* and count zero.

Horizontal Sync Separation

The Bt261 separates horizontal sync information from CSYNC* by use of the horizontal noise gate register, which derives gated composite sync by removing equalization and serration pulses at half-line intervals.

Two 12-bit noise gate start and stop registers specify at what horizontal count (with pixel clock resolution) to respectively ignore or accept falling sync transitions on CSYNC*.

The sync noise gating is provided to filter incorrect horizontal sync information from noisy video signals. The noise gating also serves a second purpose: to filter serration and equalization pulses at half-line intervals from CSYNC* during the vertical retrace interval. This enables steady synchronization of horizontal sync information during vertical retrace intervals.

HSYNC Input/Output

The HSYNC output may be programmed to be either active high or active low. The start value sets the rising edge and the stop value sets the falling edge of HSYNC relative to count zero of the horizontal counter. The beginning or falling edge of HSYNC is typically programmed to be coincident with the beginning of the noise-gated CSYNC*.

The HSYNC output may be three-stated via the command register.
HSYNC may also be configured as an input, enabling external circuitry to generate HSYNC and drive the phase comparator.

VSYNC* Output

The VSYNC register defines the clock count from the falling edge of nongated CSYNC* at which point CSYNC* is sampled to determine if the video signal is in the vertical interval. Since nongated CSYNC is used to start the VSYNC counter, two samples per horizontal line are taken during the vertical interval because of equalization and serration pulses.

For each scan line that the sample is a logical zero, the VSYNC* output is a logical zero. Thus, the VSYNC sample register should be programmed so that the sample occurs well after the end of CSYNC* and before subsequent equalization/serration pulses. VSYNC is output on the rising edge of PCLK.

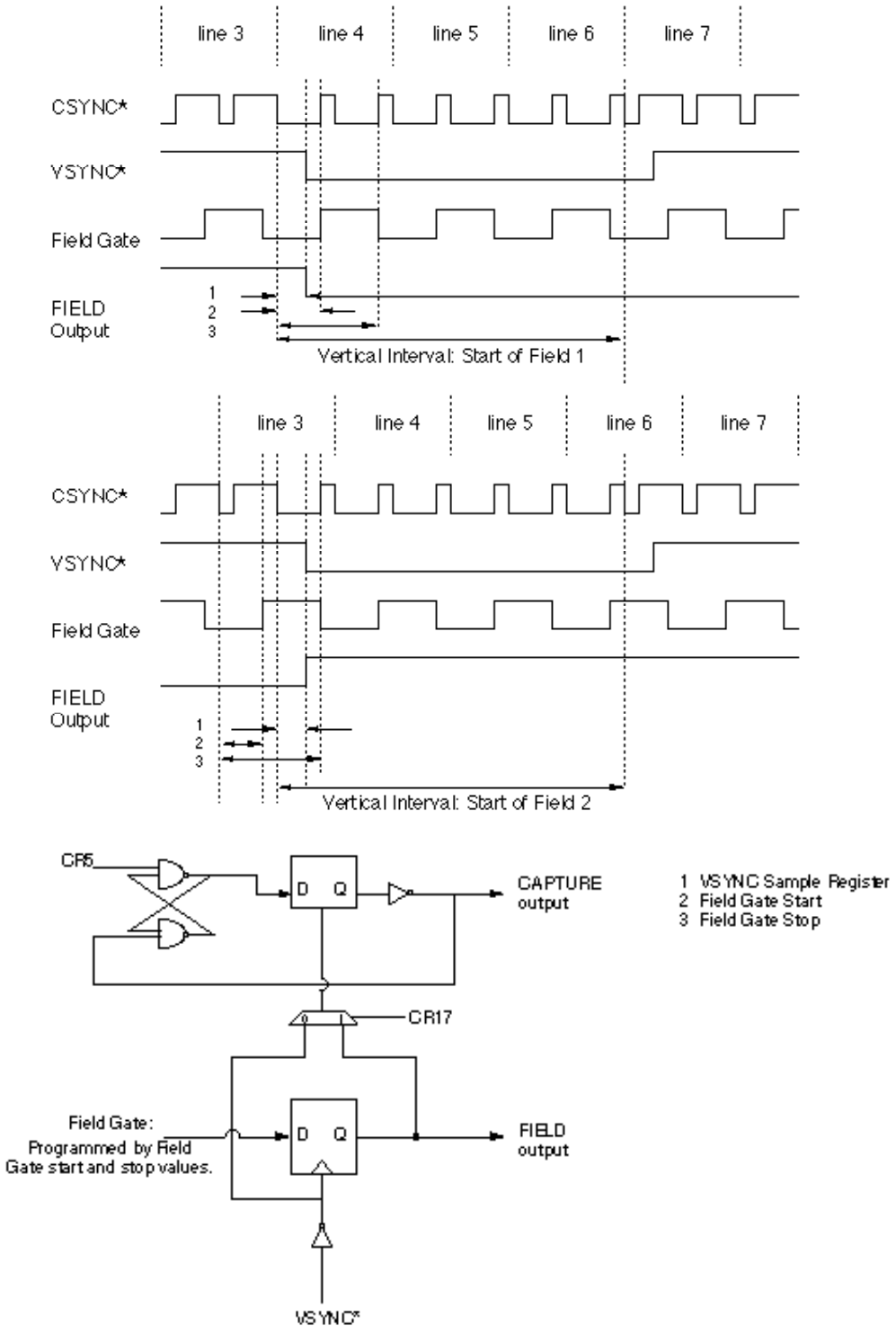
FIELD Output

The FIELD output is derived from the vertical sync information. By positioning the FIELD gate start/stop values a half-line interval apart, the half-line delay in vertical sync during the second field's vertical interval can provide a signal to distinguish the fields.

The FIELD output is clocked by VSYNC*. Therefore, FIELD start and stop values should not coincide with VSYNC or VSYNC + HCOUNT/2. The FIELD GATE start and stop values define the clock count, from the beginning of the horizontal counter, at which to set the input to a register high (start value) or low (stop value). This register is clocked by VSYNC, which occurs half a line later in the transition from field 1 to field 2. The FIELD start and stop values must be separated by, approximately, HCOUNT/2, so that opposite states are reported on subsequent fields. The polarity is such that, with the FIELD GATE start value programmed less than the stop value, FIELD output is toggled high to indicate the beginning of field 1 and toggled low to indicate the beginning of field 2. The polarity of the FIELD pin may be inverted by swapping the start and stop register values.

Figure 1 illustrates the operation of the FIELD gate and FIELD output.

Figure 1. Operation of FIELD and CAPTURE Outputs



CLAMP and ZERO Outputs

The CLAMP and ZERO outputs are provided to control the clamping and zero timing of the A/D converter or Image Digitizer. The start and stop timing is programmable by the MPU (in pixel clock cycles). ZERO is used to autocalibrate the comparators of the A/D converter or Image Digitizer. CLAMP is used to DC-restore the video signal. Both CLAMP and ZERO may be programmed to be either active high or active low.

Capture Output

The Bt261 outputs a CAPTURE signal, which is a command register bit (CR05) synchronized to the vertical sync or FIELD signals.

To capture a single frame of video in an interlaced system, the MPU resets the capture bit (CR5) low, then sets it high before the next rising edge of field. At the rising edge of FIELD, the CAPTURE output will be set to a logical zero until the next rising edge of FIELD (one frame time), when the CAPTURE output is set high.

In a non-interlaced system, the MPU resets the capture bit (CR5) low, then sets it high before the falling edge of VSYNC*. When the falling edge of VSYNC* occurs, the capture output will be set high until the next falling edge of VSYNC*.

External VCO Pixel Clock Generation

An external VCO or pixel clock may be used to drive the Bt261, as shown in Figure 2. The pixel clock signal (from the VCO if one is used) is connected to any one of the OSC input pins (the one used must be selected by command bits CR00–CR02). When the clock pin is configured as an input, it must also be driven by the pixel clock signal. The VCO must have positive control voltage (positive voltage forces a higher frequency).

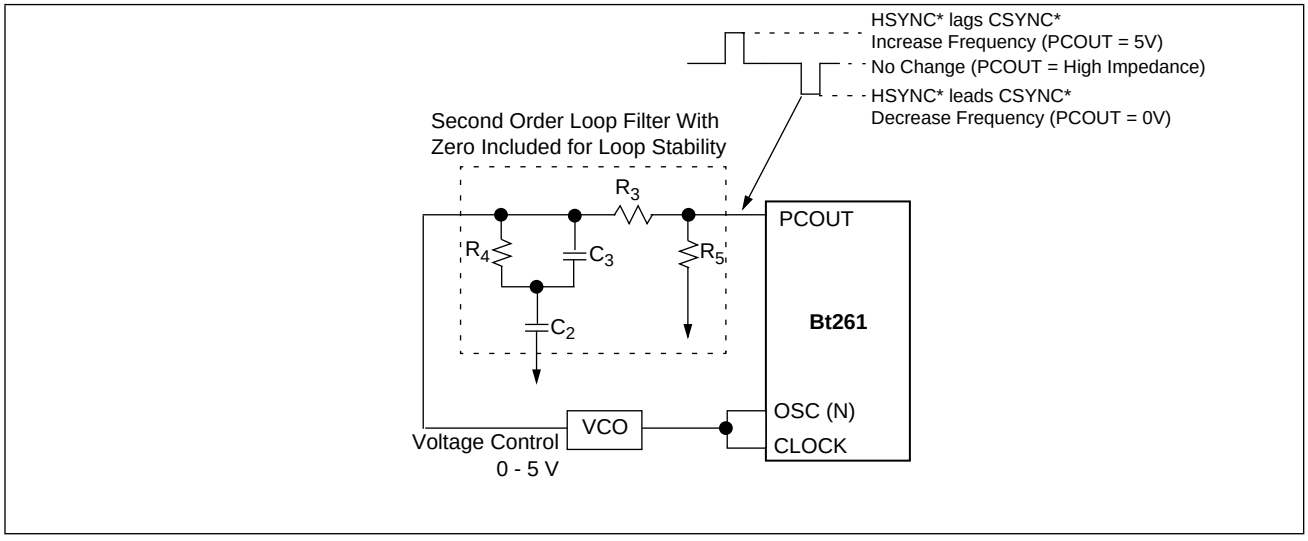
An on-chip phase comparator is available to compare the phase of HSYNC and the falling edge of the noise-gated CSYNC*.

If the falling edge of the noise-gated CSYNC* occurs before the falling edge of HSYNC, the phase comparator "dumps" a charge onto an external capacitor, increasing the VCO frequency. If the falling edge of noise-gated CSYNC* occurs after the falling edge of HSYNC, the phase comparator "sinks" a charge from the external capacitor, decreasing the VCO frequency. Because of the internal delay elements, the phase comparison occurs approximately 500 ns after the falling edge of CSYNC*.

The output of the phase comparator is PCOUT and it is a TTL-compatible three-statable output, which assumes a high-impedance state outside the phase-comparison window. The width of the output pulse on PCOUT is equal to the phase difference with a gain of 4π/VCC.

The "divide-by-N" for the PLL loop is the 12-bit HCOUNT register. Command register bits CR07 and CR06 must be set to (1,0) for proper operation. This configures the horizontal counter to be reset to zero upon reaching the HCOUNT value, which should be set to the number of pixels per line, minus 1.

Figure 2. External VCO Configuration.



Phase/Frequency Detector Operation

The phase comparator compares the phase of the falling edge of the noise-gated CSYNC* and generated HSYNC. The HSYNC can be either internally generated (and optionally output onto the HSYNC pin) or an external HSYNC signal can be input via the HSYNC pin.

Two Forms of Noise Gating Available

The Bt261 offers two forms of noise gating to remove half-line serration and equalization pulses during the vertical interval, which can cause loop disturbances and wavering at the beginning of the displayed field. The first is a digital noise gate that is programmed in pixel clock events following the falling edge of composite sync. The noise-gate start must occur before the halfway point (HCOUNT/2). The noise-gate stop value must relate to a clock count a maximum distance from the end of line, defined as one half the minimum width of the serration pulse, less 500 ns. One half the equalization pulse provides the maximum error deviation for correct phase comparison. The 500 ns delay is required because of the offset used during phase limiting. Even when phase limiting is disabled, this delay is included in both the noise-gated CSYNC* and generated HSYNC* paths. Therefore, it must be accounted for in the noise-gate stop value (see Figure 3 [a–d]). The earliest possible noise-gate stop value permits the widest phase-error tracking range. For an acquisition range greater than one half the minimum equalization pulse width (±2.3 µs or 3.6 percent of nominal RS170A), the noise gate should be set transparent by programming a start value greater than HCOUNT and a stop value less than HCOUNT until lock is verified in the active field. The status registers can be monitored to verify lock.

A second analog noise gate is activated through the phase-limit feature. This function limits the duration of phase correction to about 500 ns per coincidence of noise-gated CSYNC* and generated HSYNC. The Phase Frequency Detector (PFD) makes its comparison about 500 ns after each falling transition of either HSYNC or CSYNC*. However, with phase limiting enabled, the comparison occurs only for a 500 ns interval while both signals are low. Thus, by limiting phase comparison to a 500 ns window, transitions at half-line intervals are not detected. The phase truncation that occurs when this feature is used limits the instantaneous phase-error impulse to about 500 ns that the loop can track. This may not be adequate for some video signal sources, such as heterodyne VCRs (without time-base correction) or electronic still photography (e.g., floppy disk) cameras. If the Bt261 is programmed to permanently phase limit (CR22 set low), the phase-comparison duty is only ~0.8 percent and loop settling time is prolonged dramatically. Figure 3, Figure 4, and Figure 5 are block diagrams and examples demonstrating noise gating and phase limiting.

Both forms of noise gate can be used together for maximum acquisition range with phase-error impulse tracking up to ~3.6 percent of the line rate (the maximum depends upon the minimum width of serration pulses). For an acquisition range that exceeds ±2.3 µs, the digital noise gate must be set transparent by temporarily setting noise-gate start value greater than HCOUNT with a stop value less than HCOUNT. Acquisition can then be automatic and the phase-limit feature (CR10 = CR22 = 1) can be used with phase-lock pixel count (CR27–CR24) programmed for less than 500 ns and the phase-lock line count (CR37–CR30) programmed for less than the field line count, minus the closed-loop settling time. When phase lock is verified (by strobing CR10 low and reading back SR0 = 1 or monitoring SR05), the digital noise-gate can be reactivated by restoring the noise-gate start value to less than HCOUNT/2. When the digital noise gate is active, the phase-limit feature should be disabled for maximum phase-error tracking range (determined by the phase-lock loop's closed-loop impulse response, but limited by one-half minimum serration pulse or noise-gate width). If instantaneous phase errors exceed phase-lock pixel count, the status register SR00 bit is forced to zero, even though the loop may be tracking the phase-error impulses. Since large phase errors usually occur in the vertical blanking interval, it is prudent to reset and monitor the lock status bit after the phase-lock line count has expired in the active field. A consistent zero in SR00 would dictate restarting the acquisition sequence outlined above to maintain phase lock. Similarly, SR05 may be monitored to determine locking status.

Figure 3. (a) Actual Gate-Level Implementation of Phase Limiting and Noise Gating (b,c, and d) Minimized Block Diagrams Corresponding to Waveforms in Figure 5

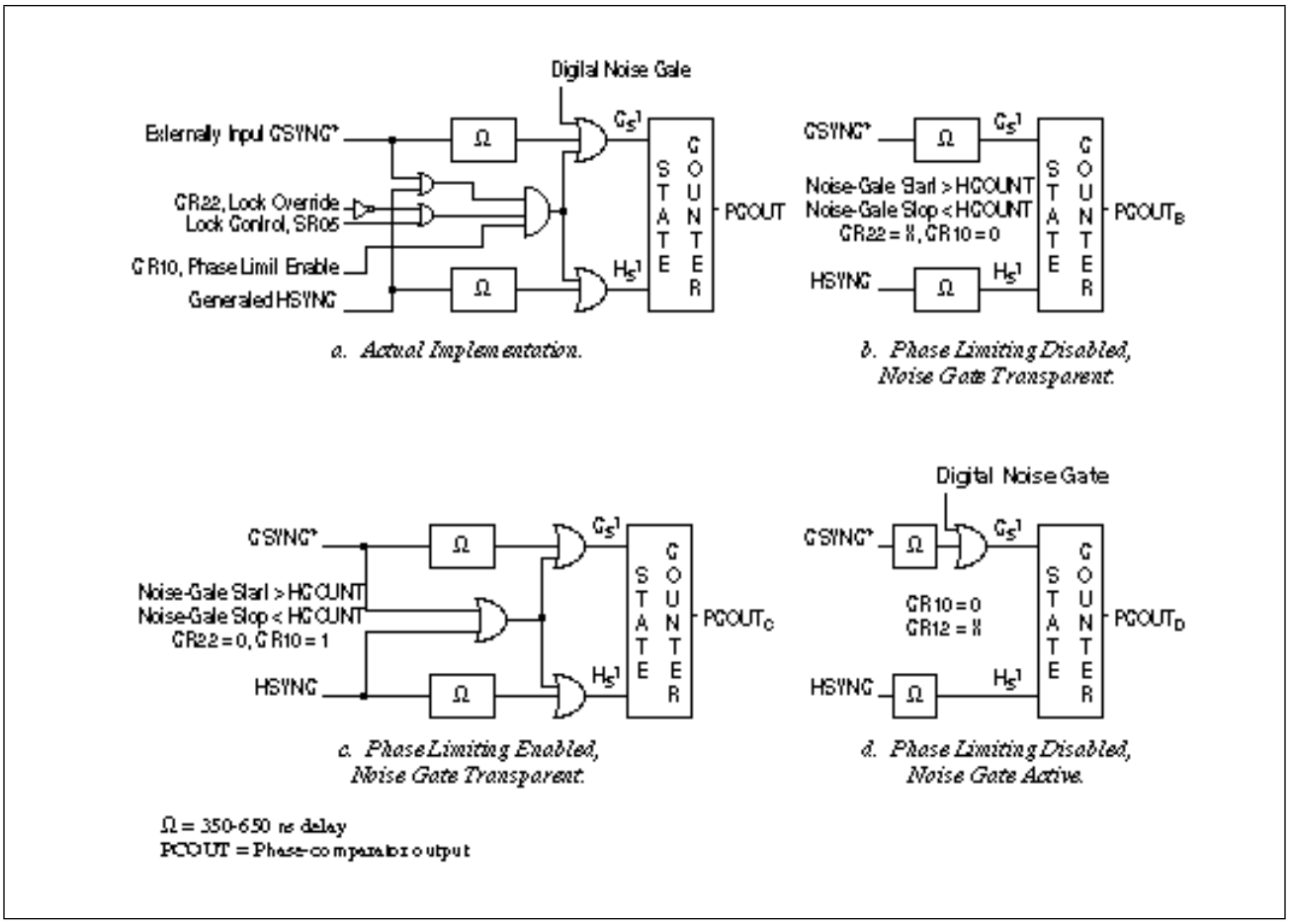


Figure 4. Phase-Comparator State Diagram

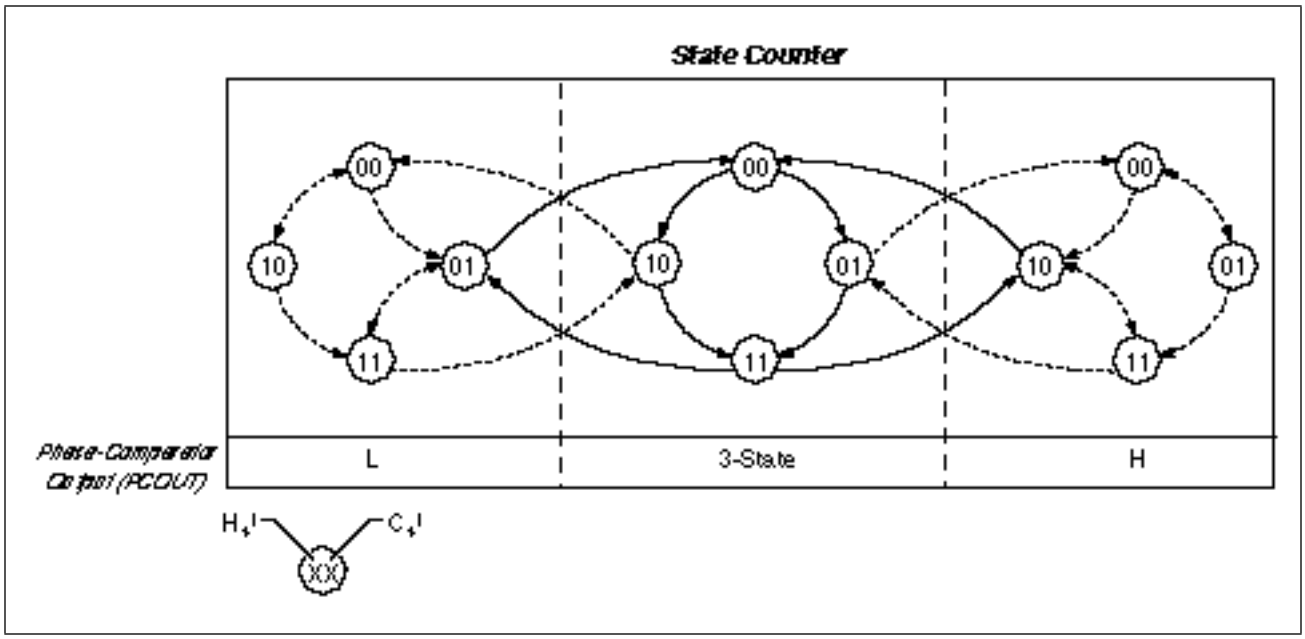
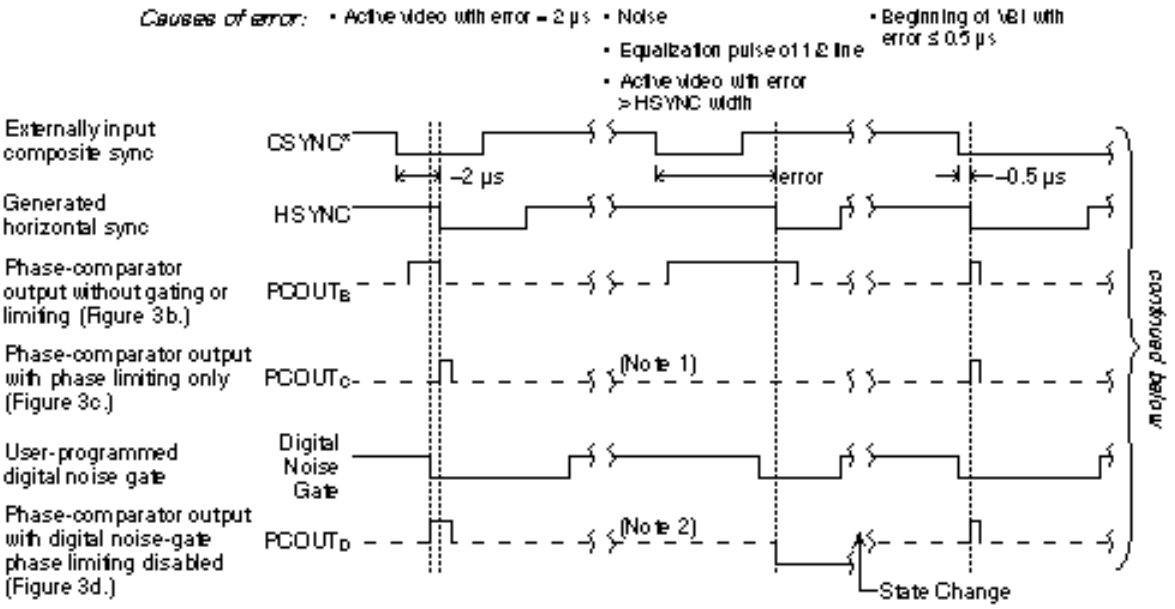
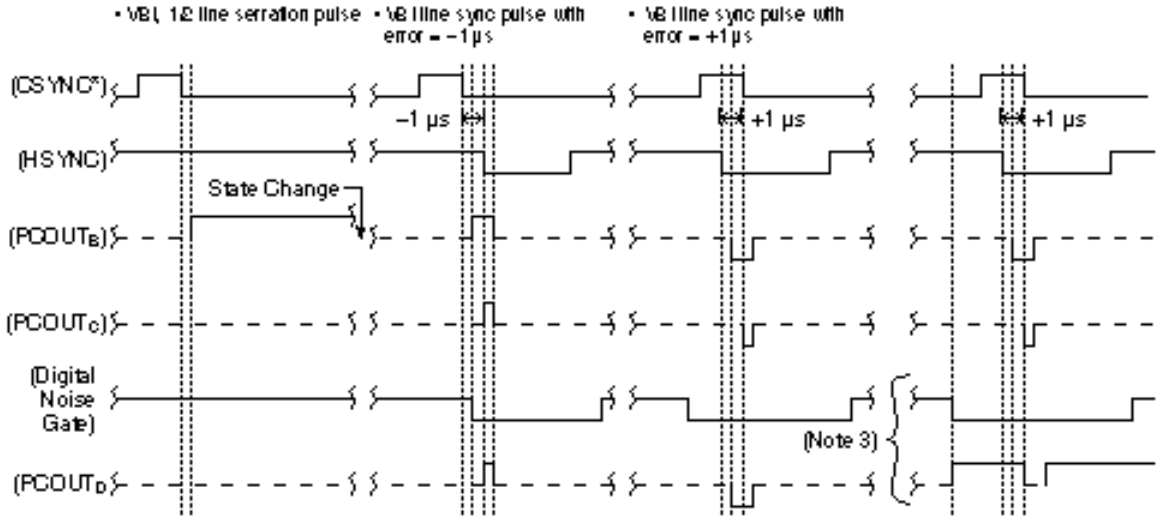


Figure 5. Examples of Phase Comparator Operation With Different Types of Error and Different Implementations of Phase Limiting and Noise Gating





VBI = Vertical Blanking Interval

Note 1: Phase limiting will not adjust for errors greater than HSYNC width, correctly ignoring half-line equalization pulses.

Note 2: The digital noise gate will activate the phase comparator correctly but not deactivate, which would improperly set the VCO input voltage.

Note 3: This is an improperly programmed digital noise gate with erroneous phase-comparator output. Noise-gate stop value is not within 500 ns of the end of line.

In general, the digital noise gate will improperly activate the phase-comparator if the error in the VBI is greater than ± 1/2 serration pulse width.

The Status Registers SR00 and SR05 Used in Automatic Phase Limiting

Bits 0 and 5 of the status register can be used to debug phase-locked-loop operation of the Bt261. Phase-lock pixel-count bits CR27–CR24 define a pixel count used by the Bt261 to determine if the part is in "Lock." The Bt261 compares the time during which the phase comparator is active (the PLL correction time) with the time defined in pixel count. If the compare time is less than phase-lock pixel count, the loop is considered locked and SR00 is not altered. If the compare time is greater than the phase-lock pixel count, SR00 is reset to zero. Previous to query, SR00 must be set to one by writing to command bit CR12.

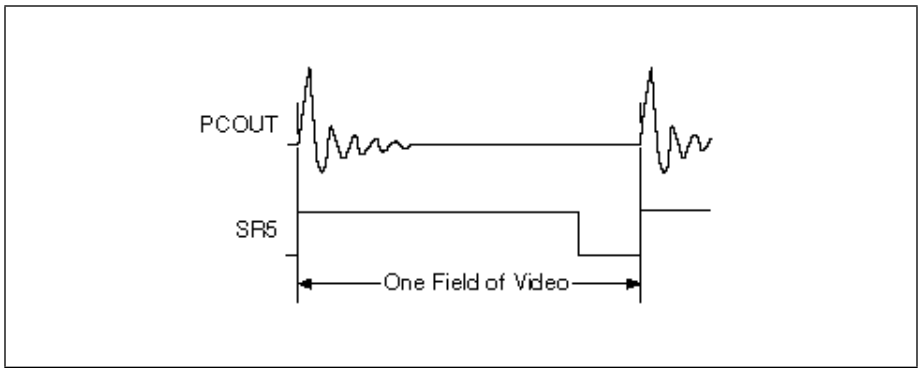
CR37–CR30 contains the phase-lock line count. This register determines the number of lines that must have a phase error less than that defined in the CR27–CR24 phase-lock pixel count for the system to be considered continuously locked. SR05 is reset to zero if there have been phase-lock line-count number of continuous lines with phase error less than that defined in the phase-lock pixel count. SR05 cannot be altered by the MPU. SR05 is set to one if SR00 is set to zero on any line (indicating a phase error greater than that defined in phase-lock pixel count).

Bit 5 of the status register is used by the phase-limiting circuitry to determine if phase limiting should be enabled or disabled. If phase limiting is automatic, i.e., when phase limiting is enabled and lock is not overridden, (CR10 = CR22 = 1), SR05 determines whether phase limiting should be performed. SR05 is the lock control indicated in Figure 3a.

The active period compared with the value in CR27–CR24 is output directly from the phase comparator. Because of this, all digital noise-gate and phase-limit operation is included when the phase error is compared with the phase-lock pixel-count value. Therefore, the value in CR27–CR24 must be less than 500 ns in the typical case or 350 ns in the worst case commercial temperature range. This requirement ensures that a phase-limited line is not incorrectly interpreted as a locked line.

SR05 can be used as a PLL debug tool. If the status register is addressed and the RD* pin of the Bt261 is held low, then SR05 will indicate the lock status. This bit will set low when lock is held for the number of lines defined in the phase-lock line count. When this condition is observed while the phase-comparator output is viewed through two vertical intervals, the Bt261 response relative to the loop performance can be studied. Lock should be indicated well before the next vertical interval (see Figure 6). Phase-limit enable must be deactivated during this evaluation (CR10 = 0); otherwise, phase limiting will affect the ability to monitor the loop-acquisition time.

Figure 6. PLL Performance Can Be Monitored Using SR05



Asynchronous (Unlocked) Pixel Clock Generation

Four oscillator clock inputs are provided (OSC), selectable by the MPU, configurable as either TTL or differential ECL inputs (designed to be driven by 10KH ECL using a single +5 V supply).

The selected OSC input is divided down to the desired pixel clock rate and duty cycle. The pixel clock low and high times are programmable by the MPU (as a function of OSC clock cycles) via the OSC count low and high registers. Note that both the rising and falling edge of the OSC inputs are used when specifying the OSC count (for example, values of 2 for the OSC count low and high registers will divide the OSC clock symmetrically by two).

The generated pixel clock is synchronized to the falling edge of the noise-gated CSYNC* each scan line. Each time a horizontal sync is detected on the VIDEO input, the CLOCK output is resynchronized by the OSC clock so that the beginning of a pixel clock cycle and the falling edge of the noise-gated CSYNC* are coincident (see Figure 7) within one half the period of the OSC input. While there is some sampling jitter on CLOCK associated with the falling edge of CSYNC*, the residual jitter in the remaining line interval is strictly a function of the OSC clock source jitter, symmetry, and amplitude/slew rate jitter, at the OSC input. Differential OSC signals of fast edges will minimize the latter contribution.

There are three ways of controlling the horizontal counter, as determined by command bit CR07 and CR06.

CR07 and CR06 are (0,1): if a falling edge of the noise-gated CSYNC* does not occur before the number of pixel clock cycles specified by HCOUNT, the horizontal counter stops at the HCOUNT value and is held there until the next falling edge of the noise-gated CSYNC*, at which time it is reset to zero. CLOCK stops in the high state at the HCOUNT value, until the next falling edge of the noise-gated CSYNC*.

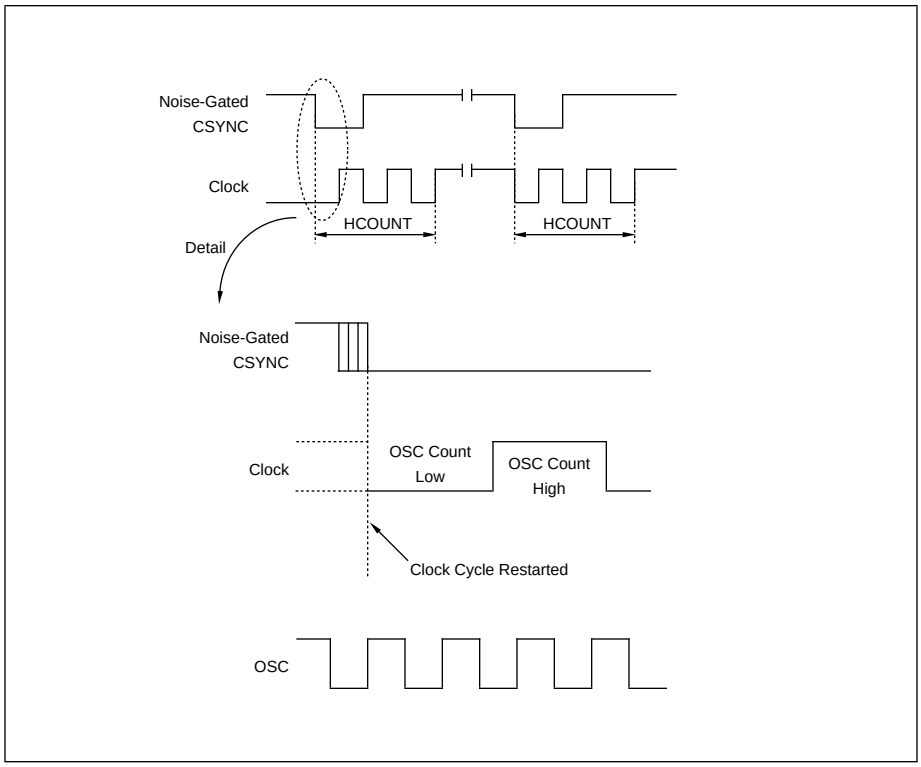
If a falling edge of the noise-gated CSYNC* occurs before the number of pixel clock cycles specified by HCOUNT, the horizontal counter is reset to zero by the falling edge of the noise-gated CSYNC*. CLOCK will be continuous and is re-synchronized to each falling edge of the noise-gated CSYNC*. This mode is used if the number of pixel clock cycles per scan line is known and is a fixed number.

CR07 and CR06 are (1,1): if a falling edge of the noise-gated CSYNC* does not occur before the number of pixel clock cycles specified by HCOUNT, the horizontal counter is reset to zero upon reaching HCOUNT, and begins incrementing again, until the next falling edge of the noise-gated CSYNC* or HCOUNT value is reached. CLOCK is continuous and is resynchronized to each falling edge of the noise-gated CSYNC*.

If a falling edge of the noise-gated CSYNC* occurs before the number of pixel clock cycles specified by HCOUNT, the horizontal counter is cleared at the falling edge of the noise-gated CSYNC*, and begins incrementing again, until the next falling edge of the noise-gated CSYNC* or HCOUNT value is reached. CLOCK will be continuous and is resynchronized to the falling edge of the noise-gated CSYNC*. This mode is used if the number of pixel clock cycles per scan line is not known or an arbitrary value is to be used.

CR07 and CR06 are (1,0): Resets H counter at HCOUNT only.

Figure 7. Pixel Clock Output Timing When Generated From Higher Speed Oscillator



Pin Descriptions

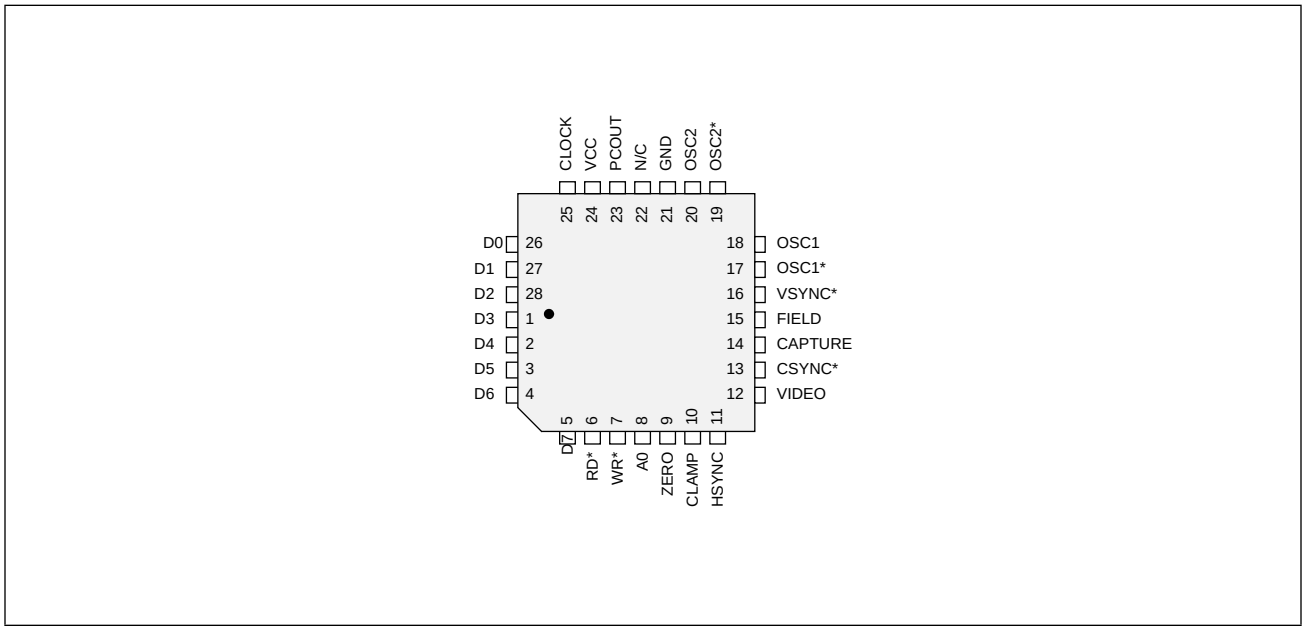
Table 2. Pin Descriptions Grouped By Pin Function

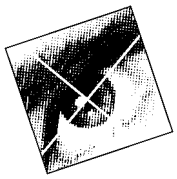
Pin Name	Description
HSYNC	Horizontal sync input/output (TTL compatible). As an output, HSYNC is programmed to be either a logical zero or logical one during the desired horizontal sync interval. It is output following the rising edge of CLOCK. As an input, it is input into the phase comparator asynchronously to the clocks with no pipeline delays.
VSYNC*	Vertical sync output (TTL compatible) with a negative composite sync output. VSYNC* is a logical zero for scan lines during detected vertical sync intervals on the VIDEO input. It is output following the rising edge of CLOCK.
CSYNC*	Composite sync output (TTL compatible). CSYNC* is a logical zero during negative composite sync intervals detected on the VIDEO input. It is output asynchronous to the clocks with no pipeline delays.
ZERO	Zero output (TTL compatible). This output is used to control the ZERO input of the image digitizer or A/D converter. It may be programmed to be either active high or active low and is output following the rising edge of CLOCK.
CLAMP	Clamp output (TTL compatible). This output is used to control the CLAMP input of the image digitizer or A/D converter. It may be programmed to be either active high or active low and is output following the rising edge of CLOCK.
FIELD	Even/odd field output (TTL compatible). For interlaced operation, this output (with transitions coincident with the VSYNC* output) indicates whether the current field is even or odd; the polarity is programmable. For noninterlaced operation, this output is always either a logical one or a logical zero, depending on whether it is programmed to be active high or low. It is output on the falling edge of VSYNC*.
PCOUT	Phase comparator output (TTL compatible). This three-state output indicates the phase difference in time between the generated horizontal sync signal (either the internally generated HSYNC or the HSYNC pin) and the recovered horizontal sync signal. High = lags, Low = leads.
VIDEO	Video and composite sync input. Either a DC-coupled TTL composite sync information or an AC-coupled analog video signal (less than 2 V peak-to-peak) may be input via this pin for detection of sync information. Sync information must be of negative polarity.
CLOCK	Pixel clock input/output (TTL compatible). The device may either drive this pin with a generated clock or an external pixel clock may drive this pin. When the CLOCK pin is externally driven, the selected OSC pin must also be driven.
OSC1, OSC1*, OSC2, OSC2*	External clock inputs (TTL or ECL compatible). These inputs are programmed to be either TTL or ECL compatible (10KH differential ECL driven by a single +5 V supply).
CAPTURE	Active video output (TTL compatible). This output is active high for a frame duration and is synchronized to the vertical sync interval and FIELD signal. It is output following the rising edge of FIELD for interlaced, or the falling edge of VSYNC* if non-interlaced.
RD*	Read control input (TTL compatible). If RD* is a logical zero, data is output onto D0–D7. RD* and WR* should not be asserted simultaneously.

Table 2. Pin Descriptions Grouped By Pin Function

Pin Name	Description
WR*	Write control input (TTL compatible). If WR* is a logical zero, data is written into the device via D0–D7. Data is latched on the rising edge of WR*. RD* and WR* should not be asserted simultaneously.
D0–D7	Bidirectional data bus (TTL compatible). MPU data is transferred into and out of the device over this 8-bit data bus. If RD* is a logical one, D0–D7 are three-stated.
AO	Address control inputs (TTL compatible). A0 specifies whether the MPU is accessing the address register (A0 = 0) or the control register specified by the address register (A0 = 1).
VCC	Power.
GND	Ground.

Figure 8. Bt261 Pinout Diagram





INTERNAL REGISTERS

Horizontal Counter

The 12-bit horizontal counter is incremented on the rising edge of CLOCK. It is not accessible by the MPU.

Command Register_0

This command register may be written to or read by the MPU at any time and is not initialized. CR00 corresponds to D0 and is the least significant bit.

CR07, CR06	Horizontal counter control (00) reserved (01) reset each noise-gated CSYNC* (10) reset to zero upon reaching HCOUNT (11) use both modes (01) and (10)	A value of (01) forces the horizontal counter to be reset to zero at the beginning of every noise-gated CSYNC*. These modes should be selected when using a high–speed oscillator to divide down and generate the pixel clock. A value of (10) specifies that the horizontal counter will be reset to zero upon reaching the HCOUNT value. This mode should be selected when using the horizontal counter as a simple divide-by-N circuit (such as when using an external VCO in a traditional phase-locked loop application). Mode 11 can be used to correct for missing sync pulses on the input video.
CR05	Capture strobe	This bit is synchronized to VSYNC* and FIELD and output onto the CAPTURE output pin.
CR04, CR03	Sync detect select (00) 25 mV (01) 50 mV (10) 100 mV (11) 125 mV	These bits specify how much above the sync tip to slice VIDEO for sync detection. If inputting TTL sync information, the highest slicing level should be selected.
CR02-CR00	Clock input select (000) TTL compatible OSC1 (001) TTL compatible OSC1* (010) TTL compatible OSC2 (011) TTL compatible OSC2* (100) ECL compatible OSC1, OSC1* (101) ECL compatible OSC2, OSC2* (110) reserved (111) reserved	These bits specify which OSC input is to be used to generate pixel clock information. ECL input selection is compatible with 10KH differential ECL driven by a single +5 V supply. *Note*: When the clock pin is driven, the selected OSC pin(s) must also be driven.

Command Register_1

This command register may be written to or read by the MPU at any time and is not initialized. CR10 corresponds to D0 and is the least significant bit.

CR17	Interlaced or noninterlaced select (0) noninterlaced operation (1) interlaced operation	This bit specifies whether an interlaced or noninterlaced video signal is being digitized. The MPU must write a logical zero followed by a logical one to this bit to reset the status bit (SR00) to a logical one.
CR16	CLOCK output disable (0) drive CLOCK output (1) three-state CLOCK output	This bit specifies whether the CLOCK pin is three-stated (logical one) or is actively driven (logical zero). A logical one enables an external pixel clock to drive the internal counters.
CR15	CSYNC* output disable (0) drive CSYNC* output (1) three-state CSYNC* output	This bit specifies whether the CSYNC* output is three-stated (logical one) or is actively driven (logical zero).
CR14	VSYNC* output disable (0) drive VSYNC* output (1) three-state VSYNC* output	This bit specifies whether the VSYNC* output is three-stated (logical one) or is actively driven (logical zero).
CR13	HSYNC output disable (0) drive HSYNC output (1) three-state HSYNC output	This bit specifies whether the HSYNC output is three-stated (logical one) or is actively driven with the internally generated HSYNC signal (logical zero). If external circuitry is driving the HSYNC pin, this bit must be set to a logical one.
CR12	Reset lock loss status bit (0) set status bit SR00 (1) inactive	This bit sets SR00, which is used to indicate loss of lock. The MPU must write a logical zero to this bit to restart the process.
CR11	Phase comparator input select (0) HSYNC pin (1) internally generated HSYNC	One input to the phase comparator is recovered composite sync. The other input to the phase comparator is specified by this bit to be either the internally generated HSYNC or the HSYNC pin. When an external source is driving the HSYNC pin, this bit should be set to a logical zero.
CR10	Phase limit enable (0) inhibit phase limiting (1) enable phase limiting	If this bit is a logical one, both horizontal sync signals (recovered and either internally or externally generated) must be present to adjust the VCO frequency. If one is missing, the VCO frequency is not adjusted. If this bit is a logical zero, a missing horizontal sync signal will adjust the VCO frequency.

Command Register_2

This command register may be written to or read by the MPU at any time and is not initialized. CR20 corresponds to D0 and is the least significant bit.

CR27, CR24	Phase lock pixel count (0001) 2 clock cycles (1111) 16 clock cycles	These bits specify the maximum number of pixel clock cycles between the falling edge of noise-gated CSYNC* and the HSYNC signal (either internally or externally generated) to be considered locked. If the number of pixel clock cycles between the falling edge of noise-gated CSYNC* and the HSYNC signal exceed this value, lock is considered to be lost for that scan line, and the lock loss status bit (SR00) is set to a logical zero.
CR23	Pixel clock mask enable (0) continuous pixel clock (1) stop pixel clock at HCOUNT	If this bit is a logical one, the CLOCK output is stopped in the logical one state when the horizontal counter reaches the HCOUNT value. This ensures a minimum pulse width when the noise-gated CSYNC* signal is asynchronously sampled. If it is a logical zero, the CLOCK output will continuously clock (if command bit CR16 is a logical zero). This bit is ignored if an external pixel clock is driving the CLOCK pin (command bit CR16 is a logical one).
CR22	Lock override (1) normal operation (0) tell phase comparator it's locked	If the Bt261 goes out of lock, the phase limiter is automatically disabled until it is back in lock. If this bit is a logical zero, this function is overridden.
CR21, CR20	Pixel clock select (00) OSC inputs (01) external pixel clock (10) OSC drives CLOCK direct (11) reserved	These bits specify whether to use the OSC-generated pixel clock or an external pixel clock (driving the CLOCK pin) to clock internal counters. In mode (00), the selected OSC input(s) is divided down by the OSC count registers to generate the pixel clock (CLOCK). If mode (01) is selected, an external pixel clock must drive the CLOCK pin and one of the OSC inputs. Command bit CR16 must be a logical one. If mode (10) is selected, the OSC clock is output directly onto the CLOCK pin. The OSC count low and high registers are ignored.

Command Register_3

This command register may be written to or read by the MPU at any time and is not initialized. CR30 corresponds to D0 and is the least significant bit.

CR37, CR30	Phase lock line count (0000 0000) 1 scan line (0000 0001) 2 scan lines (1111 1111) 256 scan lines	These bits specify the number of consecutive scan lines for which lock must be maintained. If lock is not maintained for the specified number of scan lines, the phase limiter is disabled only if command bit CR22 is a logical one. SR05 is set to zero if lock is maintained for the specified number of scan lines.

VSYNC Sample Register

This 8-bit register specifies the number of pixel clock cycles after the falling edge of nongated CSYNC* at which to sample the CSYNC* signal each scan line. By doing this, two samples per line will be taken during the vertical interval when half-line pulses are present. The FIELD gate is programmed with the horizontal counter values (which use only noise-gated CSYNC*); when sampling of the input sync occurs, VSYNC will toggle one half-line earlier at the beginning of field two as opposed to the beginning of field one. This register may be written to or read by the MPU at any time and is not initialized. Values from $00 (1) to $FF (256) may be specified. A value of 1/8 HCOUNT is recommended (~8 µs for the 15.75 KHz line-rate video). This is different from the 1/4 and 3/4 HCOUNT required for FIELD-gate start and stop values, and greater than the 5 µs maximum width of sync pulses. For a conventional video input with negative-going syncs, this produces a negative-going VSYNC* at the number of clock cycles specified after the falling CSYNC* edge. There is a 3-pixel-clock pipeline delay in clearing the horizontal counter when the part is used in phase-lock loop mode. When the pixel clock is generated by dividing down an external oscillator, this delay is in oscillator clocks. Thus, the output of this signal with respect to CSYNC* may be delayed (see Figure 8).

OSC Count Low and High Registers

These two 4-bit registers specify the number of rising and falling edges of an OSC input the pixel clock output (CLOCK) is to be low and high. Values from $02 (2) to $OE (15) may be specified. These registers may be written to or read by the MPU at any time and are not initialized. A value of $00 results in no pixel clock generation while the OSC inputs are used. The counters clock on both the rising and falling edge of the selected OSC input. For example, values of 4, 4 in OSC count low and high would result in a pixel clock with one fourth the frequency of the oscillator.

Status Register

This status register may be read by the MPU at any time and is not initialized. MPU write cycles to this register are ignored. SR00 corresponds to D0 and is the least significant bit.

SR00	Lock-loss status (pixel count related) (0) lock loss detected (1) reset or no lock loss	This bit reset if loss of lock is indicated. “Loss of lock” is defined as a greater phase error between noise-gated CSYNC* and generated HSYNC* than the phase-lock pixel count (CR27–CR24). It is reset by writing to command bit CR12.
SR05	Lock-loss bit (line-count related) (1) lock loss detected (0) lock detected for at least line-count number of lines	This bit is set if one line of video has a phase error between generated HSYNC and noise-gated CSYNC* greater than that defined by the phase-lock pixel count (CR24–CR27). This bit is reset if there have been phase-lock line count (CR37–CR30) consecutive lines with error less than that defined in the phase-lock pixel count.

Figure 9. Bt261 Suggested Register Settings.

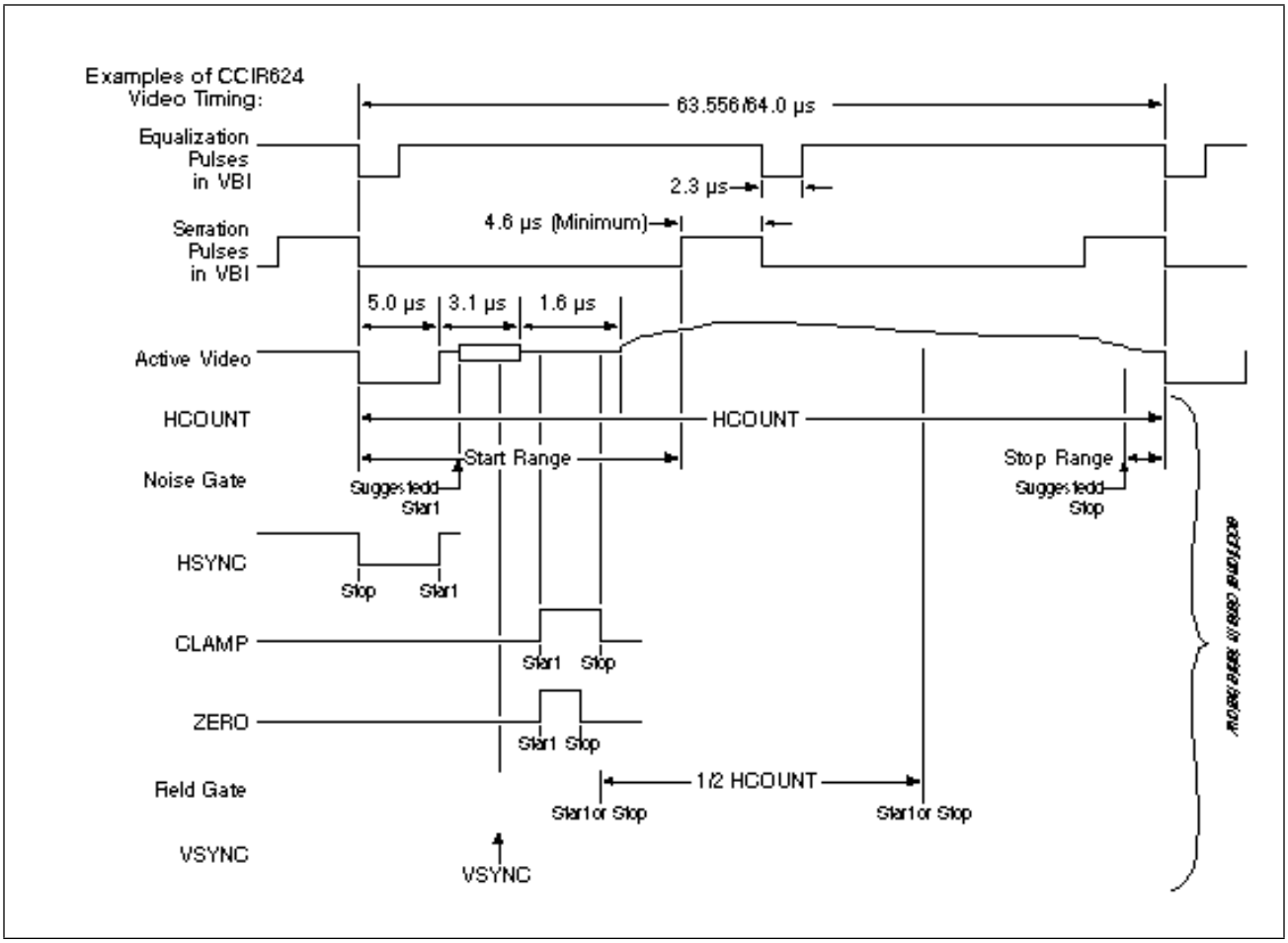


Table 3. Bt261 Suggested Register Settings

Pixel Clock Rate		NTSC(M) 12.2 MHz dec	NTSC(M) 12.2 MHz hex	PAL (B, G, I) 14.75 MHz dec	PAL (B, G, I) 14.75 MHz hex
Line Rate		**63.556 µs**		**64.0 µs**	
(HCOUNT) Number of pixels minus 1		779	30B	943	3AF
(Noise Gate)	Start 7 µs Stop 61.76 µs	88 758	58 2F6	104 917	68 395
(HSYNC) Negative polarity, 4.7 µs wide	Start 4.7 µs Stop 0 µs	59 0	3B 0	70 0	46 0
(CLAMP) One may CLAMP on burst back porch or sync tip	Start 8.5 µs Stop 9 µs	107 113	6B 71	126 134	7E 86
(ZERO)	Start 8.5 µs Stop 8.75 µs	107 110	6B 6E	126 130	7E 82
(Field Gate)	Start 15 µs Stop 45 µs	189 566	BD 236	223 668	DF 29C
(VSYNC) This gives FIELD = 0, 1 for field one and two, respectively	8 µs	98	62	118	76

HSYNC Start and Stop Registers

These two 16-bit registers specify the number of pixel clock cycles after the falling edge of noise-gated CSYNC* at which to assert or negate the HSYNC output. The [start value] specifies the number of CLOCK cycles after the falling edge of noise-gated CSYNC* that the HSYNC output is set high. The [stop value] specifies the number of CLOCK cycles after the falling edge of noise-gated CSYNC* that the HSYNC output is set low. If [start value] = [stop value], HSYNC will remain a constant logical one. Values from $0000 (1) to $0FFF (4096) may be specified. Note that there is a variable pipeline delay between the CSYNC* and HSYNC outputs. There is a 3-pixel-clock pipeline delay in clearing the horizontal counter when the part is used in phase-lock loop mode. When the pixel clock is generated by dividing down an external oscillator, this delay is in oscillator clocks. Thus, output of this signal with respect to CSYNC* may be delayed.

D4–D7 of HSYNC start high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit HSYNC start register is not updated until the write cycle to the HSYNC start high register. Thus, the writing sequence should be [HSYNC start low] [HSYNC start high].

D4–D7 of HSYNC stop high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit HSYNC stop register is not updated until the write cycle to the HSYNC stop high register. Thus, the writing sequence should be [HSYNC stop low] [HSYNC stop high].

	HSYNC Start/Stop High				**HSYNC Start/Stop Low**							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H19	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

CLAMP Start and Stop Registers

These two 16-bit registers specify the horizontal count (in pixel clocks) at which to assert and negate the CLAMP output. The [start value] specifies the number of CLOCK cycles after the falling edge of noise-gated CSYNC* that CLAMP is set high. The [stop value] specifies the number of CLOCK cycles after the falling edge of noise-gated CSYNC* that CLAMP is set low. If [start value] = [stop value], CLAMP will remain a constant logical one. Values from $0000 (1) to $0FFF (4096) may be specified. There is a 3-pixel-clock pipeline delay in clearing the horizontal counter when the part is used in phase-lock loop mode. When the pixel clock is generated by dividing down an external oscillator, this delay is in oscillator clocks. Thus, output of this signal with respect to CSYNC* may be delayed.

D4–D7 of CLAMP start high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit CLAMP start register is not updated until the write cycle to the CLAMP start high register. Thus, the writing sequence should be [clamp start low] [clamp start high].

D4–D7 of CLAMP stop high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit CLAMP stop register is not updated until the write cycle to the CLAMP stop high register. Thus, the writing sequence should be [clamp stop low] [clamp stop high].

	CLAMP Start/Stop High				**CLAMP Start/Stop Low**							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H19	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

A value corresponding to 1 µs after the falling edge of CSYNC* is recommended for the [start] value, and a value of 1 µs before the rising edge of CSYNC* is recommended for the [stop] value if DC restoration is to occur during the horizontal sync interval. If DC restoration is to occur during the back porch interval, a value corresponding to 500 ns after the rising edge of CSYNC* is recommended for the [start] value and a value corresponding to 2.5 µs after the rising edge of CSYNC* is recommended for the [stop] value. For restoration of signals with subcarrier-encoded NTSC or PAL, the 7.8–9.4 µs interval (12–15 percent of HCOUNT) following the color burst may be better for clamping a luminance signal with residual burst.

ZERO Start and Stop Registers

These two 16-bit registers specify the number of pixel clock cycles after the falling edge of noise-gated CSYNC* at which to assert or negate the ZERO output. The [start value] sets this output high at the specified number of CLOCK cycles following the falling edge of noise-gated CSYNC*. The [stop value] sets this output low at the specified number of CLOCK cycles following the falling edge of noise-gated CSYNC*. If [start value] = [stop value], ZERO will remain a constant logical one. Values from $0000 (1) to $0FFF (4096) may be specified. There is a 3-pixel-clock pipeline delay in clearing the horizontal counter when the part is used in phase-lock loop mode. When the pixel clock is generated by dividing down an external oscillator, this delay is in oscillator clocks. Thus, output of this signal with respect to CSYNC* may be delayed.

D4–D7 of ZERO start high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit ZERO start register is not updated until the write cycle to the ZERO start high register. Thus, the writing sequence should be [zero start low] [zero start high].

D4–D7 of ZERO stop high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit ZERO stop register is not updated until the write cycle to the ZERO stop high register. Thus, the writing sequence should be [zero stop low] [zero stop high].

	ZERO Start/Stop High				**ZERO Start/Stop Low**							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H19	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

Since an active high signal is need for the Bt218, Bt252, and Bt254 during non-acquisition intervals, the ZERO output can be programmed to be within the horizontal retrace interval. In addition, these devices produce a significant impulse on their video input following the zero pulse, which can affect clamping stability. So, the pulse is best positioned within the active CLAMP pulse to divert this energy. Both CLAMP and ZERO pins may be driven with the same timing.

FIELD Gate Start and Stop Registers

These two 16-bit registers specify the number of pixel clock cycles after the falling edge of noise-gated CSYNC* at which to start and stop the FIELD gate "window." With the noise gate properly programmed to ignore half-line vertical interval pulses, the VSYNC* transition will occur half a line later during the vertical sync interval between fields one and two (assuming a typical 2:1 interlaced video signal). By programming the FIELD start and stop values to have an interval exceeding half a line (e.g. starting at 1/4 line time and stopping at 3/4 line time), the FIELD output is low during field one if [start value] < [stop value] or high during field one if [start value] > [stop value], with transitions at every falling edge of VSYNC*. If [start value] = [stop value], FIELD will remain a constant logical one. Values from $0000 (1) to $0FFF (4096) may be specified. Field edge coincides with VSYNC* falling edge.

D4–D7 of FIELD gate start high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit FIELD gate start register is not updated until the write cycle to the FIELD gate start high register. Thus, the writing sequence should be [field gate start low] [field gate start high].

D4–D7 of FIELD gate stop high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit FIELD gate stop register is not updated until the write cycle to the FIELD gate stop high register. Thus, the writing sequence should be [field gate stop low] [field gate stop high].

	FIELD Gate Start/Stop High				**FIELD Gate Start/Stop Low**							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H19	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

Values of one fourth HCOUNT and three fourths HCOUNT are recommended for start and stop values, resulting in an active high FIELD output (field one = 1, field two = 0).

Noise Gate Start and Stop Registers

These two 16-bit registers specify the number of pixel clock cycles after the falling edge of CSYNC* at which to force the noise gate to be closed (start value) or open (stop value). If [start value] = [stop value], the noise gate will remain closed. The noise-gate start value should be activated no later than HCOUNT/2. The noise-gate stop value should be within one half the minimum serration pulse width minus 500 ns to the end of the horizontal line. This gating is required because of the state counter that is used to determine the phase comparison output and the 500 ns delay that is used for phase limiting. Because of this stop-value limitation, the digital noise gate can be used to track phase errors no greater than one half the minimum serration pulse width. This translates into 2.3 µs and 0.75 µs (3.6 percent and 1.2 percent of the line rate) for RS170A and RS343, respectively. For example:

Video Source	1/2 Minimum Serration Pulse	261 Gate Delay	Minimum Stop Value From End of Line	Minimum Noise-Gate Stop-Value Time
RS170A	2.3 µs	0,5 µs	1.8 µs	61,76 µs
RS343A	0,75 µs	0,5 µs	0,25 µs	63.31 µs

Note: The Brooktree Applications Handbook and the RS343A and RS170A specifications contain minimum serration pulse widths.

For wideband acquisition, the noise gate should be disabled by programming the start value greater and the stop value less than the number of pixels per line.

Values from $0000 (1) to $0FFF (4096) may be specified. This register should be initialized early to minimize indeterminate outputs during vertical retrace. This register must be properly programmed when the part is used in either phase-lock loop mode or when an external oscillator is resynchronized.

D4–D7 of noise gate start high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit noise gate start register is not updated until the write cycle to the noise gate start high register. Thus, the writing sequence should be [noise gate start low] [noise gate start high].

D4–D7 of noise gate stop high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit noise gate stop register is not updated until the write cycle to the noise gate stop high register. Thus, the writing sequence should be [noise gate stop low] [noise gate stop high].

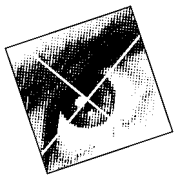
	Noise Gate Start/Stop High				Noise Gate Start/Stop Low							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H19	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

HCOUNT Register

This 12-bit register specifies the maximum number of pixel clocks to generate per horizontal line. In phase-locked applications, HCOUNT is the critical register that is resolution dependent. It should be programmed with the number of pixels per line required, minus 1. The other timing-dependent registers, including noise gate, ZERO, CLAMP, and HSYNC, will now all be programmed in terms of clock events, based upon the number of clocks per line defined in HCOUNT. For example, the HSYNC stop register is programmed to set output low at count zero, signifying the falling edge of HSYNC or the beginning of the line. The HSYNC start value is programmed to toggle high at 4.75 µs into the horizontal line, signifying the beginning of the back porch, for RS170A. The HSYNC start value in terms of a 12.27 MHz clock (square pixels NTSC) would be 59 clocks, or ~4.7 µs (see Figure 8).

The HCOUNT low and high registers are cascaded to form a 12-bit HCOUNT register. D4–D7 of HCOUNT high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 12-bit HCOUNT register is not updated until the write cycle to the HCOUNT high register. Thus, the writing sequence should be [HCOUNT low] [HCOUNT high]. Values from $0000 (1) to $0FFF (4096) may be specified. This register should be written first during initialization to minimize indeterminate output activity.

	HCOUNT High				**HCOUNT Low**							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H19	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0



APPLICATION INFORMATION

Phase Locking With the 74HC4046

Applications that call for multiple resolutions with clock rates in the 9–18 MHz range may employ the circuit (Figure 10) shown with a 74HC4046 and a passive loop filter. Residual jitter can be less than 30 ns, which is subpixel but not as good as can be achieved with LC-tuned VCOs or VCXOs. These have narrower tuning ranges. The loop parameters were obtained from a design program provided for the 74HC4046 with the Bt261's phase comparator emulating the type 2 phase detector with 4π/VCC gain (Note 1). The type 1 second-order loop is designed for 10 dB ripple suppression in closed-loop response with a critically damped response and a tracking range of 4 percent, which is adequate for most stable sources (e.g., broadcast, camera, and videodisc). Nonstandard video sources (e.g., heterodyne VCRs or floppy disk ESP cameras) may require a prefilter PLL for adequate tracking. Third-order loop filters may yield faster loop response rolloff, which reduces jitter but can prolong loop settling time.

The same circuit can be extended to 26 MHz for genlocking to higher raster frequency sources (such as noninterlaced VGA) or adapted to crystal-based operation up to 10 MHz. The VCO timing-capacitor value must be reduced to 40 pF for the former higher frequency case or replaced with a parallel resonant crystal in the latter case. Loop filter values will vary slightly in conjunction with modification of R1 and R2 VCO gain-setting resistors.

In general, VCO capture range must be limited to one octave to prevent harmonic lockup. With the low-input bias current of the 74HC4046, passive filters are simpler than active filters and can better accommodate large-value polarized capacitors. Bipolar VC(X)O implementations that use the MC4024, 74LS624, or MN3106 require active buffers with bias currents less than 10 µA to limit control voltage droop across the 64 µs interval between phase-comparison pulses. Low-absorption Mylar or Teflon capacitors in the loop filter can minimize jitter caused by capacitance modulation.

Figure 10. Operation of the Bt261 with the 74HC4046A

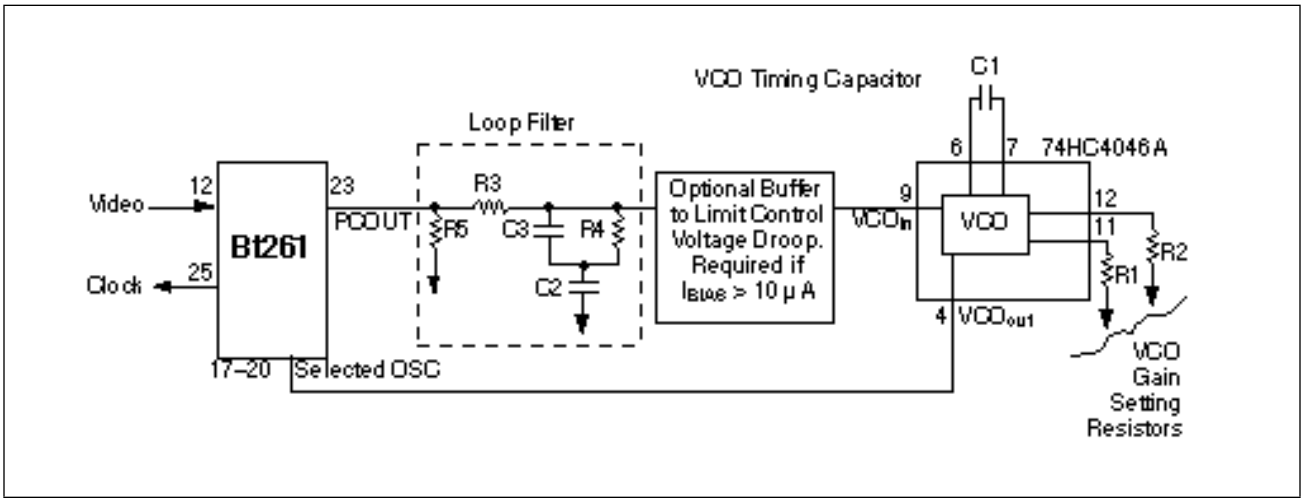


Table 4. Operation on the Bt261 with the 74HC4046A

Tracking Range	Oscillator Jitter	R_1	R_2	R_3	R_4	R_5	C_1	C_2	C_3	W_n	Damping (3)
9–18 MHz	<40 ns	3.9 kΩ	10 kΩ	470 Ω	86 Ω	500 kΩ	100 pF	10 µF	1 µF	290 Hz	0.74
17–26 MHz	<40 ns	3.9 kΩ	10 kΩ	470 Ω	86 Ω	500 kΩ	40 pF	10 µF	1 µF	290 Hz	0.74
±200 ppm of crystal center frequency	<10 ns	46 kΩ	46 kΩ	470 Ω	290 Ω	500 kΩ	≤10 MHz Resonant Crystal	3.3 nF	300 pF	290 Hz	0.74

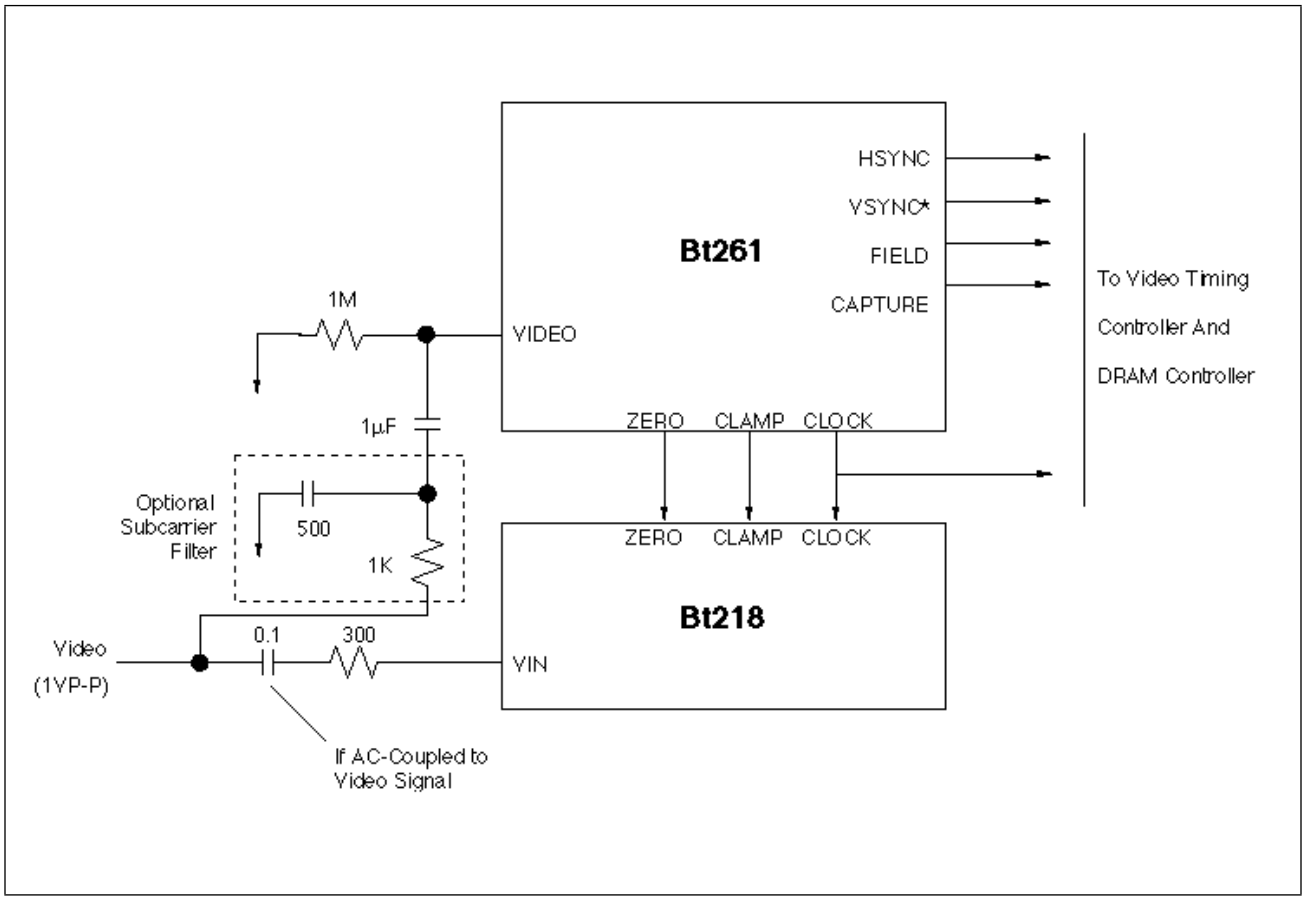
Interfacing to the Bt218

Figure 11 illustrates the interface of the Bt261 to the Bt218 Flash A/D Converter. The VIDEO input of the Bt261 connects to the VIN input of the Bt218 through a 1 µF ceramic capacitor. The sync slicing level of the Bt261 should be selected for optimum performance.

The Bt261 provides the ZERO and CLAMP signals required by the Bt218, in addition to the CLOCK.

The HSYNC, VSYNC*, FIELD, and CAPTURE signals of the Bt261 interface to the video timing controller and video DRAM controller.

Figure 11. Interfacing the Bt218



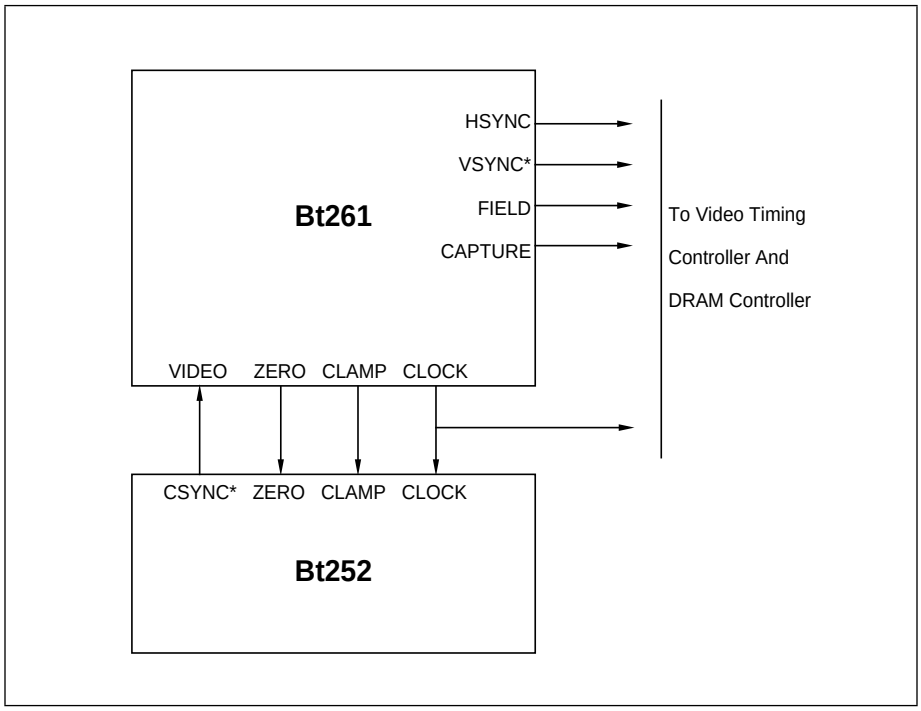
Interfacing to the Bt252

Figure 12 illustrates the interface of the Bt261 to the Bt252 Image Digitizer. The VIDEO input of the Bt261 connects directly to the CSYNC* output of the Bt252. As CSYNC* is a TTL-compatible output, the highest sync slicing level should be selected on the Bt261.

The Bt261 provides the ZERO and CLAMP signals required by the Bt252, in addition to the CLOCK.

The HSYNC, VSYNC*, FIELD, and CAPTURE signals of the Bt261 interface to the video timing controller and video DRAM controller.

Figure 12. Interfacing to the Bt252

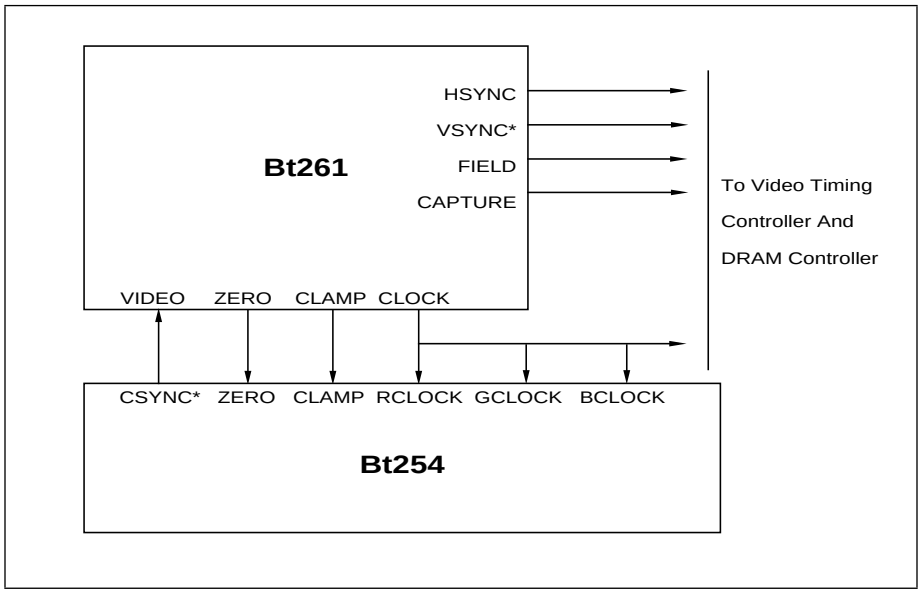


Interfacing to the Bt254

Figure 13 illustrates the interface of the Bt261 to the Bt254 Image Digitizer. The VIDEO input of the Bt261 connects directly to the CSYNC* output of the Bt254. As CSYNC* is a TTL-compatible output, the highest sync slicing level should be selected on the Bt261.

The Bt261 provides the ZERO and CLAMP signals required by the Bt254, in addition to the (R,G,B) CLOCK inputs of the Bt254.
The HSYNC, VSYNC*, FIELD, and CAPTURE signals of the Bt261 interface to the video timing controller and video DRAM controller.

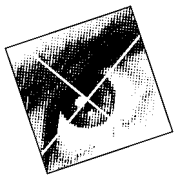
Figure 13. Interfacing to the Bt254



ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

Latchup can be prevented by ensuring that all VCC pins are at the same potential and that the VCC supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.



PARAMETRIC INFORMATION

DC Electrical Parameters

Table 5. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Ambient Operating Temperature	VCC TA	4.75 0	5.00	5.25 +70	V °C
Video Input DC-coupled AC-coupled (1)		0.2		5 2	V V_{pp}

Table 6. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (measured to GND)				7.0	V
Voltage on any Signal Pin (1)		GND–0.5		VCC + 0.5	V
Ambient Operating Temperature		–55			
Storage Temperature	TA	–65		+ 125	°C
Junction Temperature	TS			+ 150	°C
	TJ			+ 150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Notes: (1). Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. This device employs high impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

Table 7. DC Characteristics *(1 of 2)*

Parameter	Symbol	Min	Typ	Max	Units
TTL Digital Inputs				VCC + 0.5	V
Input High Voltage	VIH	2.0		VCC + 0.5	V
Input High Voltage (1)	VIH	2.2			
HSYNC Pin				0.8	V
Input Low Voltage	VIL	GND–0.5		0.4	V
Input Low Voltage (1)	VIL				
RD* Pin				1	µA
Input High Current (Vin = 2.4 V)	IIH			–1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1.5	mA
Input Low Current (Vin = 0.4 V)	IIL				
VIDEO Pin					pF
Input Capacitance	CIN		7		
(f = 1 MHz, Vin = 2.4 V)					
OSC Digital Inputs				VCC + 0.5	V
TTL Mode		2.2		0.8	V
Input High Voltage (1)	VIH	GND–0.5		1	µA
Input Low Voltage	VIL			–1	µA
Input High Current (Vin = 2.4 V)	IIH				pF
Input Low Current (Vin = 0.4 V)	IIL				
Input Capacitance	CIN				
(f = 1 MHz, Vin = 2.4 V)			7	VCC + 0.5	V
ECL Mode		VCC–1.0		VCC–1.6	V
Input High Voltage	VIH	GND–0.5		1	µA
Input Low Voltage	VIL			–1	µA
Input High Current (Vin = 4.0 V)	IIH				pF
Input Low Current (Vin = 0.4 V)	IIL				
Input Capacitance	CIN		7		
(f = 1 MHz, Vin = 2.4 V)					

Table 7. DC Characteristics *(2 of 2)*

Parameter	Symbol	Min	Typ	Max	Units
D0?–D7 Digital Outputs				0.4	V
Output High Voltage (IOH = –400 µA)	VOH	2.4			
Output Low Voltage (IOL = 6.4 mA)				0.5	V
3-state Current	VOL				
Output Capacitance					µA
	IOZ				pF
	COUT		20		
PCOUT Output				0.4	V
Output High Voltage (IOH = –400 µA)	VOH	2.4			
Output Low Voltage (IOL = 3.2 mA)				400	V
3-state Current	VOL				
Output Capacitance					µA
	IOZ				pF
	COUT		20		
Other Digital Outputs				0.4	V
Output High Voltage (IOH = –400 µA)	VOH	2.4			
Output Low Voltage (IOL = 3.2 mA)				0.5	V
3-State Current	VOL				
Output Capacitance					µA
	IOZ				pF
	COUT		20		

Notes: (1). VIH, VIL for RD*, HSYNC, and OSC inputs are tested at 3 and 0 V but guaranteed by characterization.
2. Test conditions (unless otherwise specified):"Recommended Operating Conditions." Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

AC Electrical Parameters

Table 8. AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
OSC Cycle Time	OSCmax				ns
TTL mode		13.3			ns
ECL mode		12.5			ns
CLOCK Cycle Time (1)	Fmax	33.33			ns
A0 Setup Time	1	10			ns
A0 Hold Time	2	10			ns
RD*/WR* Low Time	3	40			ns
RD*/WR* High Time	4	40			ns
RD* Asserted to Data Bus Driven	5	1			ns
RD* Asserted to Data Valid	6			30	ns
RD* Negated to Data Bus 3-Stated	7			30	ns
Write Data Setup Time	8	10			ns
Write Data Hold Time	9	10			ns
OSC High Time	10	6			ns
OSC Low Time	11	6			ns
OSC to CLOCK Output Delay	14			35	ns
VIDEO to CSYNC* Output Delay	15			35	ns
HSYNC, ZERO, CLAMP Output Delay	16			10	ns
VSYNC*, FIELD Output Delay	17			10	ns
PCOUT Output Delay	18	380	5	650	ns
Minimum Compare Differential	19			13	ns
VCC Supply Current (2)	ICC		60	90	ns

Notes: (1). Maximum load of 20 pf.
(2). At Fmax. ICC (typ) at VCC = 5.0 V. ICC (max) at VCC = 5.25 V. OSC/PCLOCK = 2, CLOCK/HSYNC ≥100.
3. Test conditions (unless otherwise specified):"Recommended Operating Conditions." TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. CLOCK, HSYNC, CLAMP, ZERO, VSYNC*, FIELD, CAPTURE, and CSYNC* output load ≤ 50 pF, D0–D7 output load ≤ 130 pF. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Timing Waveforms

Figure 13. MPU Read/Write Timing

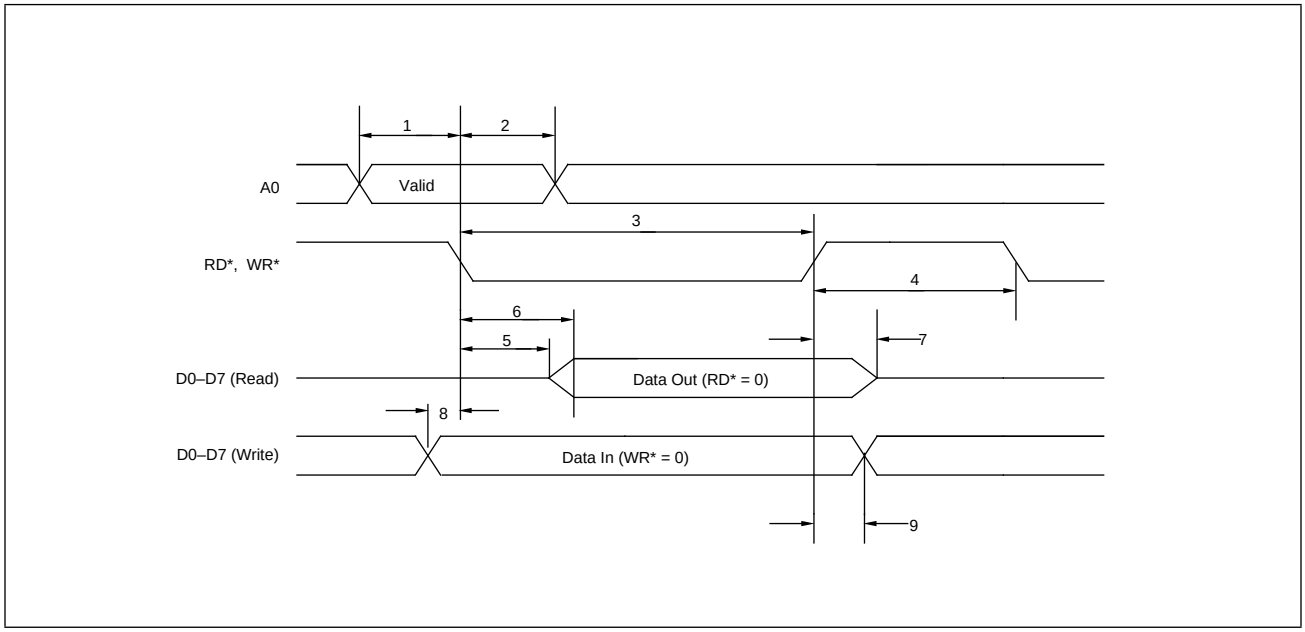


Figure 14. Video/Output Timing

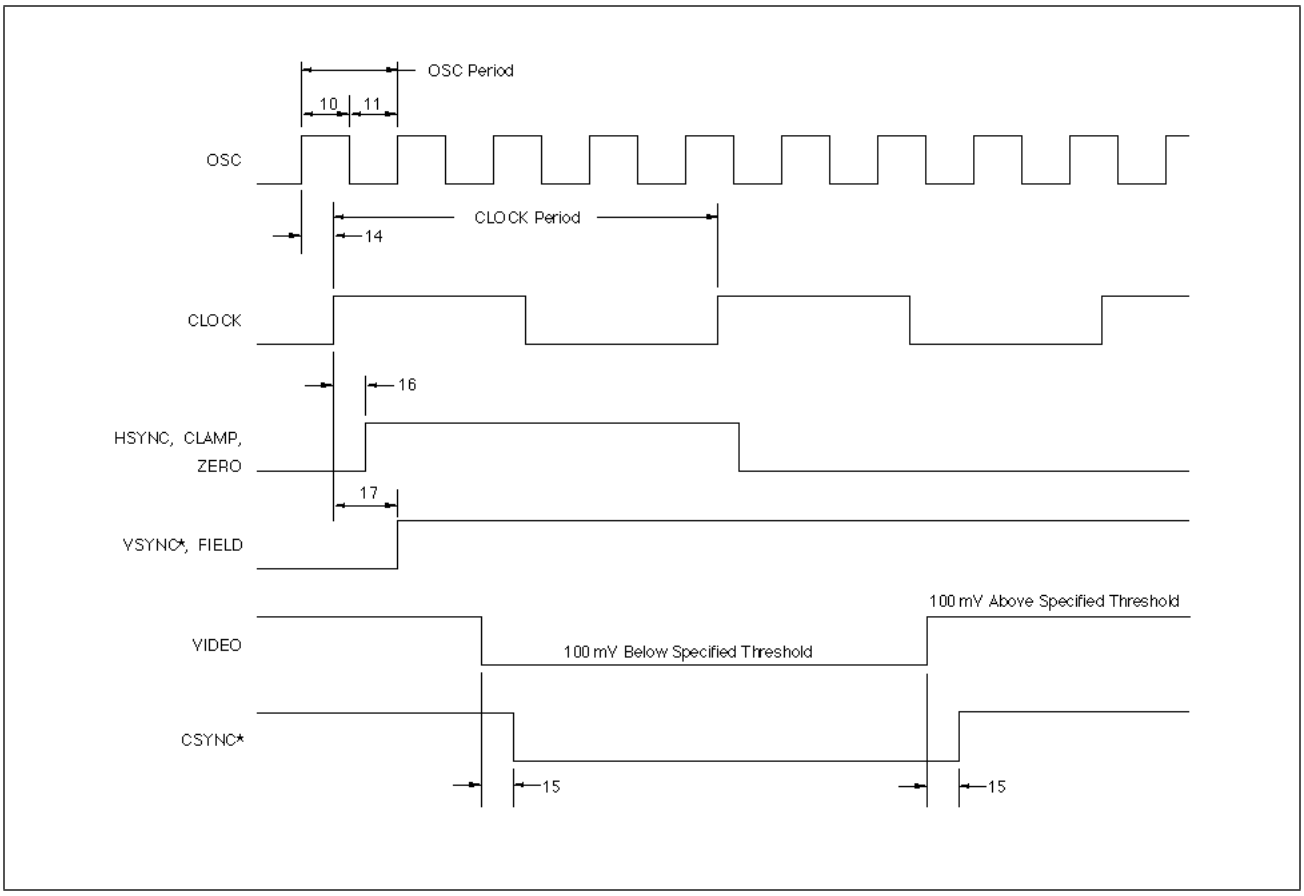


Figure 15. Video Input/Output Timing

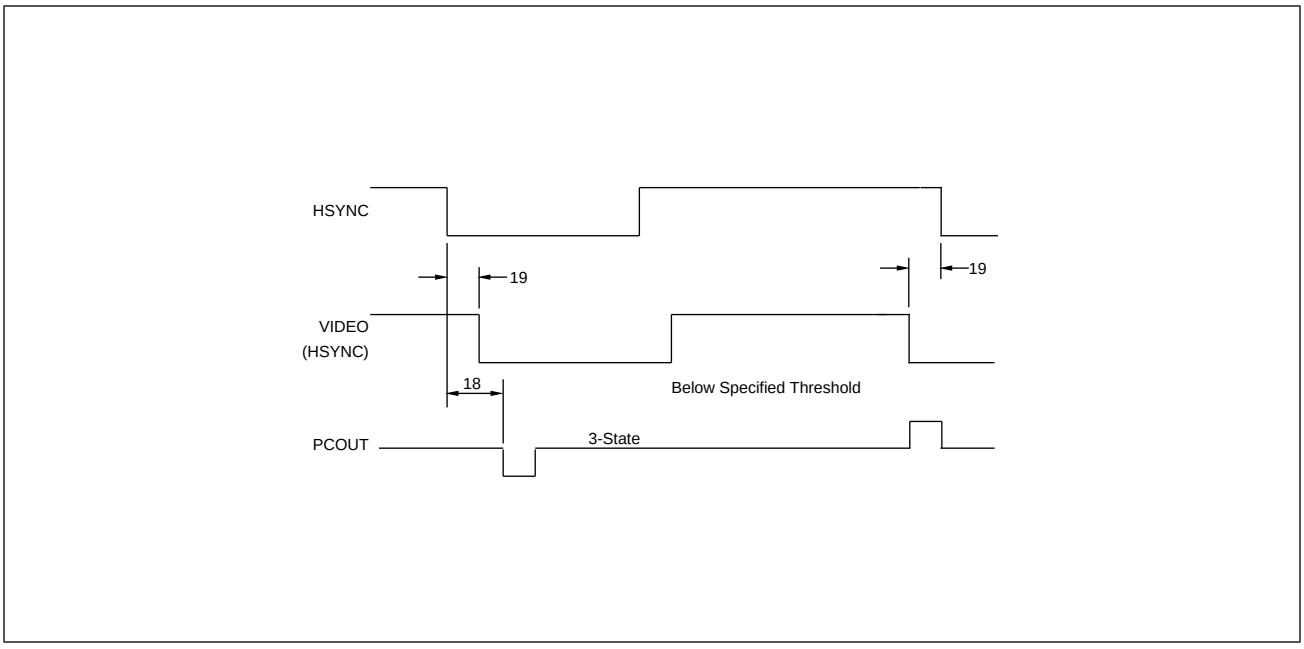
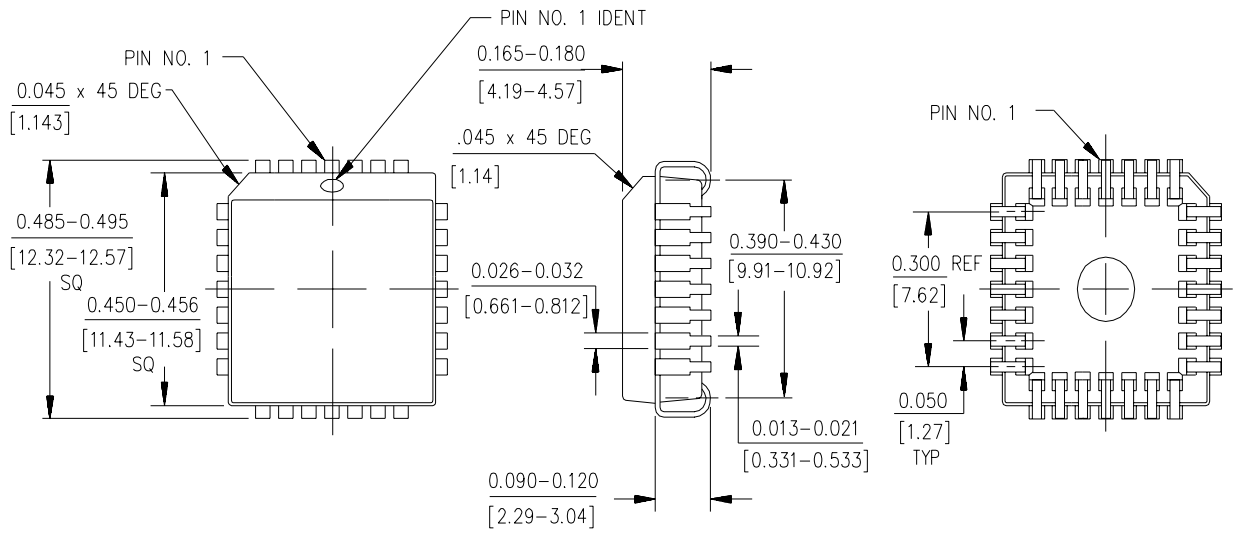


Figure 16. Package Drawing—28–pin Plastic J-Lead (PLCC)



Unless otherwise specified:

Notes: 1. Dimensions are in inches [millimeters].
2. Tolerances are: .xxx ± 0.005 [0.127].
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

Revision History

Table 9. Bt261 Datasheet Revision History

Revision	Date	Description
G, H	09-16-93	In Table 1, HCOUNT start low/high register changed to HCOUNT low/high register. In the Internal Register Section, HCOUNT register changed from 16-bit to 12-bit. The Application Information Section was revised; 0.1 µF ceramic capacitor changed to 1 µF (this change applies to Figure 10 as well). Figures 1, 4, 5, 8 and 10 were revised.

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