Thyristors logic level

BT149 series

GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

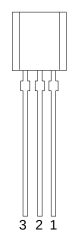
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	MAX.	UNIT
	BT149	B	D	E	G	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages	200	400	500	600	V
$I_{T(AV)}$	Average on-state current	0.5	0.5	0.5	0.5	A
$I_{T(RMS)}$	RMS on-state current	0.8	0.8	0.8	0.8	A
I_{TSM}	Non-repetitive peak on-state current	8	8	8	8	A

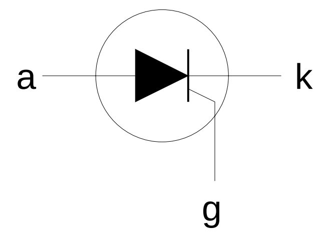
PINNING - TO92 variant

PIN	DESCRIPTION
1	cathode
2	gate
3	anode

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.				UNIT
				B	D	E	G	
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages		-	200[1]	400[1]	500[1]	600[1]	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{lead} \leq 83$ ˚C	-	0.5				A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	0.8				A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; $T_j = 25$ ˚C prior to surge; t = 10 ms	-	8				A
		t = 8.3 ms	-	9				A
I^2t	I^2t for fusing	t = 10 ms	-	0.32				A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 2$ A; $I_G = 10$ mA; $dI_G/dt = 100$ mA/µs	-	50				A/µs
I_{GM}	Peak gate current		-	1				A
V_{GM}	Peak gate voltage		-	5				V
V_{RGM}	Peak reverse gate voltage		-	5				V
P_{GM}	Peak gate power		-	2				W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.1				W
T_{stg}	Storage temperature		-40	150				˚C
T_j	Operating junction temperature		-	125				˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}lead}$	Thermal resistance junction to lead		-	-	60	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	pcb mounted; lead length = 4mm	-	150	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 10 mA; gate open circuit	-	50	200	µA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.5 mA; R_{GK} = 1 kΩ	-	2	6	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.5 mA; R_{GK} = 1 kΩ	-	2	5	mA
V_T	On-state voltage	I_T = 1 A	-	1.2	1.35	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 10 mA; gate open circuit	-	0.5	0.8	V
		V_D = $V_{DRM(max)}$; I_T = 10 mA; T_j = 125 ˚C; gate open circuit	0.2	0.3	-	V
I_D, I_R	Off-state leakage current	V_D = $V_{DRM(max)}$; V_R = $V_{RRM(max)}$; T_j = 125 ˚C; R_{GK} = 1 kΩ	-	0.05	0.1	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; R_{GK} = 1 kΩ	-	25	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 2 A; V_D = $V_{DRM(max)}$; I_G = 10 mA; dI_G/dt = 0.1 A/µs	-	2	-	µs
t_q	Circuit commutated turn-off time	V_D = 67% $V_{DRM(max)}$; T_j = 125 ˚C; I_{TM} = 1.6 A; V_R = 35 V; dI_{TM}/dt = 30 A/µs; dV_D/dt = 2 V/µs; R_{GK} = 1 kΩ	-	100	-	µs

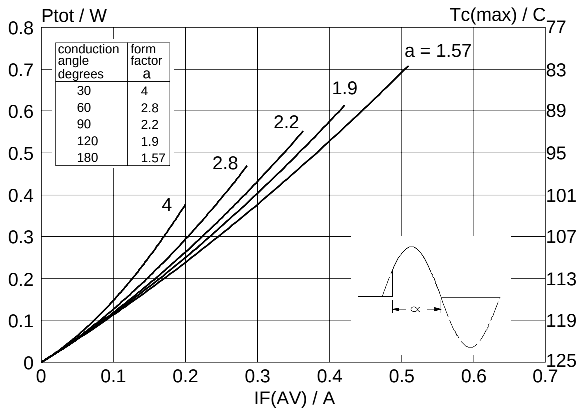


Fig.1. Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}$/ $I_{T(AV)}$.

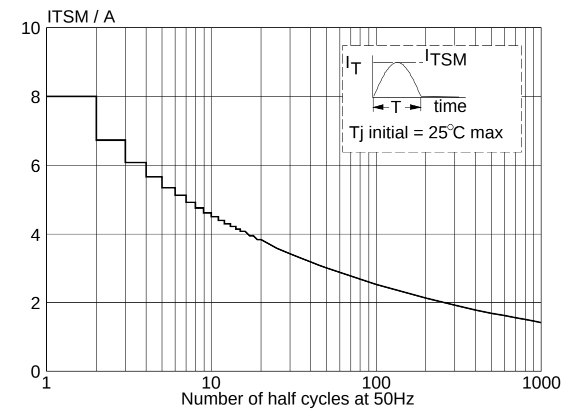


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

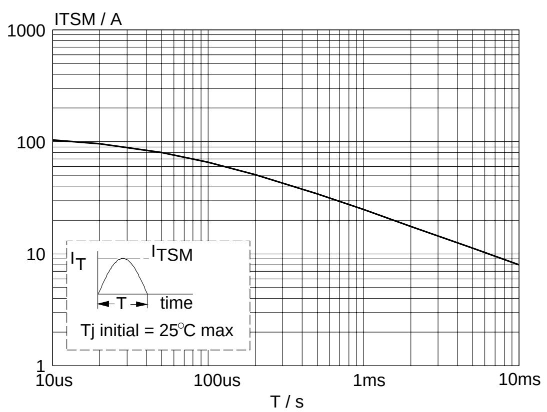


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq$ 10ms.

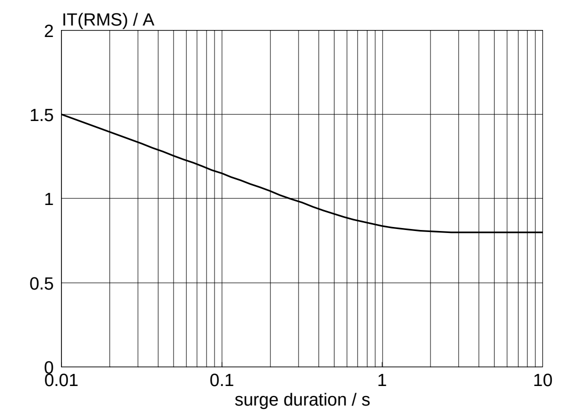


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{lead} \leq 83^{\circ}C$.

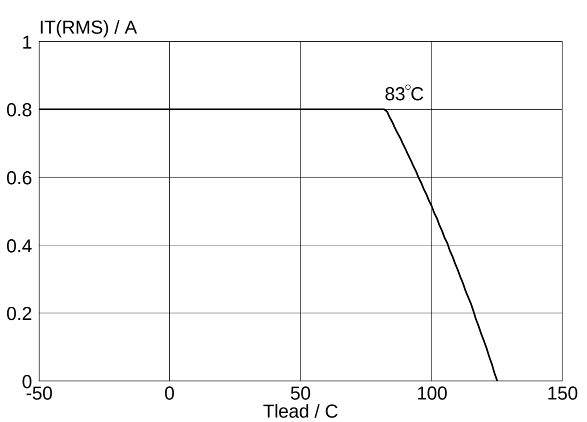


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus lead temperature, T_{lead}.

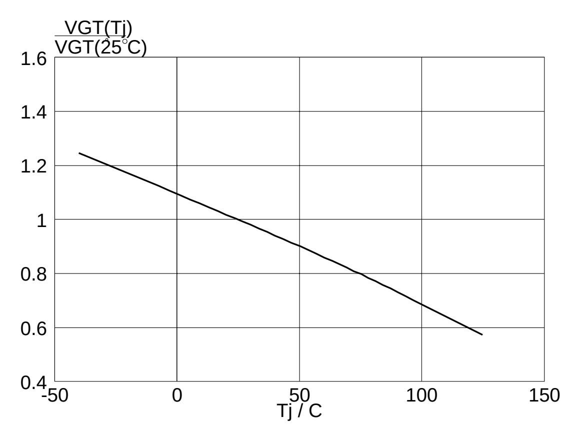


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ $V_{GT}(25^{\circ}C)$, versus junction temperature T_j.

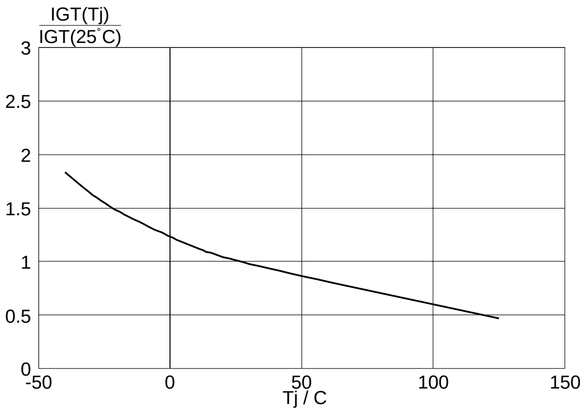


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25^\circ C)$, versus junction temperature T_j.

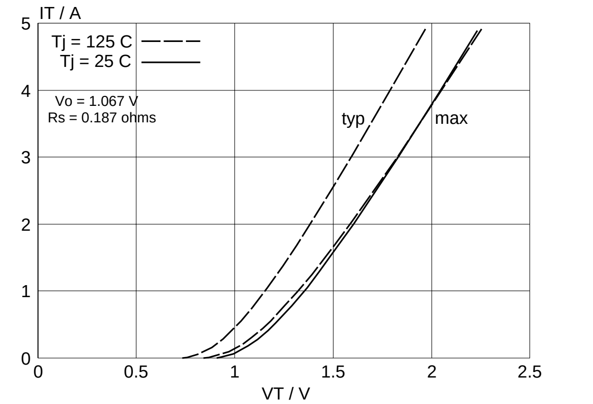


Fig.10. Typical and maximum on-state characteristic.

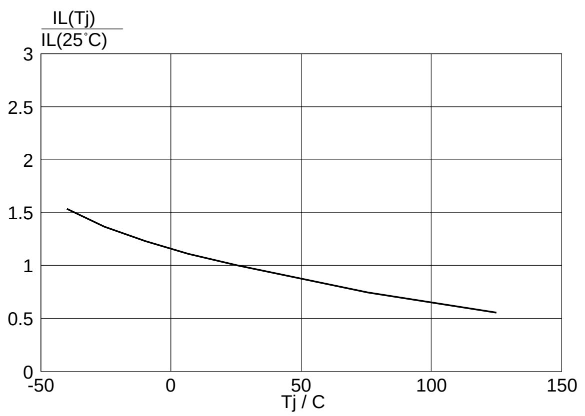


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25^\circ C)$, versus junction temperature T_j, R_{GK} = 1 kΩ.

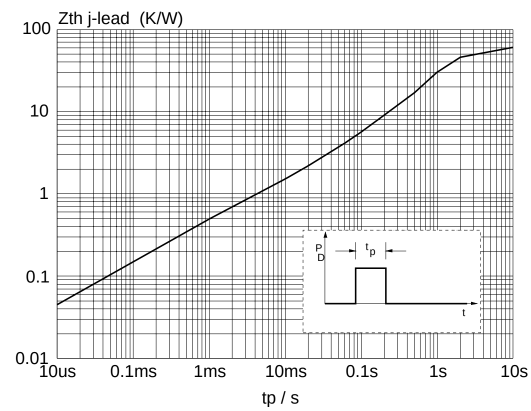


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}lead}$, versus pulse width t_p.

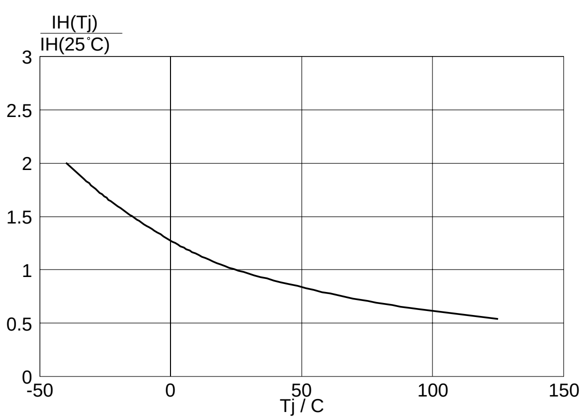


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25^\circ C)$, versus junction temperature T_j, R_{GK} = 1 kΩ.

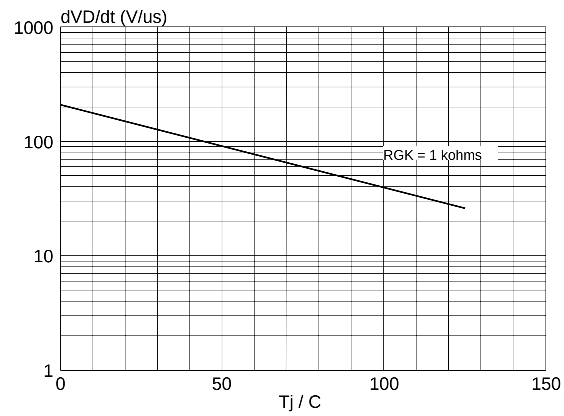


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

MECHANICAL DATA

Dimensions in mm

Net Mass: 0.2 g

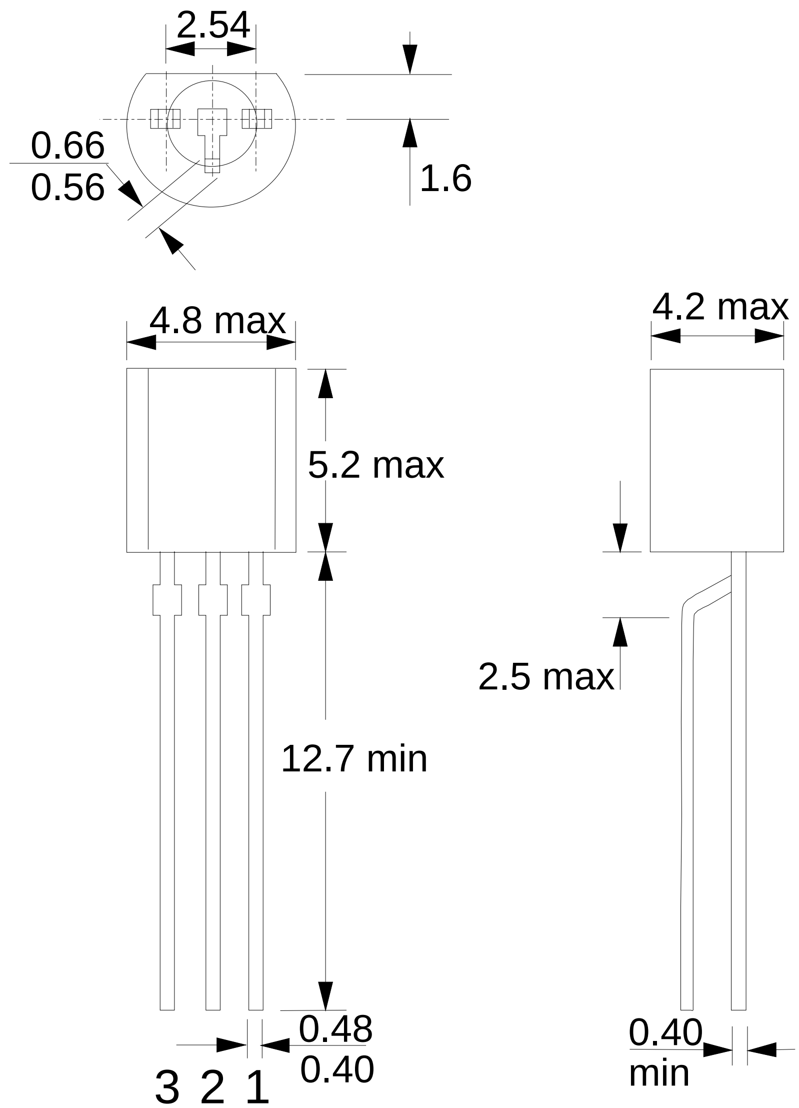


Fig.13. TO92; plastic envelope.

Notes

1. Epoxy meets UL94 V0 at 1/8".

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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