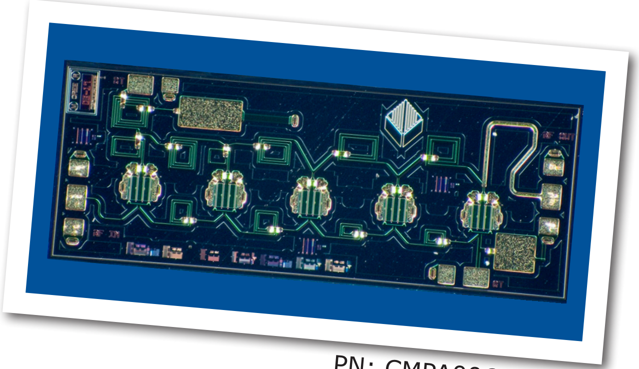
PRELIMINARY

CMPA0060002D

2 Watt, 20 MHz - 6000 MHz GaN HEMT MMIC Power Amplifier

Cree's CMPA0060002D is a gallium nitride (GaN) High Electron Mobility Transistor (HEMT) based monolithic microwave integrated circuit (MMIC). GaN has superior properties compared to silicon or gallium arsenide, including higher breakdown voltage, higher saturated electron drift velocity and higher thermal conductivity. GaN HEMTs also offer greater power density and wider bandwidths compared to Si and GaAs transistors. This MMIC employs a distributed (traveling-wave) amplifier design approach, enabling extremely wide bandwidths to be achieved in a small footprint.



PN: CMPA0060002D

Typical Performance Over 0.5-6.0 GHz (T_C = 25˚C)

Parameter	0.5 GHz	1.0 GHz	2.5 GHz	4.0 GHz	6.0 GHz	Units
Gain	18.7	17.4	17.6	17.4	17.6	dB
Saturated Output Power @ P_{IN} 23 dBm	7.0	6.3	5.7	4.3	3.6	W
Power Gain @ P_{IN} 23 dBm	15.4	15.0	14.5	13.3	12.5	dB
PAE @ P_{IN} 23 dBm	43	40	36	28	31	%

Note: V_{DD} = 28 V, I_D = 100 mA

Features

- 17 dB Small Signal Gain
- 2 W Typical P_{SAT}
- Operation up to 28 V
- High Breakdown Voltage
- High Temperature Operation
- Size 0.169 x 0.066 x 0.004 inches

Applications

- Ultra Broadband Amplifiers
- Fiber Drivers
- Test Instrumentation
- EMC Amplifier Drivers

Rev 0.5 – June 2010

Absolute Maximum Ratings (not simultaneous) at 25˚C

Parameter	Symbol	Rating	Units
Drain-source Voltage	V_{DSS}	84	VDC
Gate-source Voltage	V_{GS}	-10, +2	VDC
Storage Temperature	T_{STG}	-65, +150	˚C
Operating Junction Temperature	T_J	225	˚C
Maximum Forward Gate Current	I_{GMAX}	2	mA
Thermal Resistance, Junction to Case (packaged)[1]	$R_{\theta JC}$	4.0	˚C/W

Note[1] Eutectic die attach using 80/20 AuSn mounted to a 40 mil thick CuW carrier.

Electrical Characteristics (Frequency = 20 MHz to 6,000 MHz unless otherwise stated; T_C = 25˚C)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics						
Gate Threshold Voltage[1]	V_{TH}	-3.8	-3.3	-2.7	V	V_{DS} = 20 V, ΔI_D = 2 mA
Saturated Drain Current[2]	I_{DS}	–	1.94	–	A	V_{DS} = 6.0 V, V_{GS} = 2.0 V
RF Characteristics[5]						
Small Signal Gain[3]	S21	13.5	18	–	dB	V_{DD} = 26 V, I_{DQ} = 100 mA
Input Return Loss	S11	–	9	–	dB	V_{DD} = 26 V, I_{DQ} = 100 mA
Output Return Loss	S22	–	11	–	dB	V_{DD} = 26 V, I_{DQ} = 100 mA
Output Power[4]	P_{OUT}	2	4	–	W	V_{DD} = 26 V, I_{DQ} = 100 mA, P_{IN} = 23 dBm
Power Added Efficiency	PAE	–	30	–	%	V_{DD} = 26 V, I_{DQ} = 100 mA, P_{IN} = 23 dBm
Power Gain	G_P	–	13.0	–	dB	V_{DD} = 26 V, I_{DQ} = 100 mA, P_{IN} = 23 dBm
Output Mismatch Stress	VSWR	–	–	5 : 1	Ψ	No damage at all phase angles, V_{DD} = 26 V, I_{DQ} = 100 mA, P_{IN} = 23 dBm

Notes:

[1] The device will draw approximately 20-25 mA at pinch off due to the internal circuit structure.

[2] Scaled from PCM data.

[3] The lowest test frequency is 1.0 GHz due to the lack of a low frequency termination.

[4] Test frequencies 1.0, 2.5, and 4.0 GHz.

[5] All data pulsed with Pulse Width = 10 μsec, Duty Cycle = 0.1%.

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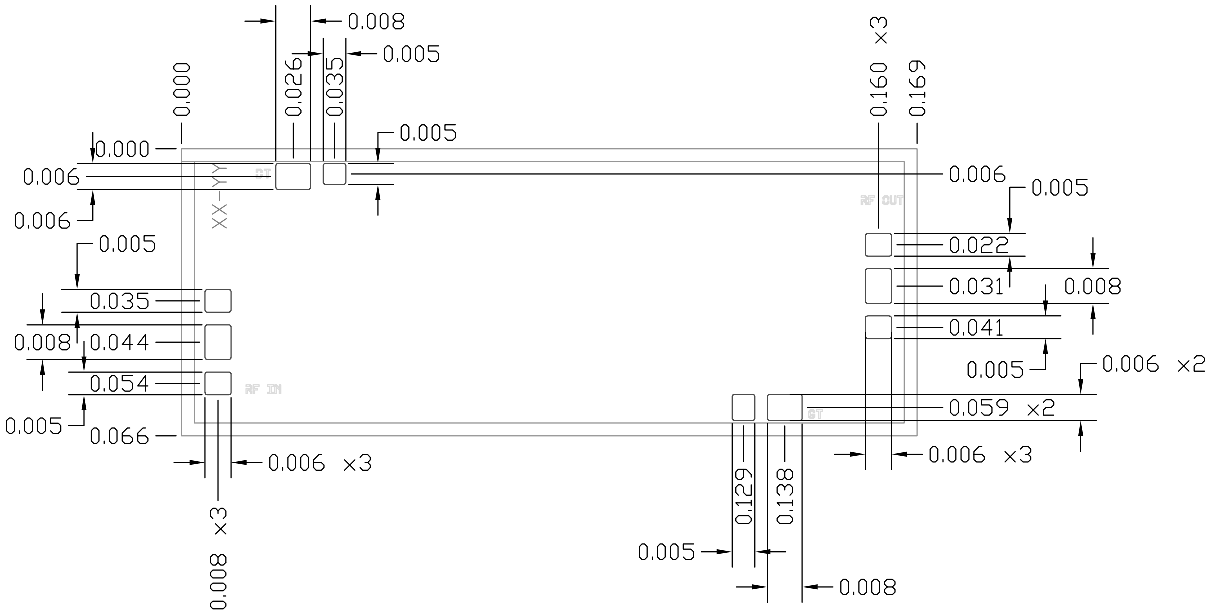
Die Dimensions (units in inches)



Overall die size 0.169 x 0.066 (+0/-0.005) inches, die thickness 0.004 inches.
All Gate and Drain pads must be wire bonded for electrical connection.

Pad Number	Function	Description	Pad Size (in)
1	RF IN[1]	RF-Input pad. Matched to 50 ohm. Requires gate control from an external bias –T from -2.3 V to -3.8 V.	0.008” x 0.006”
2	Gate Termination	Off Chip termination for the Gate. It needs to be DC-blocked .	0.008” x 0.006”
3	Drain Termination	Off Chip termination for the Drain. It needs to be DC-blocked.	0.008” x 0.006”
4	RF OUT[1]	RF-Output pad. Matched to 50 ohm. Requires Drain supply from an external bias –T up to 26 V , 800 mA	0.008” x 0.006”

Notes:
[1] The RF In and Out pads have a ground-signal-ground configuration with a pitch of 0.010 inches.

Die Assembly Notes:

- Recommended solder is AuSn (80/20) solder. Refer to Cree’s website for the Eutectic Die Bond Procedure application note at www.cree.com/wireless.
- Vacuum collet is the preferred method of pick-up.
- The backside of the die is the Source (ground) contact.
- Die back side gold plating is 5 microns thick minimum.
- Thermosonic ball or wedge bonding are the preferred connection methods.
- Gold wire must be used for connections.
- Use the die label (XX-YY) for correct orientation.

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Functional Block Diagram

This device employs a wideband, traveling wave amplifier topology. It has an internal termination for both the Drain and the Gate, which works well over 2.5-6.0 GHz. For operation below 2.5 GHz an external termination is required. This termination needs to be DC-blocked and suitable to withstand up to 3 W of RF power. (Refer to the reference design section for the LF-termination in this data sheet for more details). The circuits also require external wideband Bias –T's to supply voltage to the Gate and Drain. The Bias-T at the Drain needs to be designed to handle 28 V and up to 800 mA.

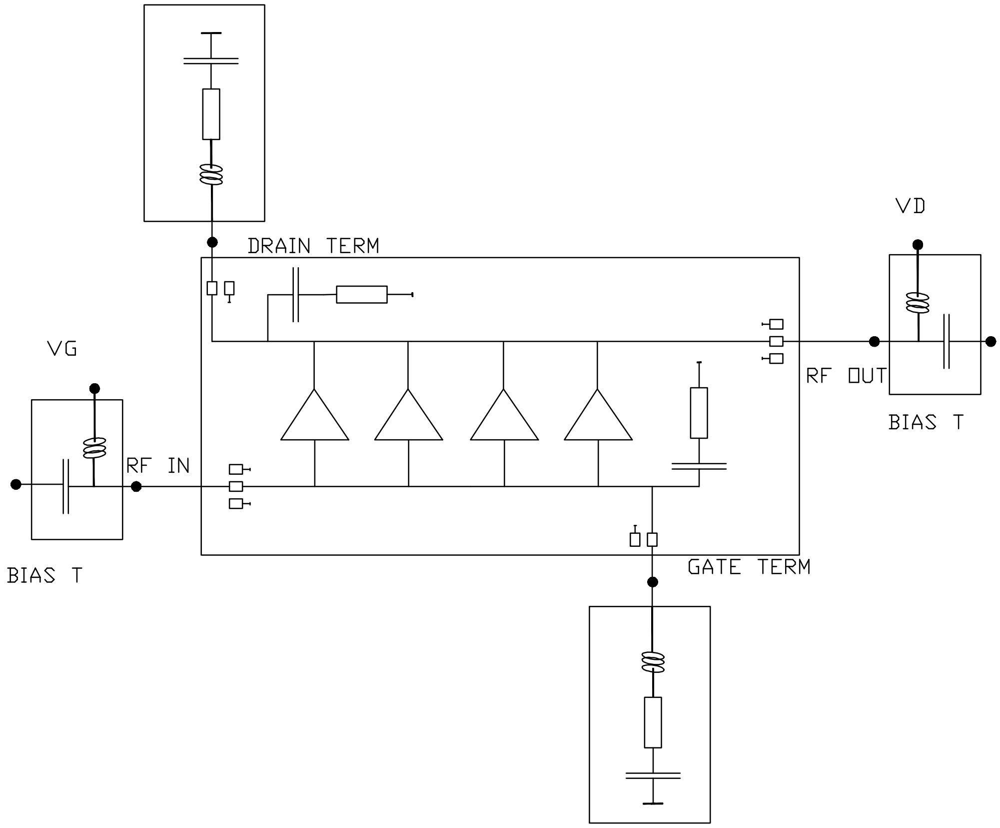

Figure 1.

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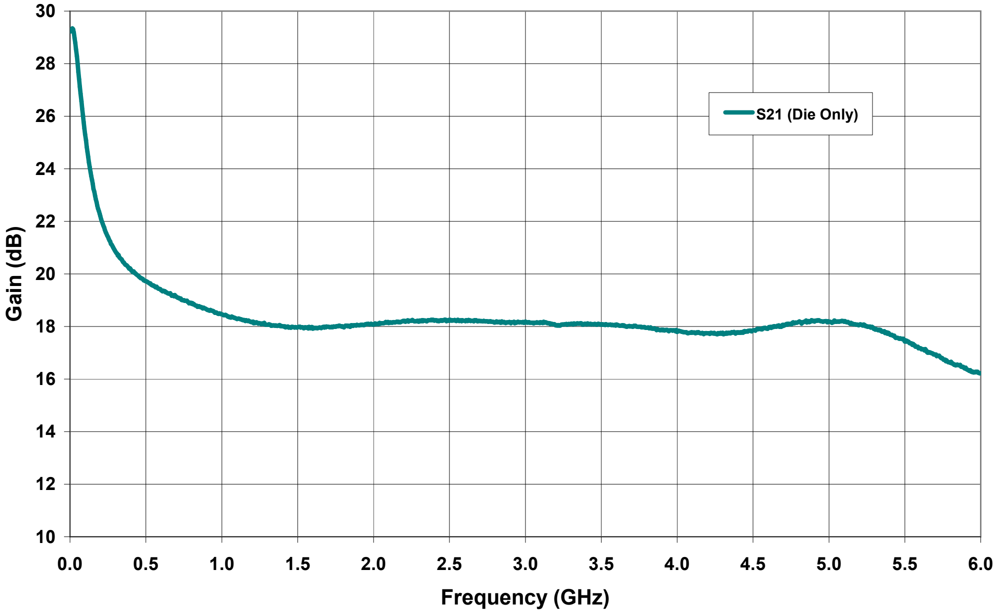
External Termination Reference Design

The following is a plot of the gain of the die only.



Notes:

[1] An off chip termination is needed to reduce the high gain peak at low frequencies.

[2] The off chip termination should be designed to minimize the impact on the MMIC's performance at higher frequencies.

LRC Reference Circuit

The Drain and Gate circuit use the same L and C components but different values for the resistor.

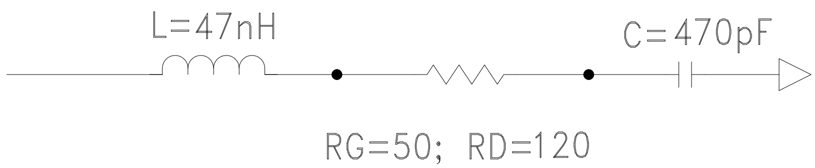


Figure 2.

The Drain resistor needs to be dimensioned to handle 3 W of RF dissipation for the lowest frequencies while the Gate resistor needs to handle 0.5 W. The suppliers of the SMT components are:

L1 = 47 nH, CoilCraft PN: 0402CS –47NXJB

C1 = 470 pf Murata PN: GRM1885C2A471A01D

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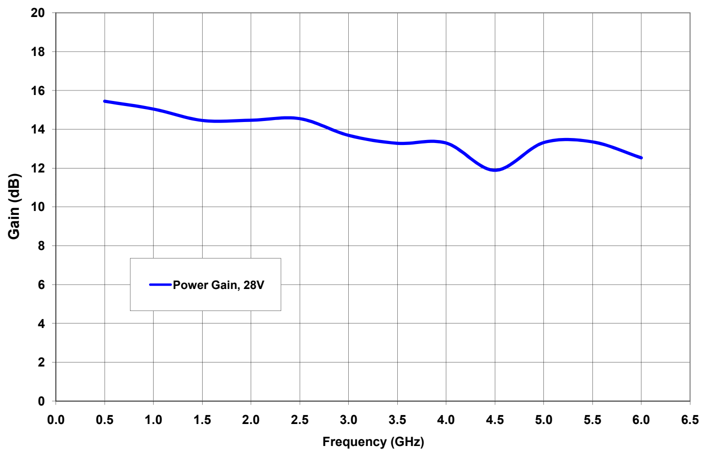
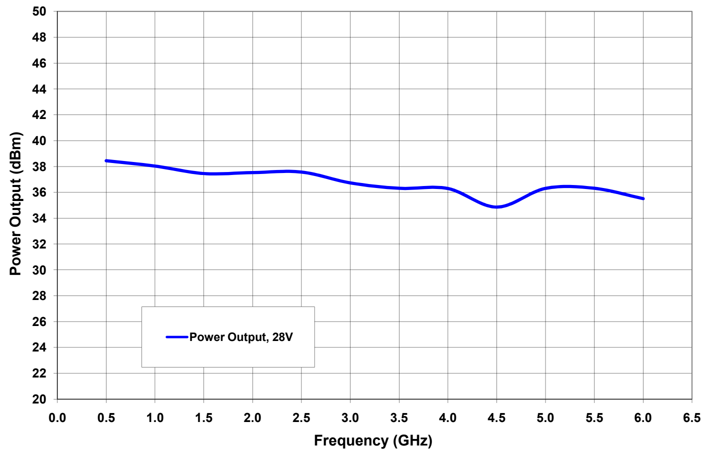
Typical Performance

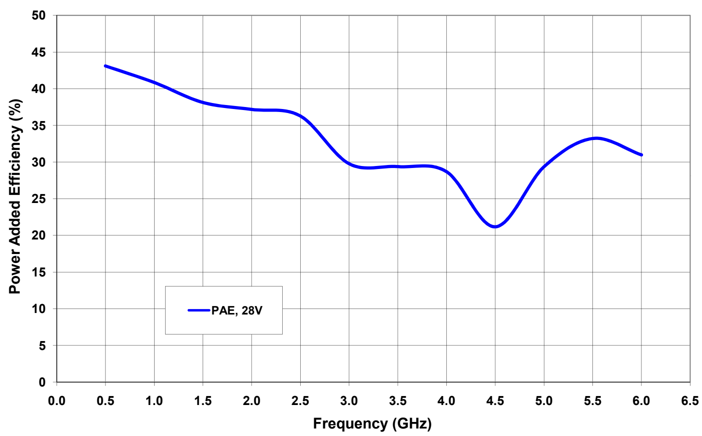
Power Gain vs Frequency
V_{DD} = 28 V, P_{IN} = 23 dBm



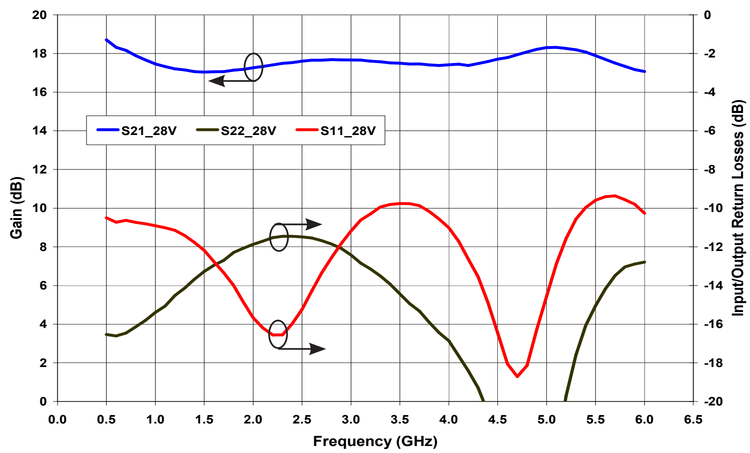
Power Output vs Frequency
V_{DD} = 28 V, P_{IN} = 23 dBm



Power Added Efficiency vs Frequency
V_{DD} = 28V, P_{IN} = 23 dBm



Gain and Return Losses vs Frequency
V_{DD} = 28 V, I_{DQ} = 100 mA



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