

P Channel Enhancement Mode MOSFET ST2305

-3.5A

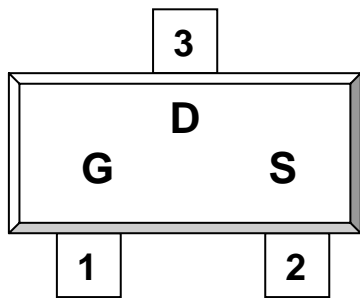
DESCRIPTION

The ST2305 is the P-Channel logic enhancement mode power field effect transistor are produced using high cell density, DMOS trench technology.

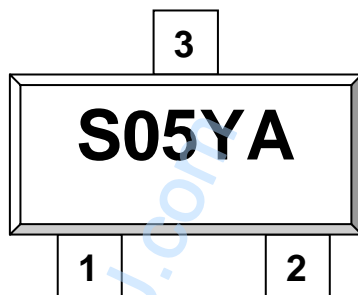
This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other batter powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION SOT-23-3L



1.Gate 2.Source 3.Drain



S: Subcontractor Y: Year Code A: Process Code

FEATURE

- -10V/-3.5A, $R_{DS(ON)} = 50\text{m-ohm}$
@VGS = -4.5V
- -10V/-3.0A, $R_{DS(ON)} = 70\text{m-ohm}$
@VGS = -2.5V
- -10V/-2.0A, $R_{DS(ON)} = 105\text{m-ohm}$
@VGS=-1.8V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3L package design



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ABSOLUTE MAXIMUM RATINGS (Ta = 25 Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	-10	V
Gate-Source Voltage	V _{GSS}	+/-12	V
Continuous Drain Current (T _J =150)	I _D	T _A =25	A
		T _A =70	-2.8
Pulsed Drain Current	I _{DM}	-10	A
Continuous Source Current (Diode Conduction)	I _S	-1.6	A
Power Dissipation	P _D	T _A =25	W
		T _A =70	0.8
Operation Junction Temperature	T _J	150	
Storage Temperature Range	T _{STG}	-55/150	
Thermal Resistance-Junction to Ambient	R _{JA}	120	/W


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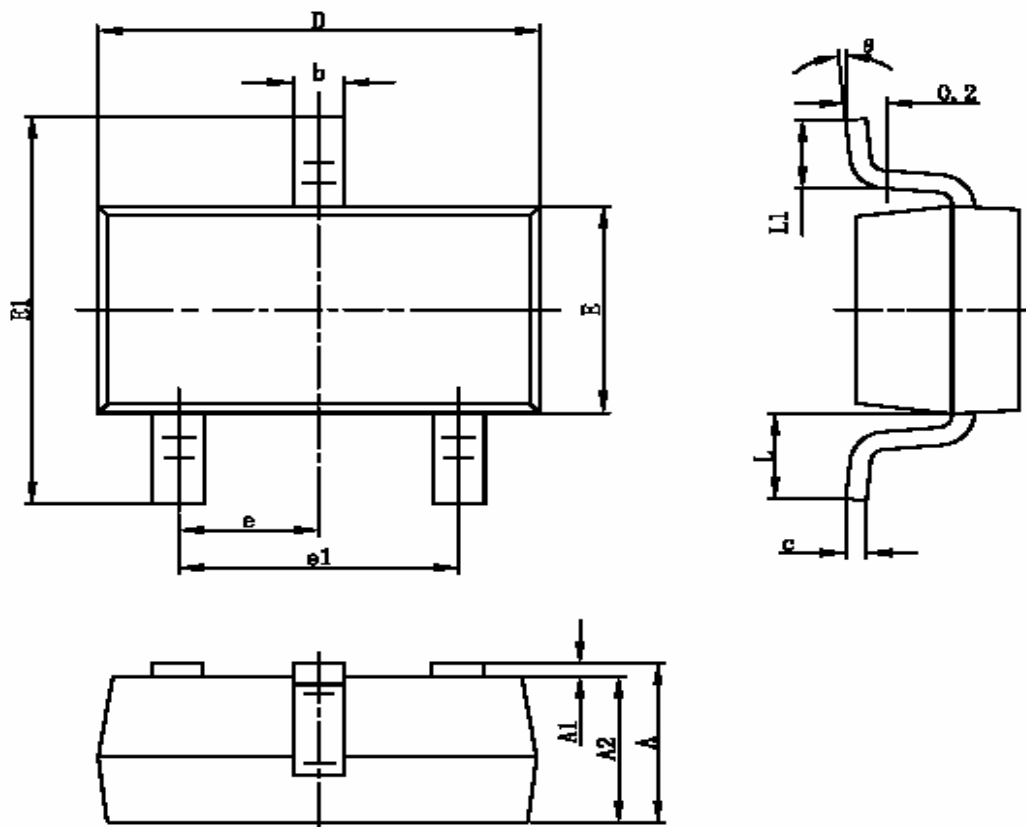
ELECTRICAL CHARACTERISTICS (Ta = 25 Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-10			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.45		-1.5	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=+/-12V$			100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-20V, V_{GS}=0V$			-1	uA
		$V_{DS}=-20V, V_{GS}=0V$ $T_J=55$			-10	
On-State Drain Current	$I_{D(on)}$	$V_{DS} = -5V, V_{GS}=-4.5V$ $V_{DS} = -5V, V_{GS}=-2.5V$	-6 -3			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-3.5A$ $V_{GS}=-2.5V, I_D=-2.0A$ $V_{GS}=-1.8V, I_D=-2.0A$		0.045 0.55 0.09	0.05 0.07 0.105	
Forward Transconductance	g_{fs}	$V_{DS}=-5V, I_D=-3.5V$		8.5		S
Diode Forward Voltage	V_{SD}	$I_S=-1.6A, V_{GS}=0V$		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-10V, V_{GS}=-4.5V$ $I_D = -3.5A$		10	12	nC
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			2		
Input Capacitance	C_{iss}	$V_{DS}=-10V, V_{GS}=0V$ $F=1MHz$		1200		pF
Output Capacitance	C_{oss}			300		
Reverse Transfer Capacitance	C_{rss}			210		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-10V, R_L=6$ $I_D=-1.0A, V_{GEN}=-4.5V$ $R_G=6$		13	25	nS
	t_r			20	35	
Turn-Off Time	$t_{d(off)}$			42	70	
	t_f			20	35	



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SOT-23-3L PACKAGE OUTLINE


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
theta	0°	8°	0°	8°

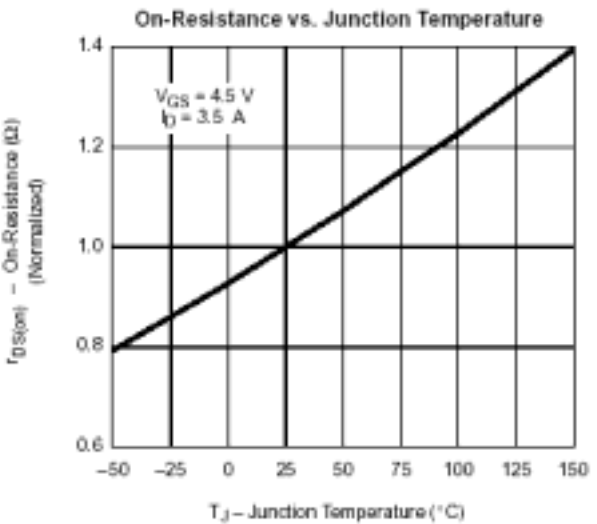
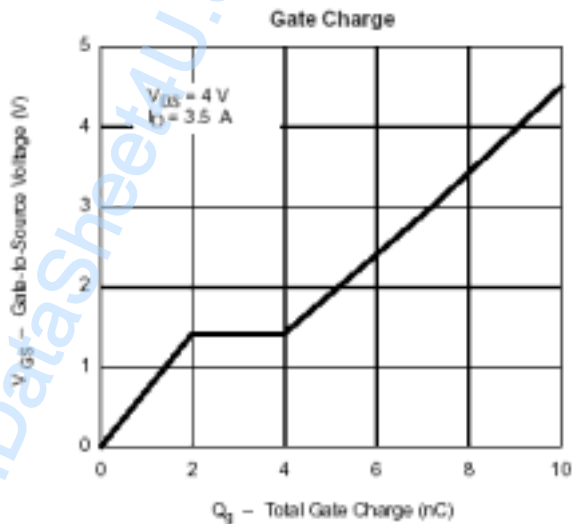
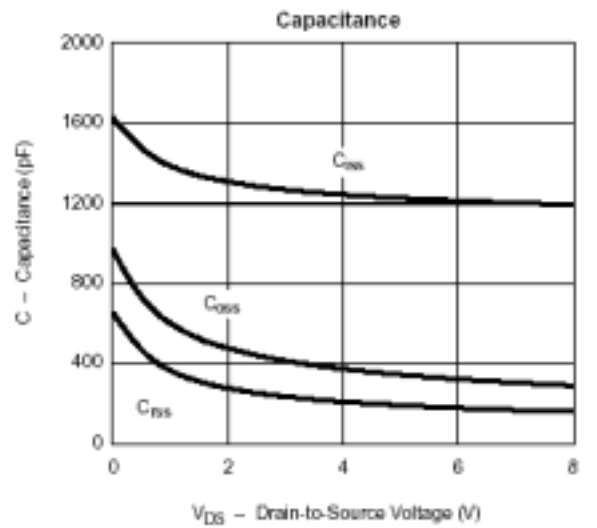
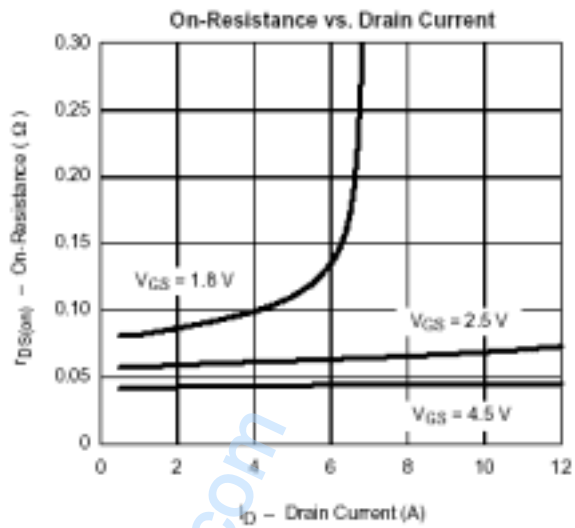
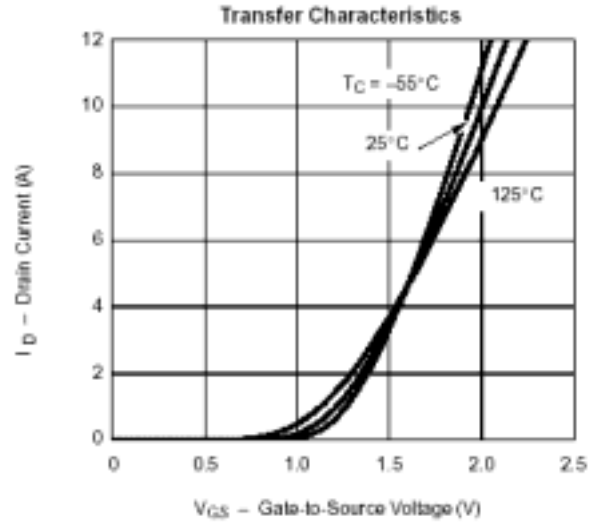
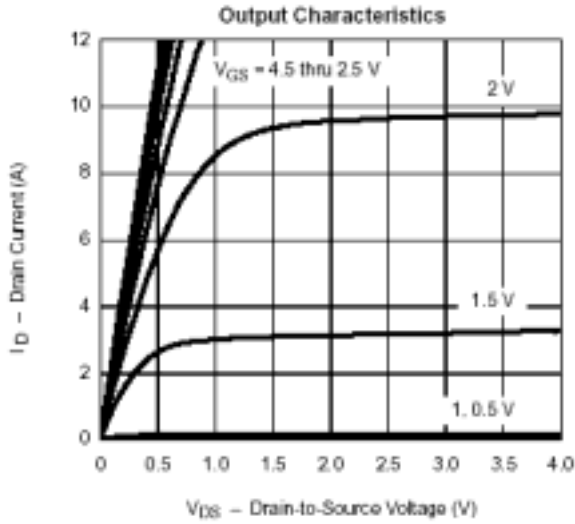

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