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**P Channel Enhancement Mode MOSFET      ST2301**

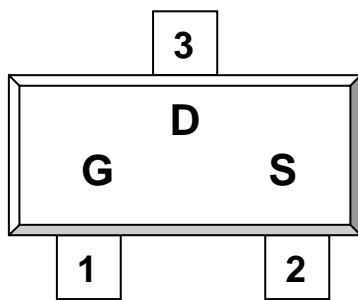

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**-2.8A****DESCRIPTION**

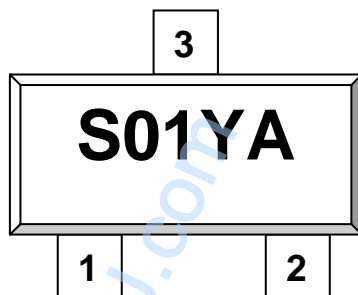
The ST2301 is the P-Channel logic enhancement mode power field effect transistor are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other batter powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

**PIN CONFIGURATION**  
**SOT-23-3L**


1.Gate   2.Source   3.Drain



S: Subcontractor   Y: Year Code   A: Process Code

**FEATURE**

- -20V/-2.8A,  $R_{DS(ON)} = 120\text{m-ohm}$  @VGS = -4.5V
- -20V/-2.0A,  $R_{DS(ON)} = 170\text{m-ohm}$  @VGS = -2.5V
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3L package design

**STANSON TECHNOLOGY**

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**ABSOLUTE MAXIMUM RATINGS** (Ta = 25 Unless otherwise noted )

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V <sub>DSS</sub>	-20	V
Gate-Source Voltage	V <sub>GSS</sub>	+12	V
Continuous Drain Current (T <sub>J</sub> =150 )	I <sub>D</sub>	-2.5	A
		T <sub>A</sub> =25	
	T <sub>A</sub> =70		
Pulsed Drain Current	I <sub>DM</sub>	-10	A
Continuous Source Current (Diode Conduction)	I <sub>S</sub>	-1.6	A
Power Dissipation	P <sub>D</sub>	1.25	W
		T <sub>A</sub> =25	
	T <sub>A</sub> =70		
Operation Junction Temperature	T <sub>J</sub>	150	
Storage Temperature Range	T <sub>STG</sub>	-55/150	
Thermal Resistance-Junction to Ambient	R <sub>JA</sub>	120	/W


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**P Channel Enhancement Mode MOSFET ST2301****-2.5A****ELECTRICAL CHARACTERISTICS ( Ta = 25 Unless otherwise noted )**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.45		-1.5	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=+8V$			+100	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-30V, V_{GS}=0V$			-1	uA
		$V_{DS}=-30V, V_{GS}=0V$ $T_J=55$			-10	
On-State Drain Current	$I_{D(on)}$	$V_{DS} = -5V, V_{GS}=-4.5V$	-6			A
		$V_{DS} = -5V, V_{GS}=-2.5V$	-3			
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-2.8A$		0.09	0.12	
		$V_{GS}=-2.5V, I_D=-2.0A$		0.145	0.17	
Forward Transconductance	$g_{fs}$	$V_{DS}=-5V, I_D=-2.8V$		6.5		S
Diode Forward Voltage	$V_{SD}$	$I_S=-1.6A, V_{GS}=0V$		-0.8	-1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=-6V, V_{GS}=-4.5V$ $I_D = -2.8A$		5.8	10	nC
Gate-Source Charge	$Q_{gs}$			0.85		
Gate-Drain Charge	$Q_{gd}$			1.7		
Input Capacitance	$C_{iss}$	$V_{DS}=-6V, V_{GS}=0V$ $F=1MHz$		415		pF
Output Capacitance	$C_{oss}$			223		
Reverse Transfer Capacitance	$C_{rss}$			23		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-6V, R_L=6$ $I_D=-1A, V_{GEN}=-4.5V$ $R_G=6$		13	25	nS
	$t_r$			36	60	
Turn-Off Time	$t_{d(off)}$			42	70	
	$t_f$			34	60	

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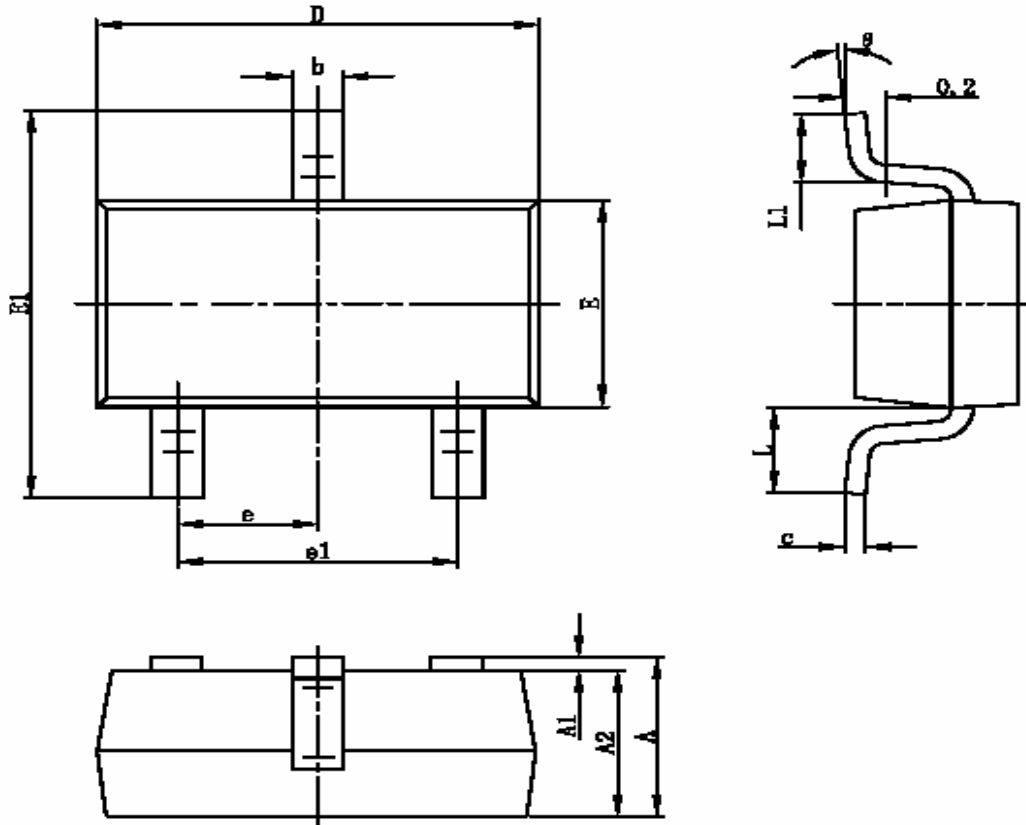
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## -2.5A

### SOT-23-3L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°



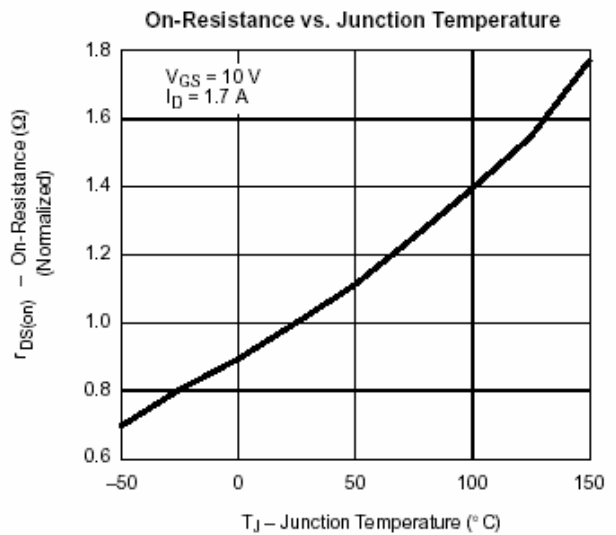
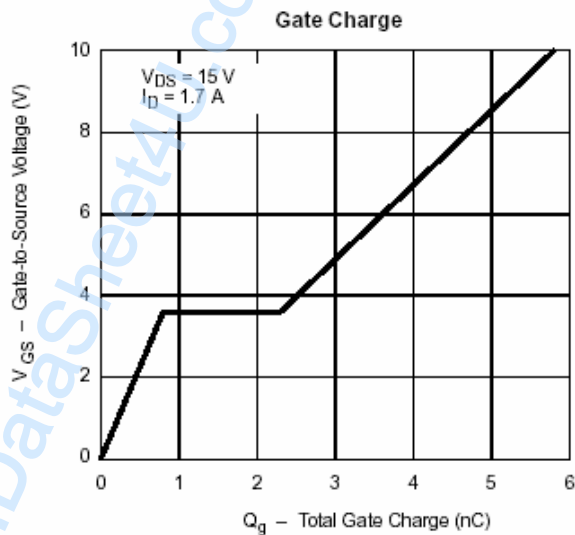
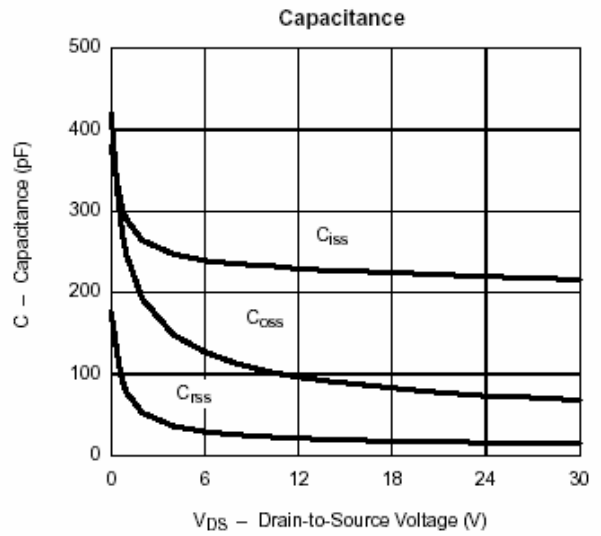
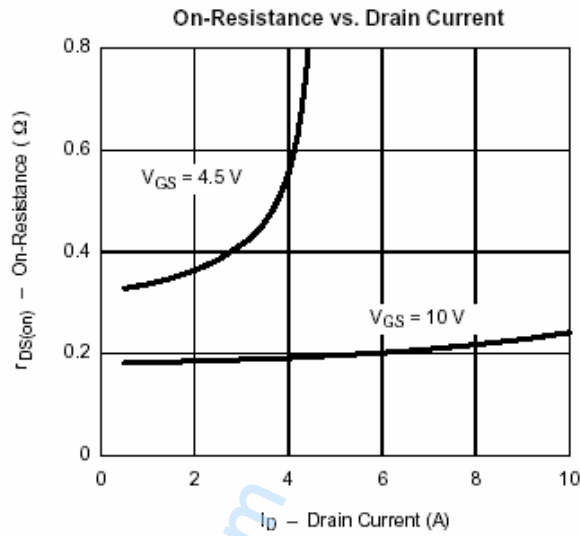
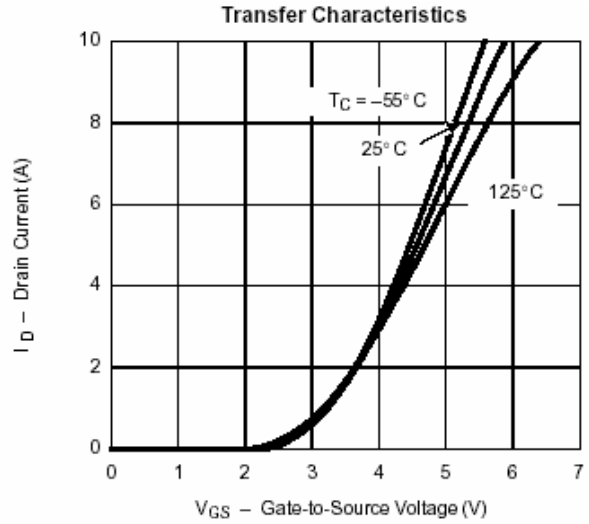
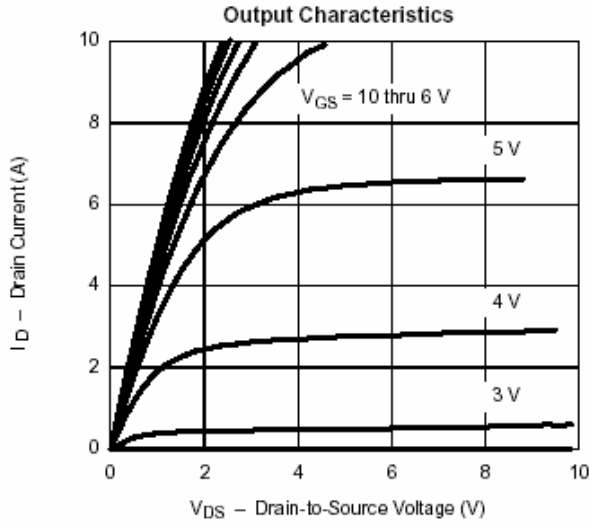
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## TYPICAL CHARACTERISTICS (25 Unless noted)



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