Sitronix

ST7577

132 x 39 Dot Matrix LCD Controller/Driver

1. INTRODUCTION

ST7577 is a driver & controller LSI for graphic dot-matrix liquid crystal display systems. ST7577 contains 132 segment and 39 common driver circuits. This chip is connected directly to a microprocessor, accepts 3-line, 4-line serial peripheral interface (SPI) or 8-bit parallel interface, display data can stores in an on-chip Display Data RAM (DDRAM) of 132 x 39 bits. It performs Display Data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

Single-chip LCD controller & driver

Driver Output Circuits

- 132 segments / 39 commons (DTY="L")
- 132 segments / 12 commons (DTY="H")

On-chip Display Data RAM (DDRAM)

- Capacity: 132X39=5148 bits

Microprocessor Interface

- 8-bit parallel bi-directional interface with 6800-series or 8080-series
- 4-line SPI (serial peripheral interface) available (only write operation)
- 3-line SPI (serial peripheral interface) available

On-chip Low Power Analog Circuit

- Embedded Boosters with voltage regulation function that generates high-accuracy voltage (externally V0I / XV0I voltage supply is also supported).
- Voltage regulation temperature gradient -0.07%/°C
- Programmable Booster stages: X3,X4.
- On-chip electronic contrast control function
- Built-in Voltage Follower generates LCD bias voltages (1/4 to 1/7).

Built-in oscillator

- Built-in oscillator requires no external components (external clock input is also supported)

External RESB (reset) pin

Supply voltage range

- V_{DD} - V_{SS} (Digital): 2.4 to 3.3V (typical);
- V_{DD2} - V_{SS} (Analog): 2.4 to 3.3V (typical).

Display supply voltage (V0-V_{SS}) range: 3.0V~8.31V

Temperature range: -30 to +85 degree

Support LCD Module Size up to 1.4"

ST7577	**6800 , 8080 , 4-Line , 3-Line interface**	

3. ST7577 Pad Arrangement (COG)

Chip Size: 6074μm(X) x 720μm(Y)

Chip Thickness: 480μm

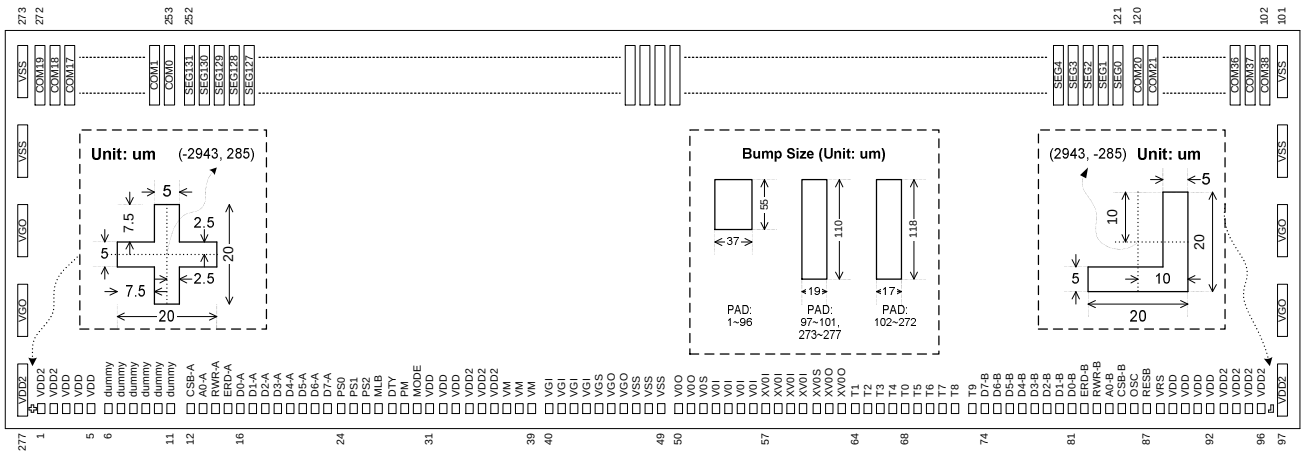
Bump Height: 15μm

PAD Pitch:

PAD	Pitch	PAD	Pitch	PAD	Pitch	PAD	Pitch
1~5	60	40~49	60	97~101	130	253~272	34
5~6	84.5	49~50	70	101~102	69	272~273	69
6~11	60	50~72	60	102~120	34	273~277	130
11~12	84.5	72~73	70	120~121	57	277-1	83
12~39	60	73~96	60	121~252	34		
39~40	89	96~97	83	252~253	57		

Rough layout

- For easy LCM design, the Power-1, Power-2 & Power-3 are identical (any one of them can be used). Power-3 has VGI, VGS, V0O, V0I, V0S, XV0O, XV0I and XV0S which are not in Power-1 or Power-2.
- I/O Port-A and I/O Port-B are identical (except “RESB” pin). “MODE” pin is used to select Port-A or Port-B. Please note the unused pins should be left floating.



4. Pad Center Coordinates

PAD No.	PAD Name	X	Y
1	VDD2	-2899.00	-286.50
2	VDD2	-2839.00	-286.50
3	VDD	-2779.00	-286.50
4	VDD	-2719.00	-286.50
5	VDD	-2659.00	-286.50
6	dummy	-2574.50	-286.50
7	dummy	-2514.50	-286.50
8	dummy	-2454.50	-286.50
9	dummy	-2394.50	-286.50
10	dummy	-2334.50	-286.50
11	dummy	-2274.50	-286.50
12	CSB_A	-2190.00	-286.50
13	A0_A	-2130.00	-286.50
14	RWR_A	-2070.00	-286.50
15	ERD_A	-2010.00	-286.50
16	D0_A	-1950.00	-286.50
17	D1_A	-1890.00	-286.50
18	D2_A	-1830.00	-286.50
19	D3_A	-1770.00	-286.50
20	D4_A	-1710.00	-286.50
21	D5_A	-1650.00	-286.50
22	D6_A	-1590.00	-286.50
23	D7_A	-1530.00	-286.50
24	PS0	-1470.00	-286.50
25	PS1	-1410.00	-286.50
26	PS2	-1350.00	-286.50
27	MLB	-1290.00	-286.50
28	DTY	-1230.00	-286.50
29	PM	-1170.00	-286.50
30	MODE	-1110.00	-286.50
31	VDD	-1050.00	-286.50
32	VDD	-990.00	-286.50
33	VDD	-930.00	-286.50
34	VDD2	-870.00	-286.50
35	VDD2	-810.00	-286.50
36	VDD2	-750.00	-286.50
37	VM	-690.00	-286.50
38	VM	-630.00	-286.50
39	VM	-570.00	-286.50
40	VGI	-481.00	-286.50
41	VGI	-421.00	-286.50
42	VGI	-361.00	-286.50
43	VGI	-301.00	-286.50
44	VGS	-241.00	-286.50
45	VGO	-181.00	-286.50

PAD No.	PAD Name	X	Y
46	VGO	-121.00	-286.50
47	VSS	-61.00	-286.50
48	VSS	-1.00	-286.50
49	VSS	59.00	-286.50
50	V0O	129.00	-286.50
51	V0O	189.00	-286.50
52	V0S	249.00	-286.50
53	V0I	309.00	-286.50
54	V0I	369.00	-286.50
55	V0I	429.00	-286.50
56	V0I	489.00	-286.50
57	XV0I	549.00	-286.50
58	XV0I	609.00	-286.50
59	XV0I	669.00	-286.50
60	XV0I	729.00	-286.50
61	XV0S	789.00	-286.50
62	XV0O	849.00	-286.50
63	XV0O	909.00	-286.50
64	T1	969.00	-286.50
65	T2	1029.00	-286.50
66	T3	1089.00	-286.50
67	T4	1149.00	-286.50
68	T0	1209.00	-286.50
69	T5	1269.00	-286.50
70	T6	1329.00	-286.50
71	T7	1389.00	-286.50
72	T8	1449.00	-286.50
73	T9	1519.00	-286.50
74	D7_B	1579.00	-286.50
75	D6_B	1639.00	-286.50
76	D5_B	1699.00	-286.50
77	D4_B	1759.00	-286.50
78	D3_B	1819.00	-286.50
79	D2_B	1879.00	-286.50
80	D1_B	1939.00	-286.50
81	D0_B	1999.00	-286.50
82	ERD_B	2059.00	-286.50
83	RWR_B	2119.00	-286.50
84	A0_B	2179.00	-286.50
85	CSB_B	2239.00	-286.50
86	OSC	2299.00	-286.50
87	RESB	2359.00	-286.50
88	VRS	2419.00	-286.50
89	VDD	2479.00	-286.50
90	VDD	2539.00	-286.50

PAD No.	PAD Name	X	Y
91	VDD	2599.00	-286.50
92	VDD	2659.00	-286.50
93	VDD2	2719.00	-286.50
94	VDD2	2779.00	-286.50
95	VDD2	2839.00	-286.50
96	VDD2	2899.00	-286.50
97	VDD2	2982.00	-260.00
98	VGO	2982.00	-130.00
99	VGO	2982.00	0.00
100	VSS	2982.00	130.00
101	VSS	2982.00	260.00
102	COM[38]	2913.00	255.00
103	COM[37]	2879.00	255.00
104	COM[36]	2845.00	255.00
105	COM[35]	2811.00	255.00
106	COM[34]	2777.00	255.00
107	COM[33]	2743.00	255.00
108	COM[32]	2709.00	255.00
109	COM[31]	2675.00	255.00
110	COM[30]	2641.00	255.00
111	COM[29]	2607.00	255.00
112	COM[28]	2573.00	255.00
113	COM[27]	2539.00	255.00
114	COM[26]	2505.00	255.00
115	COM[25]	2471.00	255.00
116	COM[24]	2437.00	255.00
117	COM[23]	2403.00	255.00
118	COM[22]	2369.00	255.00
119	COM[21]	2335.00	255.00
120	COM[20]	2301.00	255.00
121	SEG[0]	2244.00	255.00
122	SEG[1]	2210.00	255.00
123	SEG[2]	2176.00	255.00
124	SEG[3]	2142.00	255.00
125	SEG[4]	2108.00	255.00
126	SEG[5]	2074.00	255.00
127	SEG[6]	2040.00	255.00
128	SEG[7]	2006.00	255.00
129	SEG[8]	1972.00	255.00
130	SEG[9]	1938.00	255.00
131	SEG[10]	1904.00	255.00
132	SEG[11]	1870.00	255.00
133	SEG[12]	1836.00	255.00
134	SEG[13]	1802.00	255.00
135	SEG[14]	1768.00	255.00

PAD No.	PAD Name	X	Y
136	SEG[15]	1734.00	255.00
137	SEG[16]	1700.00	255.00
138	SEG[17]	1666.00	255.00
139	SEG[18]	1632.00	255.00
140	SEG[19]	1598.00	255.00
141	SEG[20]	1564.00	255.00
142	SEG[21]	1530.00	255.00
143	SEG[22]	1496.00	255.00
144	SEG[23]	1462.00	255.00
145	SEG[24]	1428.00	255.00
146	SEG[25]	1394.00	255.00
147	SEG[26]	1360.00	255.00
148	SEG[27]	1326.00	255.00
149	SEG[28]	1292.00	255.00
150	SEG[29]	1258.00	255.00
151	SEG[30]	1224.00	255.00
152	SEG[31]	1190.00	255.00
153	SEG[32]	1156.00	255.00
154	SEG[33]	1122.00	255.00
155	SEG[34]	1088.00	255.00
156	SEG[35]	1054.00	255.00
157	SEG[36]	1020.00	255.00
158	SEG[37]	986.00	255.00
159	SEG[38]	952.00	255.00
160	SEG[39]	918.00	255.00
161	SEG[40]	884.00	255.00
162	SEG[41]	850.00	255.00
163	SEG[42]	816.00	255.00
164	SEG[43]	782.00	255.00
165	SEG[44]	748.00	255.00
166	SEG[45]	714.00	255.00
167	SEG[46]	680.00	255.00
168	SEG[47]	646.00	255.00
169	SEG[48]	612.00	255.00
170	SEG[49]	578.00	255.00
171	SEG[50]	544.00	255.00
172	SEG[51]	510.00	255.00
173	SEG[52]	476.00	255.00
174	SEG[53]	442.00	255.00
175	SEG[54]	408.00	255.00
176	SEG[55]	374.00	255.00
177	SEG[56]	340.00	255.00
178	SEG[57]	306.00	255.00
179	SEG[58]	272.00	255.00
180	SEG[59]	238.00	255.00

PAD No.	PAD Name	X	Y
181	SEG[60]	204.00	255.00
182	SEG[61]	170.00	255.00
183	SEG[62]	136.00	255.00
184	SEG[63]	102.00	255.00
185	SEG[64]	68.00	255.00
186	SEG[65]	34.00	255.00
187	SEG[66]	0.00	255.00
188	SEG[67]	-34.00	255.00
189	SEG[68]	-68.00	255.00
190	SEG[69]	-102.00	255.00
191	SEG[70]	-136.00	255.00
192	SEG[71]	-170.00	255.00
193	SEG[72]	-204.00	255.00
194	SEG[73]	-238.00	255.00
195	SEG[74]	-272.00	255.00
196	SEG[75]	-306.00	255.00
197	SEG[76]	-340.00	255.00
198	SEG[77]	-374.00	255.00
199	SEG[78]	-408.00	255.00
200	SEG[79]	-442.00	255.00
201	SEG[80]	-476.00	255.00
202	SEG[81]	-510.00	255.00
203	SEG[82]	-544.00	255.00
204	SEG[83]	-578.00	255.00
205	SEG[84]	-612.00	255.00
206	SEG[85]	-646.00	255.00
207	SEG[86]	-680.00	255.00
208	SEG[87]	-714.00	255.00
209	SEG[88]	-748.00	255.00
210	SEG[89]	-782.00	255.00
211	SEG[90]	-816.00	255.00
212	SEG[91]	-850.00	255.00
213	SEG[92]	-884.00	255.00
214	SEG[93]	-918.00	255.00
215	SEG[94]	-952.00	255.00
216	SEG[95]	-986.00	255.00
217	SEG[96]	-1020.00	255.00
218	SEG[97]	-1054.00	255.00
219	SEG[98]	-1088.00	255.00
220	SEG[99]	-1122.00	255.00
221	SEG[100]	-1156.00	255.00
222	SEG[101]	-1190.00	255.00
223	SEG[102]	-1224.00	255.00
224	SEG[103]	-1258.00	255.00
225	SEG[104]	-1292.00	255.00

PAD No.	PAD Name	X	Y
226	SEG[105]	-1326.00	255.00
227	SEG[106]	-1360.00	255.00
228	SEG[107]	-1394.00	255.00
229	SEG[108]	-1428.00	255.00
230	SEG[109]	-1462.00	255.00
231	SEG[110]	-1496.00	255.00
232	SEG[111]	-1530.00	255.00
233	SEG[112]	-1564.00	255.00
234	SEG[113]	-1598.00	255.00
235	SEG[114]	-1632.00	255.00
236	SEG[115]	-1666.00	255.00
237	SEG[116]	-1700.00	255.00
238	SEG[117]	-1734.00	255.00
239	SEG[118]	-1768.00	255.00
240	SEG[119]	-1802.00	255.00
241	SEG[120]	-1836.00	255.00
242	SEG[121]	-1870.00	255.00
243	SEG[122]	-1904.00	255.00
244	SEG[123]	-1938.00	255.00
245	SEG[124]	-1972.00	255.00
246	SEG[125]	-2006.00	255.00
247	SEG[126]	-2040.00	255.00
248	SEG[127]	-2074.00	255.00
249	SEG[128]	-2108.00	255.00
250	SEG[129]	-2142.00	255.00
251	SEG[130]	-2176.00	255.00
252	SEG[131]	-2210.00	255.00
253	COM[0]	-2267.00	255.00
254	COM[1]	-2301.00	255.00
255	COM[2]	-2335.00	255.00
256	COM[3]	-2369.00	255.00
257	COM[4]	-2403.00	255.00
258	COM[5]	-2437.00	255.00
259	COM[6]	-2471.00	255.00
260	COM[7]	-2505.00	255.00
261	COM[8]	-2539.00	255.00
262	COM[9]	-2573.00	255.00
263	COM[10]	-2607.00	255.00
264	COM[11]	-2641.00	255.00
265	COM[12]	-2675.00	255.00
266	COM[13]	-2709.00	255.00
267	COM[14]	-2743.00	255.00
268	COM[15]	-2777.00	255.00
269	COM[16]	-2811.00	255.00
270	COM[17]	-2845.00	255.00

PAD No.	PAD Name	X	Y
271	COM[18]	-2879.00	255.00
272	COM[19]	-2913.00	255.00
273	VSS	-2982.00	260.00
274	VSS	-2982.00	130.00
275	VGO	-2982.00	0.00
276	VGO	-2982.00	-130.00
277	VDD2	-2982.00	-260.00

* Unit: μm

* “dummy” pads are floating and not connected to any part of circuits.
* Please refer to Page6 for detail output Map (especially for 1/12 & 1/39 duty).

5. BLOCK DIAGRAM

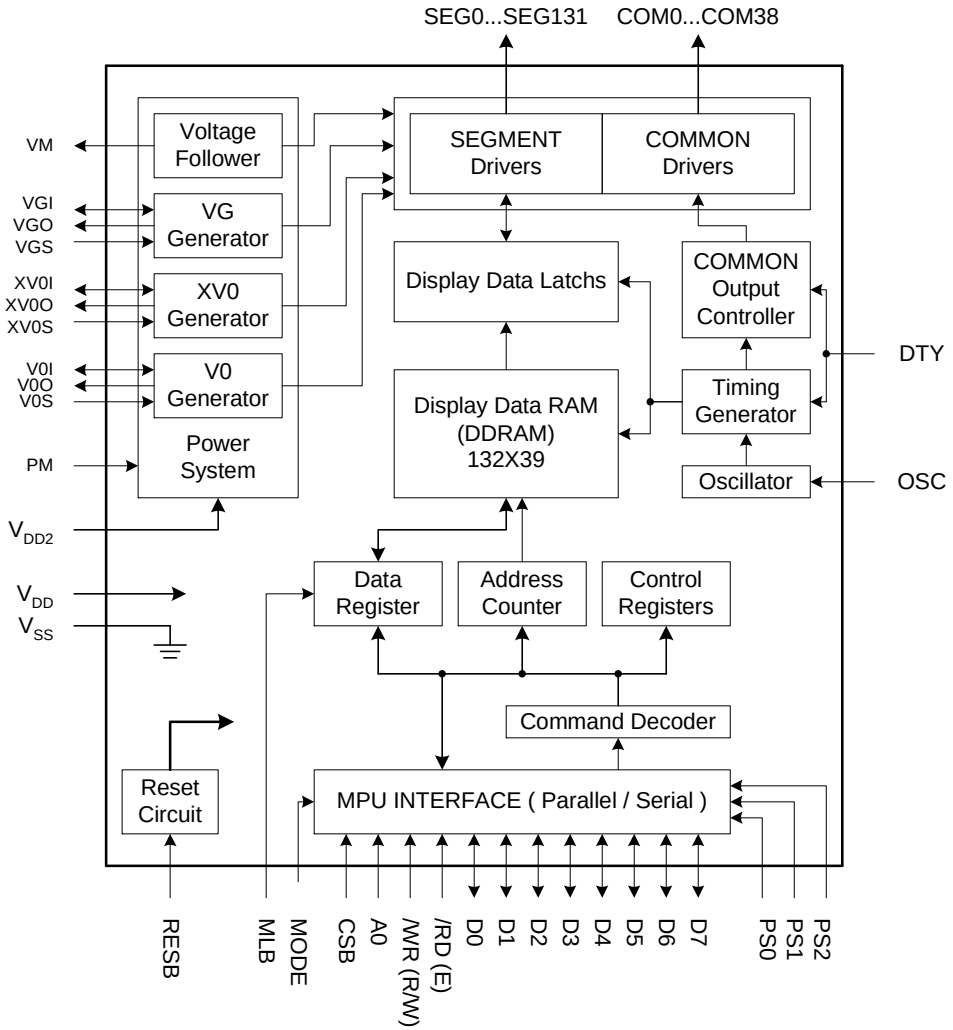


Figure 1 Block Diagram

6. PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Pin Count</th></tr>
<tr><td colspan="4">LCD DRIVER OUTPUTS</td></tr>
<tr><td>SEG0…SEG131</td><td>O</td><td>LCD segment driver outputs.
This display data and the M signal control the output voltage of segment driver.
<table>
<tr><th rowspan="2">Display data</th><th rowspan="2">Frame</th><th colspan="2">Segment drover output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>+</td><td>VG</td><td>V_{SS}</td></tr>
<tr><td>H</td><td>-</td><td>V_{SS}</td><td>VG</td></tr>
<tr><td>L</td><td>+</td><td>V_{SS}</td><td>VG</td></tr>
<tr><td>L</td><td>-</td><td>VG</td><td>V_{SS}</td></tr>
<tr><td colspan="2">Power save mode</td><td>V_{SS}</td><td>V_{SS}</td></tr>
</table></td><td>132</td></tr>
<tr><td>COM0…COM38</td><td>O</td><td>LCD column driver outputs.
This internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><th rowspan="2">Display data</th><th rowspan="2">Frame</th><th colspan="2">Common drover output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>+</td><td colspan="2">XV0</td></tr>
<tr><td>H</td><td>-</td><td colspan="2">V0</td></tr>
<tr><td>L</td><td>+</td><td colspan="2">VM</td></tr>
<tr><td>L</td><td>-</td><td colspan="2">VM</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">V_{SS}</td></tr>
</table></td><td>39</td></tr>
<tr><td colspan="4">MICROPROCESSOR INTERFACE</td></tr>
<tr><td>PS0…PS2</td><td>I</td><td>Microprocessor interface select input pin.
<table>
<tr><th>PS2</th><th>PS1</th><th>PS0</th><th>State</th></tr>
<tr><td>“L”</td><td>“L”</td><td>“L”</td><td>4 Pin-SPI MPU interface</td></tr>
<tr><td>“H”</td><td>“L”</td><td>“L”</td><td>3 Pin-SPI MPU interface</td></tr>
<tr><td>“L”</td><td>“H”</td><td>“L”</td><td>8080-series parallel MPU interface</td></tr>
<tr><td>“H”</td><td>“H”</td><td>“L”</td><td>6800-series parallel MPU interface</td></tr>
</table></td><td>3</td></tr>
<tr><td>CSB_A
(for Port-A)
CSB_B
(for Port-B)</td><td>I</td><td>Chip select input pins.
Data/instruction I/O is enabled only when CSB is “L”. When chip select is non-active, D0 to D7 is high impedance.
* MODE pin will select one of two CSB pins. The unused one should be left floating.</td><td>1*

1*</td></tr>
<tr><td>RESB</td><td>I</td><td>Reset input pin.
When RESB is “L”, initialization is executed.</td><td>1</td></tr>
<tr><td>A0_A
(for Port-A)
A0_B
(for Port-B)</td><td>I</td><td>It determines whether the data bits are data or a command.
A0=“H”: Indicates that D0 to D7 are display data.
A0=“L”: Indicates that D0 to D7 are control data.
When in 3-line SPI interface, left it connected to V_{DD}.
* MODE pin will select one of two A0 pins. The unused one should be left floating.</td><td>1*

1*</td></tr>
</table>

<table>
<tr>
<td>RWR_A
(for Port-A)
RWR_B
(for Port-B)</td>
<td>I</td>
<td>Read/Write execution control pin (PS[0:1]=[L:H]).
<table>
<tr><th>PS2</th><th>MPU type</th><th>RWR</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>R/W</td><td>Read/Write control input pin
R/W=“H”: read;
R/W=“L”: write.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data on D0 to D7 are latched at the rising edge of the /WR signal.</td></tr>
</table>
When in the serial interface, left it connected to V_{DD}.
* MODE pin will select one of two RWR pins. The unused one should be left floating.</td>
<td>1*

1*</td>
</tr>
<tr>
<td>ERD_A
(for Port-A)
ERD_B
(for Port-B)</td>
<td>I</td>
<td>Read/Write execution control pin (PS[0:1]=[L:H]).
<table>
<tr><th>PS2</th><th>MPU Type</th><th>/RD(E)</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read/Write control input pin
R/W=“H”: When E is “H”, D0 to D7 are in an output status;
R/W=“L”: The data on D0 to D7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RD</td><td>Read enable clock input pin.
When /RD is “L”, D0 to D7 are in an output status.</td></tr>
</table>
When in the serial interface, left it connected to V_{DD}.
* MODE pin will select one of two RWR pins. The unused one should be left floating.</td>
<td>1*

1*</td>
</tr>
<tr>
<td>D7_A…D0_A
(for Port-A)
D7_B…D0_B
(for Port-B)</td>
<td>I/O</td>
<td>When using 8-bit parallel interface: 6800, 8080
8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus.
When chip select is not active, D0 to D7 is high impedance.

When using serial interface: 4-LINE
D0: serial input clock (SCLK);
D1, D2, D3: serial input data (SDA), must be connected together;
D4~D7 must be connected to V_{DD} (not used).
When chip select is not active, D0 to D7 is high impedance.

When using serial interface: 3-LINE
D0: serial input clock (SCLK).
D1, D2, D3: serial input data (SDA), must be connected together;
D4~D7 must be connected to V_{DD} (not used).
When chip select is not active, D0 to D7 is high impedance.</td>
<td>8*

8*</td>
</tr>
</table>

LCD DRIVER CLOCK SUPPLY			
OSC	**I**	**When the on-chip oscillator is used, this input must be connected to V_{DD}.** An external clock signal, if used, is connected to this pin. The oscillator and external clock are both inhibited by connecting the OSC pin to V_{SS} and the display is not clocked and may be left in a DC state. To avoid this, the chip should always be put into Power Down Mode before stopping the clock.	**1**
POWER SUPPLY PIN			
V_{SS}	**Power**	Ground.	**3**
V_{DD}	**Power**	Digital Supply voltage. The 2 supply rails, V_{DD} and V_{DD2} , could be connected together (for single power). **If a Digital Option pin is high, must be this level.**	**10**
V_{DD2}	**Power**	Analog Supply voltage. The 2 supply rails, V_{DD} and V_{DD2} , could be connected together (for single power).	**9**
VRS	**Power**	Reference voltage. Must be left open.	**1**
V0I, V0O, V0S	**Power**	Positive LCD driving voltage for commons. V0I is the V0 power source for the LCD driver. If using external V0, apply the external power source on these pads. V0O is the internal V0 regulator output pad. V0S is the feedback for the internal V0 voltage compensation circuit. They should be separate in ITO and be connected together by FPC.	**7**
XV0I, XV0O,XV0S	**Power**	Negative LCD driving voltage for commons. XV0I is the XV0 power source for the LCD driver. If using external XV0, apply the external power source on these pads. XV0O is the internal XV0 regulator output pad. XV0S is the feedback for the internal XV0 voltage compensation circuit. They should be separate in ITO and be connected together by FPC.	**7**
VGI, VGO, VGS	**Power**	LCD driving voltage for segments. VGI is the VG power source for the LCD driver. If using external VG, apply external power source on these pads. VGO is the internal VG regulator output pad. VGS is the feedback for the internal VG voltage compensation circuit. They should be separate in ITO and be connected together by FPC.	**7**
VM	**Power**	LCD driving voltage for commons.	**3**

CONFIGURATION PIN			
MLB	I	Data format (MSB on top or LSB on top). MLB="H", MSB on top (D7 on top); MLB="L", LSB on top (D0 on top).	1
DTY	I	Duty selection pin. Please refer to Page11 for detail output Map. DTY="L", 1/39 duty; DTY="H", 1/12 duty.	1
PM	I	Set power mode. This pin will change the V0 (Vop) formula parameter. V0=(a + $V_{OP[6:0]}$ x b) PM="L", a=3.0V, b=0.03V; PM="H", a=4.5V, b=0.03V.	1
MODE	I	Select MPU interface Port-A (left side) or Port-B (right side). MODE="L", use Port-A (Port-B should be floating). MODE="H", use Port-B (Port-A should be floating).	1
TEST PIN			
T0~T9	Test	T0~T8 left them open. T9 must connect to V_{DD}.	10

- I ST7577 has 2 sets of interface port (Port-A & Port-B). These two ports can be selected by "MODE" pin. Port-A and Port-B are identical (CSB, A0, /RW, /RD, D7~D0) except RESB pin.
- I The unused pins should be left floating.
- I The Microprocessor Interface pins should not be left floating under any operation mode.

Recommend I/O pins ITO Resistance Limitation

Pin Name	ITO Resistance
VRS, T[8:0]	**Floating**
V_{SS}	**<100Ω**
V_{DD}	**<100Ω**
V_{DD2}	**<100Ω**
V0 (V0I + V0O + V0S), XV0 (XV0I + XV0O + XV0S), VG (VGI + VGO + VGS), VM	**<500Ω**
CSB, A0, /RD, /WR, D[7:0]	**<1KΩ**
PS[2:0], OSC[*1], MLB, DTY, MODE, T9	**<5KΩ**
RESB	**<10KΩ**

Notes:

1. If using internal clock, OSC is connect to V_{DD} and the limitation of ITO resistance will be "No Limitation". If using external clock, the ITO resistance of OSC should be kept lower than 500Ω to keep the clock signal quality.

7. FUNCTIONS DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

The CSB pin is used for chip selection. ST7577 can interface with an MPU when CSB is "L". When CSB is “H”, the control pins (A0, /RD and /WR) are disabled and D0 to D7 are set to be high impedance. If using serial interface, the internal shift register and the counter are reset when CSB=”H”.

Parallel / Serial Interface

ST7577 has five types of interface to communicate with an MPU, which are three serial and two parallel interfaces. The parallel or serial interface is determined by PS[2:0] pin as shown below.

Table 1 Parallel/Serial Interface Selection

PS2	PS1	PS0	CSB	A0	State
“L”	“L”	“L”	CSB	A0	4 Pin-SPI MPU interface
“H”	“L”	“L”	CSB	"H"	3 Pin-SPI MPU interface
“L”	“H”	“L”	CSB	A0	8080-series parallel MPU interface
“H”	“H”	“L”	CSB	A0	6800-series parallel MPU interface

Parallel Interface

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by PS[2:0] as shown in Table 2. The type of data transfer is determined by A0, ERD and RWR as shown in Table 3.

Table 2 Microprocessor Selection for Parallel Interface

PS2	PS1	PS0	CSB	A0	ERD	RWR	DB0 to DB7	MPU bus
H	H	L	CSB	A0	E	R/W	DB0 to DB7	6800-series
L	H	L	CSB	A0	/RD	/WR	DB0 to DB7	8080-series

Table 3 Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	E (/RD)	R/W (/WR)	/RD (E)	/WR (R/W)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

NOTE: When ERD pin is always pulled high in 6800-series interface, the CSB can be used as enable signal. In this case, interface data is latched at the rising edge of CSB and the access type is determined by A0, RWR as 6800-series mode.

Serial Interface

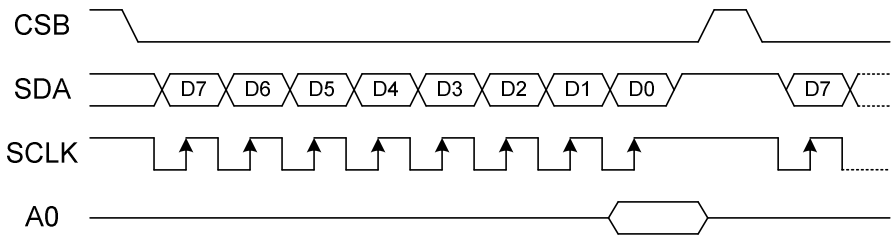
ST7577 supports 2 kinds of serial interface and the type is selected by PS2~PS0 as shown below.

Serial Mode	PS2	PS1	PS0	CSB	A0
4-line SPI interface	L	L	L	CSB	A0
3-line SPI interface	H	L	L	CSB	Not Used Fix to “H”

PS2="L", PS1="L", PS0="L": 4-line SPI interface

When ST7577 is set into 4-line SPI interface mode, setting CSB to be "L" will active this chip. If CSB is "H", the internal 8-bit shift register and a 3-bit counter are reset. When CSB is "L", the serial data (SDA) and the serial clock (SCLK) are set into input mode. The input signal on SDA will be latched into the shift register from D7 to D0 at the rising edge of the serial clock. The display data/instruction indication is controlled via the register select pin: A0. If A0="L", the input signal on SDA will be treated as instruction; if A0="H", the input signal on SDA will be treated as data. After 8-bit data are written into the Data Display RAM, the DDRAM column address pointer will be increased by one automatically.

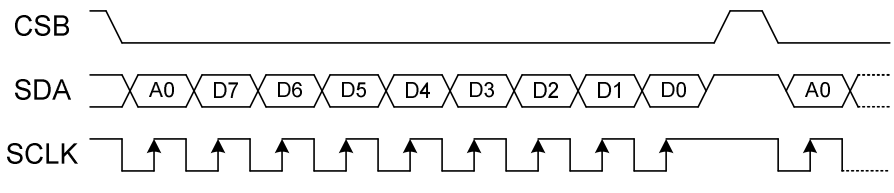
Figure 2 4-line SPI Timing



PS2="H", PS1="L", PS0="L": 3-line SPI interface

Because 3-line SPI interface mode does not have a register selection pin "A0", this mode latches the A0 bit first and then latches 8-bit input (please refer to the following figure).

Figure 3 3-line SPI Timing



Data Transfer

ST7577 uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in Figure 4. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in Figure 5. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

Figure 4 Write Timing

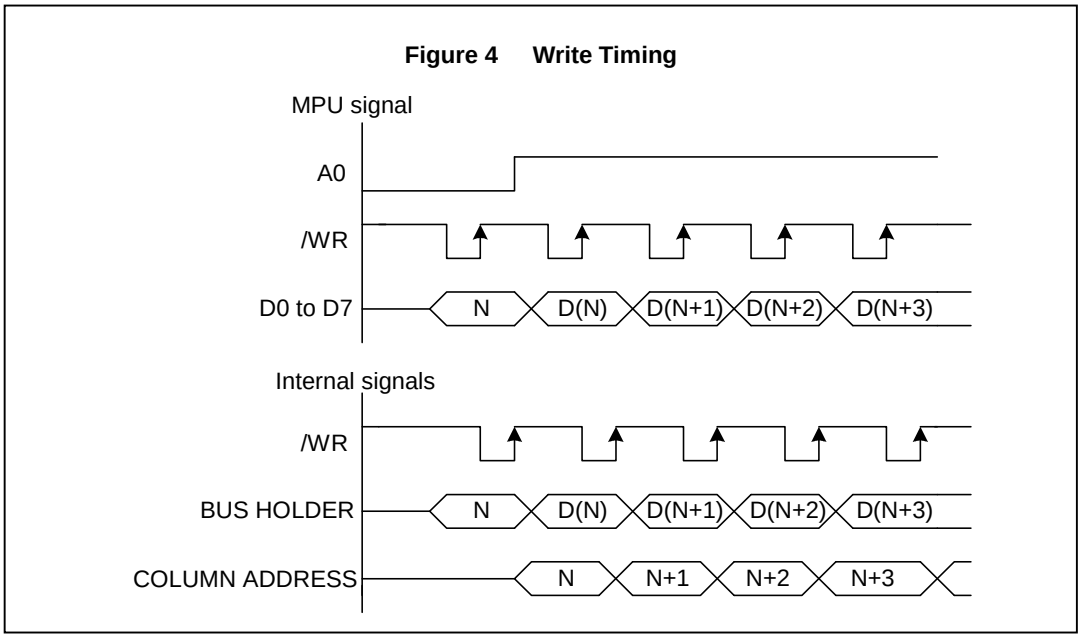
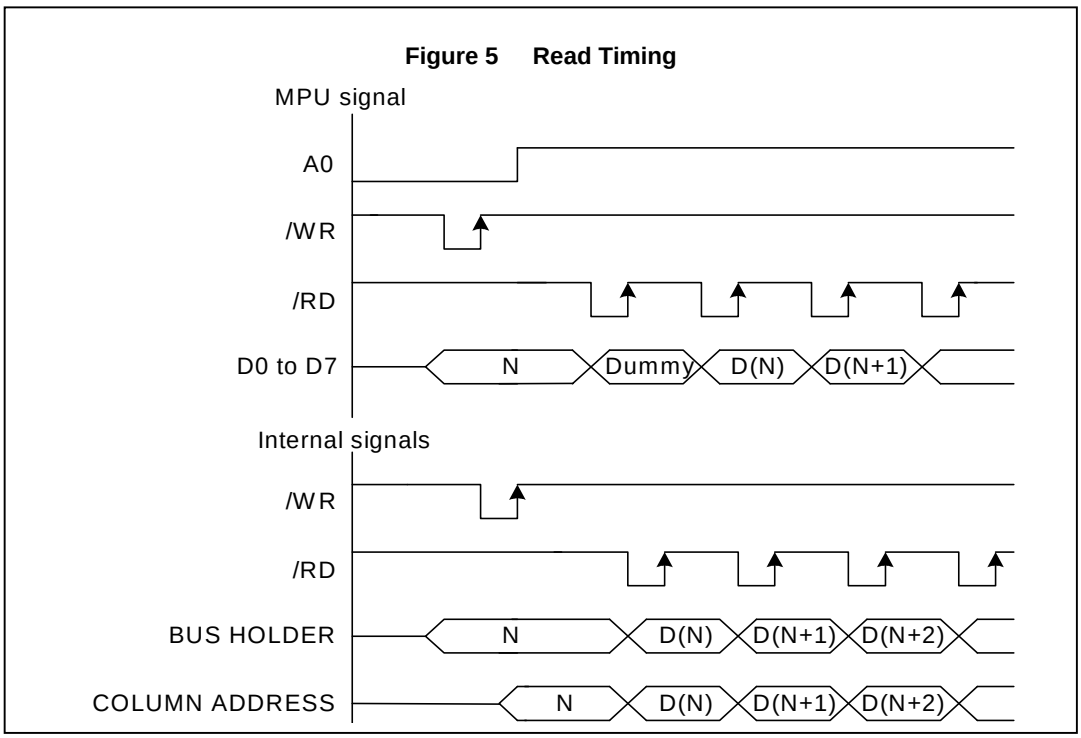


Figure 5 Read Timing



DISPLAY DATA RAM (DDRAM)

ST7577 contains a 132X39 bit static RAM that stores the display data. The Display Data RAM stores the dot data for the LCD display. It is 132-column by 39-row addressable array: 132X39 (4-page X 8-bit + 1-page X 7-bit). Each pixel can be selected when the page and column addresses are specified. The 39 rows are divided into 4 pages (with 8 lines, COM 0~38) and the 4th page (with 7 lines, COM32~38). Data is read from or written to each page directly through D7 to D0. The display data (D7~D0) corresponds to the LCD common-line direction (default: top to down). The microprocessor can write to and read (only Parallel interfaces) from DDRAM by the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker or data-conflict.

DDRAM ORGANIZATION

Data is written in bytes into the RAM matrix of ST7577 as shown in Figure 6~Figure 9. The Display Data RAM is a matrix of 132 by 39 bits. The address pointer keeps the X and Y address. The valid address ranges are: X=0~131, Y=0~4.

The default data orientation of DDRAM is controlled by the hardware pin “MLB”.
When MLB=”L”, the data write into DDRAM is from D0~D7 (LSB on top). Please refer to Figure 6.
When MLB=”H”, the data write into DDRAM is from D7~D0 (MSB on top). Please refer to Figure 7.

Figure 6 DDRAM Format, If MLB=0

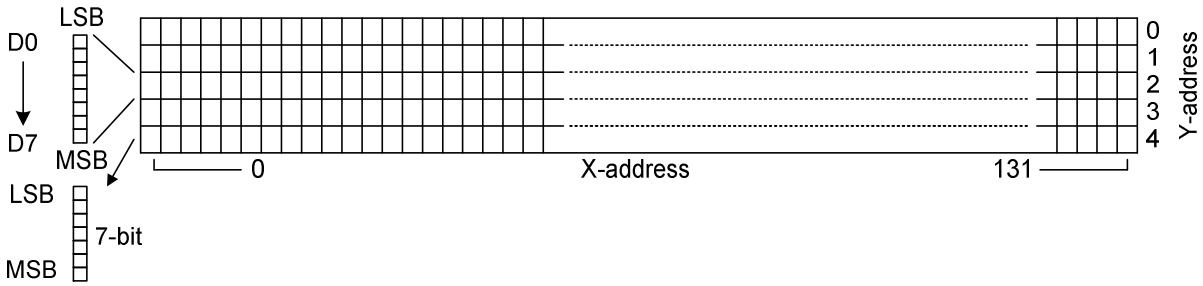
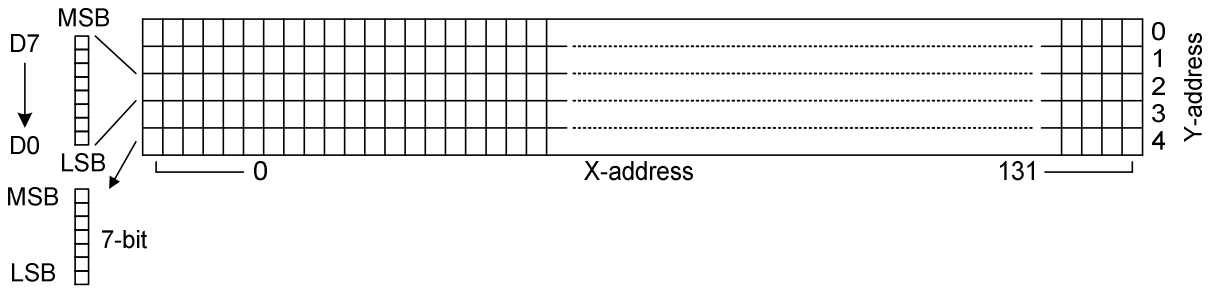


Figure 7 DDRAM Format, If MLB=1



COLUMN ADDRESS CIRCUIT

Column Address Circuit has an 8-bit preset counter that points to each column of DDRAM as shown in Figure 6. The valid range is from 0 to 131. The DDRAM column address can be specified by the Set X address instruction.

PAGE ADDRESS CIRCUIT

This circuit is for providing a page address to Display Data RAM. It incorporates 3-bit Y address register and can be programmed by the “Set Y address of RAM” instruction. Page Address 4 is a special RAM area for the rest display data where only 7-bit of RAM cells are valid (please refer to Figure 6 & Figure 7).

START LINE ADDRESS CIRCUIT

This circuit assigns DDRAM a line address that is scanned first at the beginning of each frame. By setting Start Line Address repeatedly, the display pattern looks like scrolling vertically in the screen without changing the contents of DDRAM (refer to Figure 11). When setting the Start Line Address (with “Set Start Line” instruction), the data of the same specified line address in DDRAM are transferred to the Display Data Latch Circuit at the beginning of each frame.

ADDRESSING

ST7577 will automatically increases the address when sequential access. This feature allows MPU to access the display data in DDRAM continuously without setting the address before each access.

In horizontal addressing mode, the X address is automatically increased by 1 after each byte access (refer to Figure 8). After the last X address (X=131), X address wraps around to 0 and Y address increases to the next page. After the very last address (X=131, Y=4), the address pointers wrap around to the original address (X=0, Y=0).

In vertical addressing mode, the Y address is automatically increased by 1 after each byte access (refer to Figure 9). After the last Y address (Y=4), Y address wraps around to 0 and X address increases to the next column. After the very last address (X=131, Y=4), the address pointers wrap around to the original address (X=0, Y=0).

Figure 8 Addressing Mode: Horizontal (V=0)

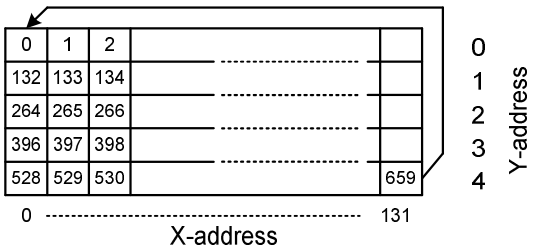


Figure 9 Addressing Mode: Vertical (V=1)

LCD DRIVER DISPLAY DIRECTION

Register bits XD (horizontal direction) and MY (vertical mirror) control the horizontal and vertical display direction. XD controls the X-address write direction in DDRAM while MY controls the common output direction. Therefore, it is necessary to rewrite the display data to DDRAM after changing XD-bit setting. Refer to the following figure.

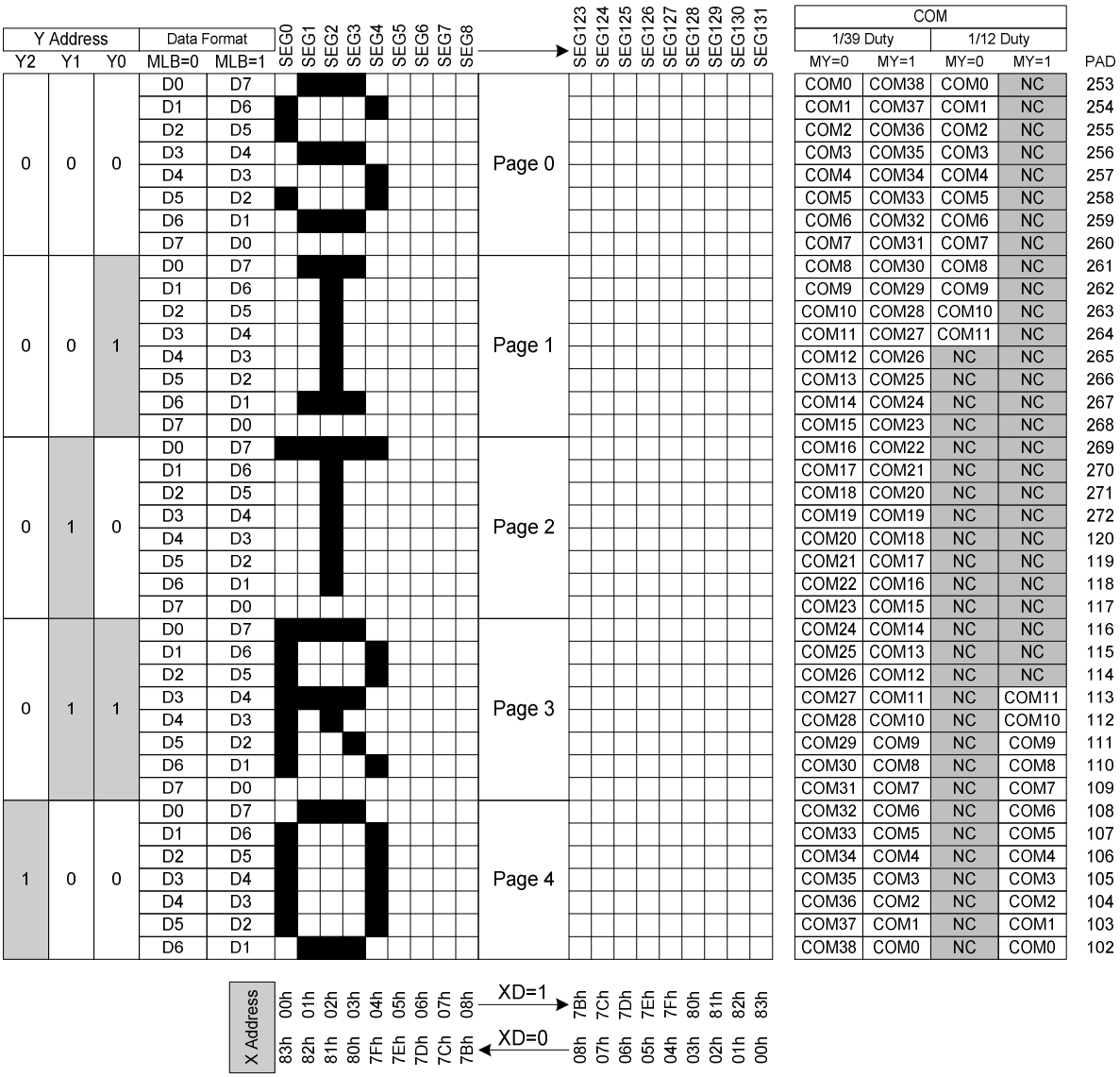


Figure 10 LCD Driver Display Direction

DDRAM MAP vs. START LINE

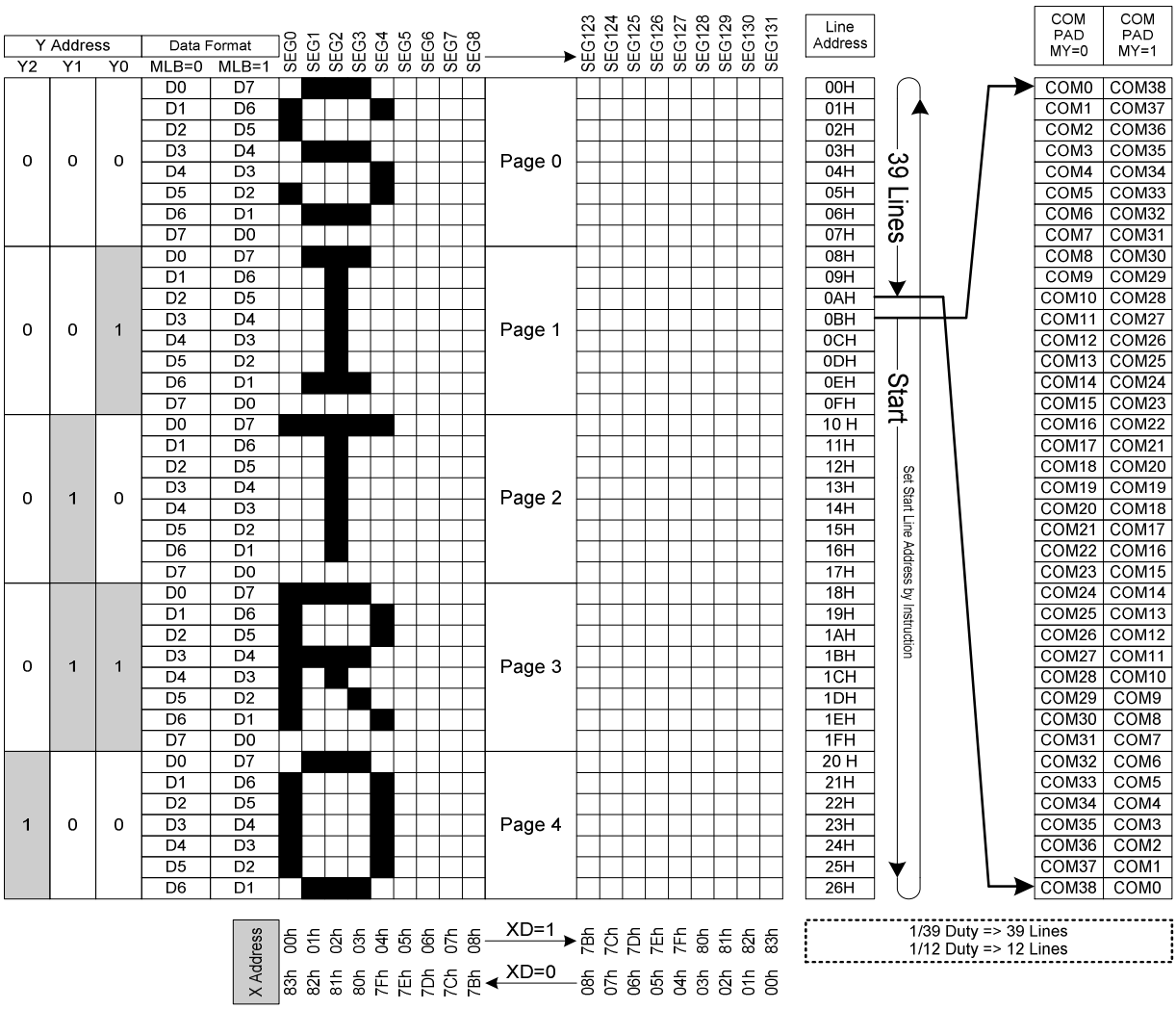
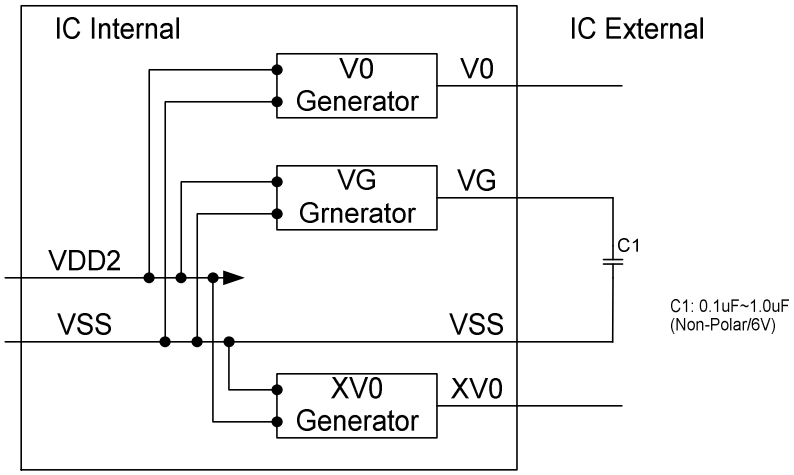


Figure 11 Display Data RAM Map (39 COM)

LCD DRIVER CIRCUIT

ST7577 built-in LCD driver circuit has 132-channel segment drivers and 39-channel common drivers. The LCD panel driving voltage depends on the combination of display data and M signal (frame indicator).

Figure 12 External Power Parts



The referential external component values are listed below (it is determined by the worse condition of 1.4” panel).
C1=0.1uF~1uF (Non-Polar/6V, default 1uF)

Customer applications are not necessary the same as the values listed above. The value can be determined by customer’s LCD module (panel loading and ITO resistance) and application (VDD, V0, bias and etc.).

PARTIAL DISPLAY (SOFTWARE)

The Partial Display function is controlled by software instruction. This feature is only available under 1/39 duty mode (DTY="L"). Although only 26 common outputs are used, the duty of Partial Display is not changed (1/39 Duty). Those unused commons output the non-selected waveform.

There are 3 options for partial display operation: Upper, Middle and Lower (refer to Figure 13~Figure 14).

Figure 15 Partial Display OFF (DA1=0,DA0=0)

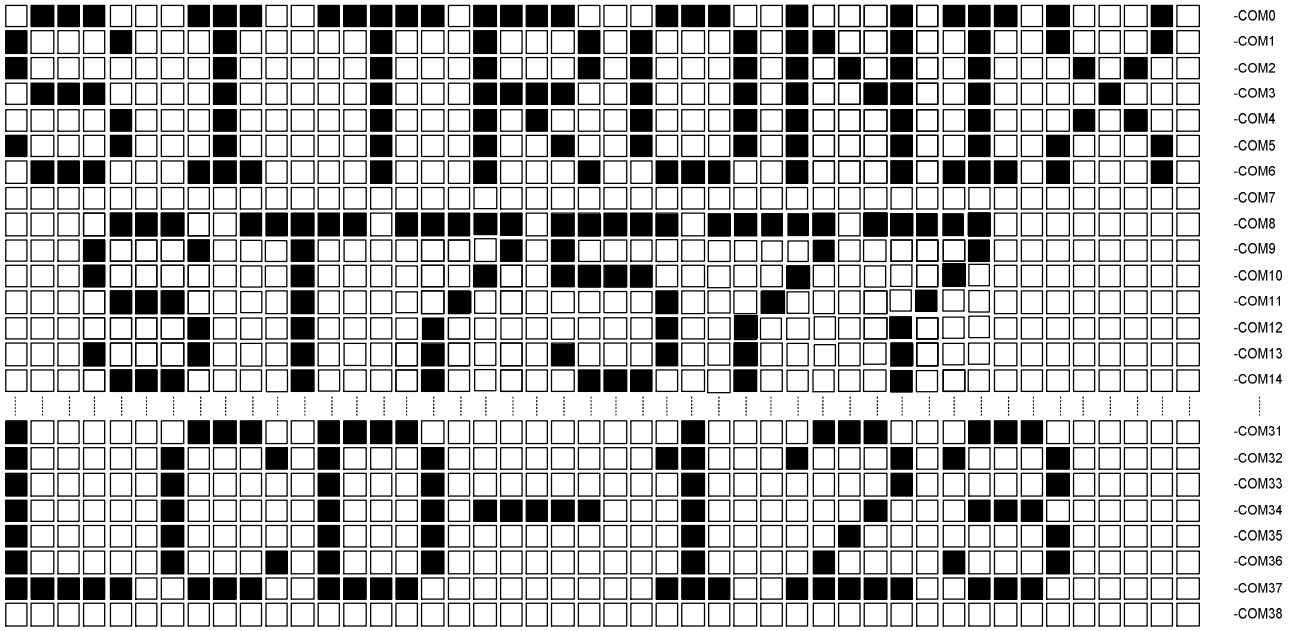


Figure 16 Partial Display: Upper Mode (DA1=0, DA0=1)

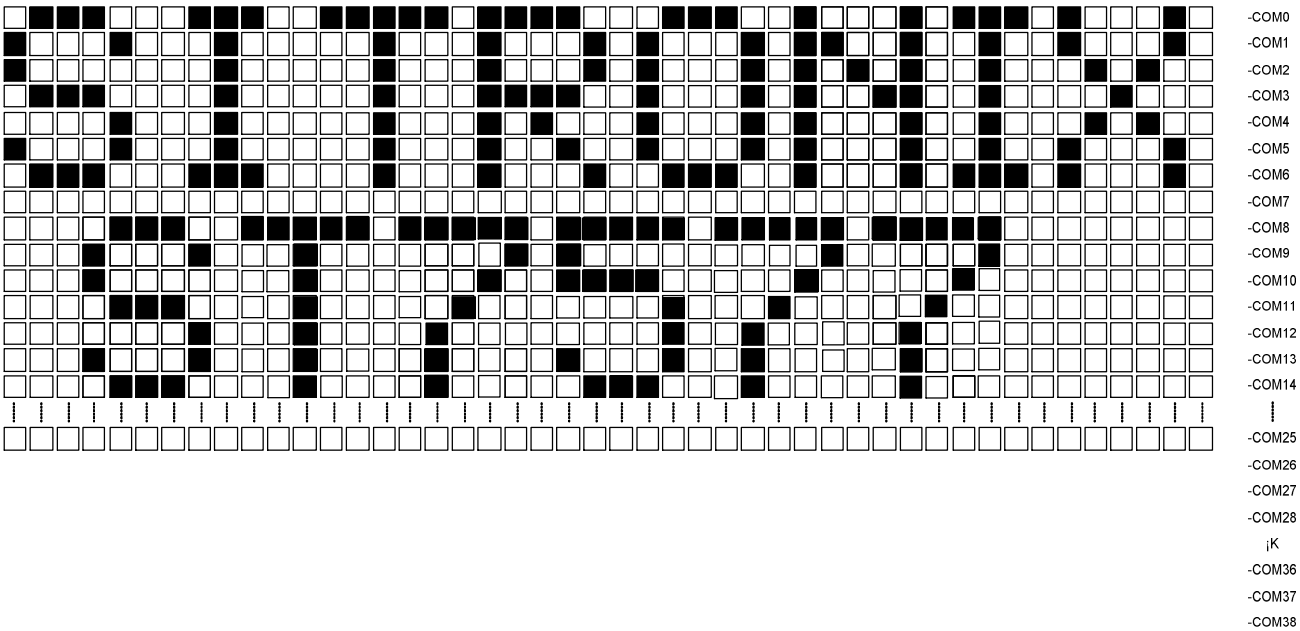


Figure 17 Partial Display: Middle Mode (DA1=1, DA0=0)

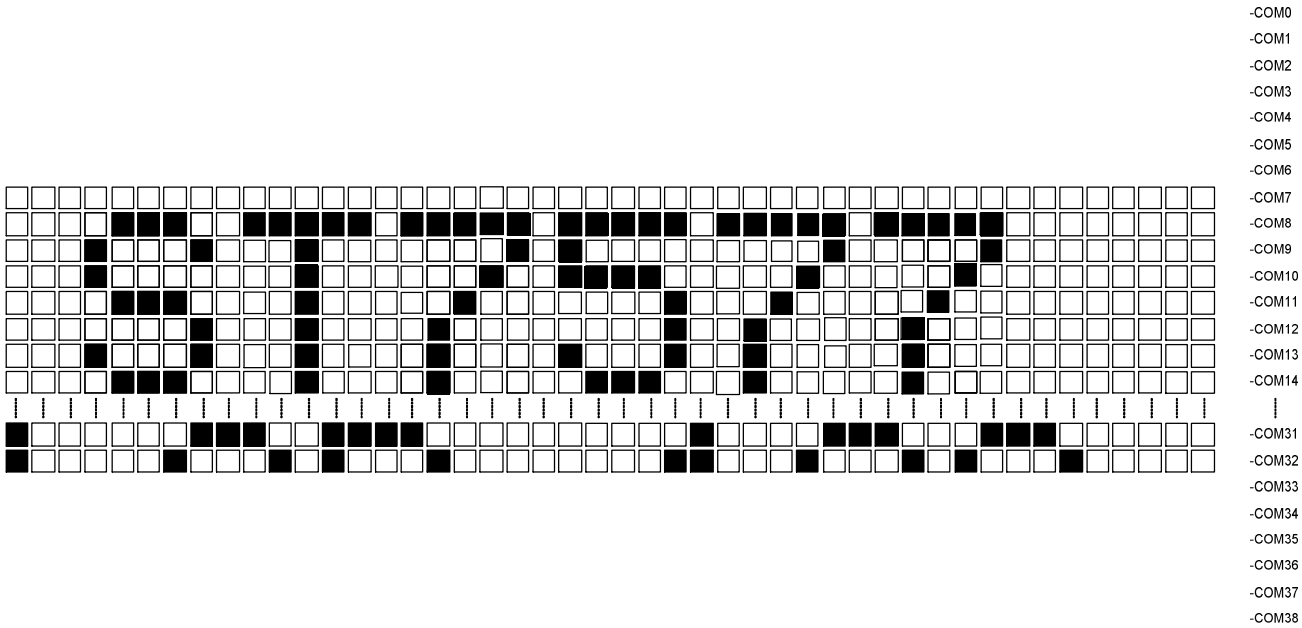
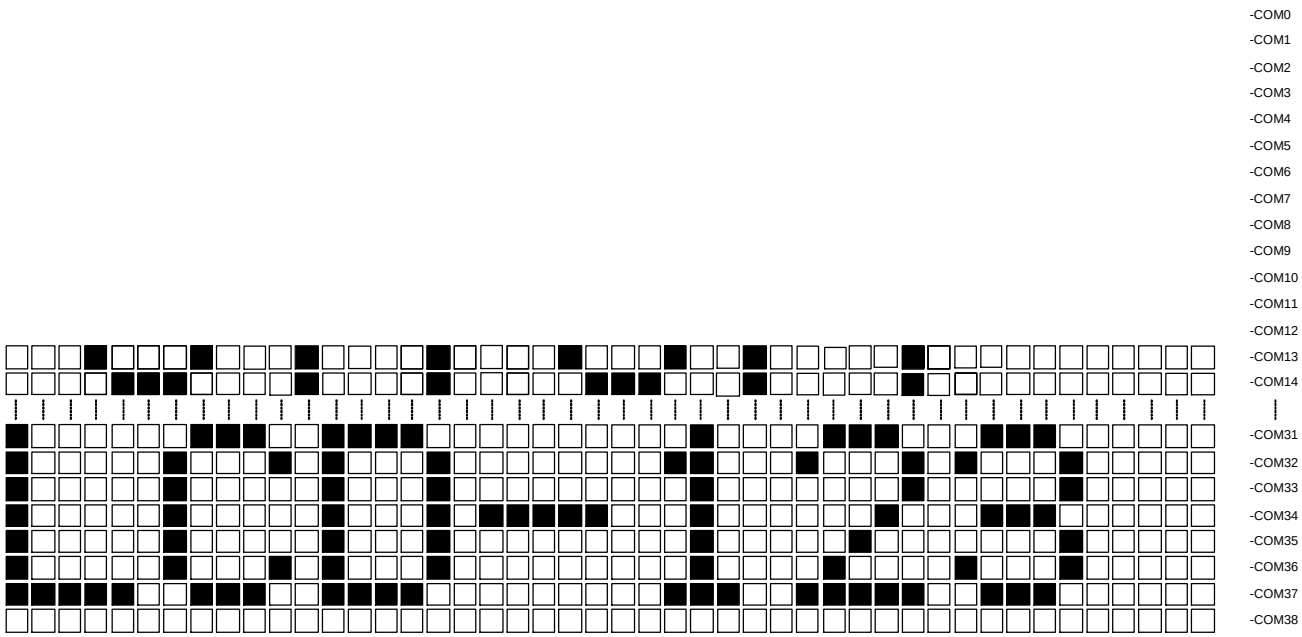


Figure 18 Partial Display: Lower Mode (DA1=1, DA0=1)



8. RESET CIRCUIT

Setting RESB to “L” can initialize internal function. While RESB is “L”, no instruction except read status can be accepted. The initialization by RESB is essential before using.

When RESB becomes “L”, the following procedures will start.
Fix COM/SEG outputs at V_{SS}.
Page address: Y[2:0]=0
Column address: X[7:0]=0
COM Scan Direction MY=0
SEG Select Direction XD=1
Data Format: MLB=MLB pin setting
Power down mode: PD=1
Initial V0 setting: V_{OP}[6:0]=0
Display control: Display Blank: D=E=0
Normal instruction set: H=0
Frame Rate = 73Hz. FR[2:0]=011b
Duty selection: Depends on DTY pin setting.
Booster setting: BE=0, PC[1:0]=01b (Booster Efficiency Level 2, Booster X3)
Bias system: BS[1:0]=[0,0] (1/7 Bias)

After power-on, RAM data are undefined and the Display status is “Blank”. It’s better to initialize whole DDRAM (fill all 00h or write the display pattern) before turning the Display ON.

9. INSTRUCTION TABLE

INSTRUCTION	A0	R/W (/WR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
H=0 or 1 (Independent of H)											
NOP	0	0	0	0	0	0	0	0	0	0	No Operation.
Reset	0	0	0	0	0	0	0	0	0	1	Software Reset
Function Set	0	0	0	0	1	MY	XD	PD	V	H	Scan direction (COM/SEG); Power mode (ON/OFF); Addressing mode; Instruction table selection.
Read Status	0	1	PD	0	D	E	XD	MY	V	MLB	Read status (setting).
Read Data	1	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Read DDRAM data.
Write Data	1	0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Write data into DDRAM.

INSTRUCTION	A0	R/W (/WR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
H=0											
Reserved	0	0	0	0	0	0	0	0	1	X	Do NOT use.
End read-modify-write	0	0	0	0	0	0	0	1	1	0	End Read-Modify-Write
Enable read-modify-write	0	0	0	0	0	0	0	1	1	1	Enable Read-Modify-Write
Display Control	0	0	0	0	0	0	1	D	0	E	Set display configuration.
Frame Rate	0	0	0	0	0	1	0	FR_2	FR_1	FR_0	Frame Rate control
Set Y address of DDRAM	0	0	0	1	0	0	0	Y_2	Y_1	Y_0	Set DDRAM Y address (0≤Y≤4)
Set X address of DDRAM (Low)	0	0	1	0	0	0	X_3	X_2	X_1	X_0	Set DDRAM X address Set the high-nibble first and then low-nibble. (0≤X≤131)
Set X address of DDRAM (High)	0	0	1	0	0	1	X_7	X_6	X_5	X_4	
H=1											
Reserved	0	0	0	0	0	0	0	0	1	X	Do NOT use.
Partial Mode	0	0	0	0	0	0	0	1	DA1	DA0	Set Partial display mode (Display Area)
Booster Control	0	0	0	0	0	0	1	BE	PC1	PC0	Control booster stages and booster efficiency.
BIAS System	0	0	0	0	0	1	0	1	BS1	BS0	Set BIAS system.
Set V0	0	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}	Set V0 voltage to register.
Set Start Line (Vertical-Scroll)	0	0	0	1	S_5	S_4	S_3	S_2	S_1	S_0	Specify the first scan line in the DDRAM.

10. INSTRUCTION DESCRIPTION

Function Set

A0	R/W(/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	MY	XD	PD	V	H

Flag	Description
MY	Set COM scan direction: MY=0: Normal direction (COM0->COM38, duty is determined by the "Display Duty" setting); MY=1: Reverse direction (COM38->COM0, duty is determined by the "Display Duty" setting).
XD	Set DDRAM write direction. XD=1: Write from X=0 to X=131 (Normal direction); XD=0: Write from X=131 to X=0 (Reverse direction).
PD	Set the power mode: PD=0: Chip is active; PD=1: Chip is in power save mode. In power save mode, all LCD outputs at V_{SS}, built-in power circuits (Booster, Regulator and Follower) are turned OFF, Oscillator OFF (external clock is possible), RAM contents is not cleared; RAM data can be written.
V	Select Vertical or Horizontal addressing mode. V=0: Horizontal addressing mode; V=1: Vertical addressing mode.
H	H is used to select the extended instruction set. Please refer to the instruction table.

Read Status

A0	R/W(/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	PD	0	D	E	XD	MY	V	MLB

Flag	Description
PD	PD=0: Chip is active; PD=1: Chip is in power down mode.
D, E	**D** / **E** / **Display Mode** 0 / 0 / Display Blank (DDRAM Data is masked out) 0 / 1 / All Segments ON 1 / 0 / Normal mode 1 / 1 / Inverse Display mode
XD, MY	**XD** / **MY** / **Display Mode** 0 / 0 / Only horizontal direction is mirrored. 0 / 1 / Both horizontal and vertical direction is mirrored. 1 / 0 / Normal direction. 1 / 1 / Only vertical direction is mirrored.
V	Select Vertical or Horizontal addressing mode. V=0: Horizontal addressing mode; V=1: Vertical addressing mode.
MLB	Data Format. MLB=0: LSB on top; MLB=1: MSB on top.

Read Data

Read the specified 8-bit data in DDRAM to the microprocessor. The location is specified by the X-address and Y-address.

A0	R/W(/WR)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	Read Data							

Write Data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

A0	R/W(/WR)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	Read Data							

NOP

No operation.

A0	R/W(/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0

Reset

This is the Software RESET instruction. This is same as hardware reset.

A0	R/W(/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	1

H=0

When Function Set instruction sets H=0, the selected instruction descriptions are as below.

End Read-Modify-Write

This command releases the Read-Modify-Write mode, and returns the column and row address to the address it was at when the mode was entered.

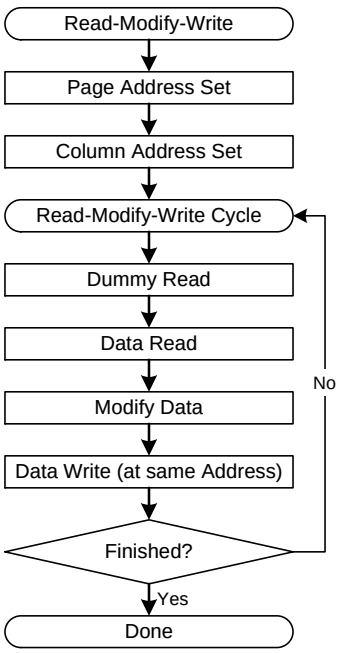
A0	R/W(/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	1	0

Enable Read-Modify-Write

This command is used paired with the ”End Read-Modify-Write” instruction. Once this command has been input, the display data read command does not change the column and row address, but only the display data write command increments (+1) the address depend on V register setting. This mode is maintained until the END command is input. When the END command is input, the address returns to the address it was at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

A0	R/W(/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	1	1

* Even in read/modify/write mode, other commands aside from display data read/write commands can also be used.



Display Control

The bits D and E configure the display mode.

A0	R/W(/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	D	0	E

Flag	Description
D, E	D / E / Display Mode 0 / 0 / Display Blank (DDRAM Data is masked out, segments will always output non-selected waveform) 0 / 1 / All Segments ON 1 / 0 / Normal mode 1 / 1 / Inverse Display mode

Frame Rate

This command is used to select the frame rate.

A0	R/W(/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	FR_2	FR_1	FR_0

The optional Frame Rates are: (no matter 1/39 , or 1/12 duty mode, the frame rate will be controlled in the specified range)

FR_2	FR_1	FR_0	Frame Rate
0	0	0	60 Hz
0	0	1	65 Hz
0	1	0	70 Hz
0	1	1	73 Hz (Default)
1	0	0	76 Hz
1	0	1	80 Hz
1	1	0	85 Hz
1	1	1	90 Hz

Set Y address of DDRAM

Y[2:0] specifies the Y address of the Display Data RAM (DDRAM).

A0	R/W(/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	Y_2	Y_1	Y_0

Y2	Y1	Y0	Addressed Page	Allowed X address	Valid bit (MLB= “H”)
0	0	0	Page0	0 ~ 131	D7~D0
0	0	1	Page1	0 ~ 131	D7~D0
0	1	0	Page2	0 ~ 131	D7~D0
0	1	1	Page3	0 ~ 131	D7~D0
1	0	0	Page4	0 ~ 131	D7~D1

Set X address of DDRAM

Specify the X address to point the columns of the Display Data RAM (DDRAM). The valid range is 0~131.

Set X address of DDRAM (Low)

A0	R/W(/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	X_3	X_2	X_1	X_0

Set X address of DDRAM (High)

A0	R/W(/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	1	X_7	X_6	X_5	X_4

X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Column Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	1	129
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

H=1

When Function Set instruction sets H=1, the selected instruction descriptions are as below.

Partial Mode

This instruction configures the Partial Display mode. Please note that the actual duty is not changed.

A0	R/W(/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	DA1	DA0

Flag	Description
DA[1:0]	Use DA[1:0] to select the display area. The duty is not changed among all these modes.

DA1	DA0	Partial Display Mode
0	0	Full Display (Partial Display Mode OFF).
0	1	Upper Mode (COM0~COM25)
1	0	Middle Mode (COM7~COM32)
1	1	Lower Mode (COM13~COM38)

Booster Control

This instruction configures the built-in voltage booster.

A0	R/W(/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	BE	PC1	PC0

Flag	Description
BE	ST7577 supports software configurable Booster Efficiency. Customers can change the BE and PC[1:0] according to the LCD panel loading and their power consumption requirement. The higher level provides higher driving ability while the power consumption is also higher.

BE	Booster Efficiency Level
0	Booster Efficiency Level 2 (Default)
1	Booster Efficiency Level 1

Flag	Description
PC[1:0]	ST7577 supports software selectable Booster Stage. Customers can change the BE[1:0] and PC[1:0] according to the LCD panel loading and their power consumption requirement. The higher stage generates higher driving ability while the power consumption is also higher.

PC1	PC0	Booster Stage
0	1	Booster X3
1	X	Booster X4

BIAS System

ST7577 is built-in a BIAS-voltage generation system for driving the LCD. The bias can be specified by this instruction.

A0	R/W(/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	1	BS1	BS0

The referential settings of Bias, Duty and V0 are listed below: (assume VDD2=2.8V)

BS1	BS0	BIAS	Recommend Duty
0	0	7	1/39
0	1	6	1/39
1	0	5	1/39, 1/12
1	1	4	1/12

LCD voltage

Symbol	Voltage for 1/5 BIAS
V0	V0
VG	2/5 of V0
VM	1/5 of V0
V_{SS}	V_{SS}

* Be sure the VG is in operable range:
(1.28V ≤ VG ≤ VDD2-0.2V) in any operation condition.

Set V0

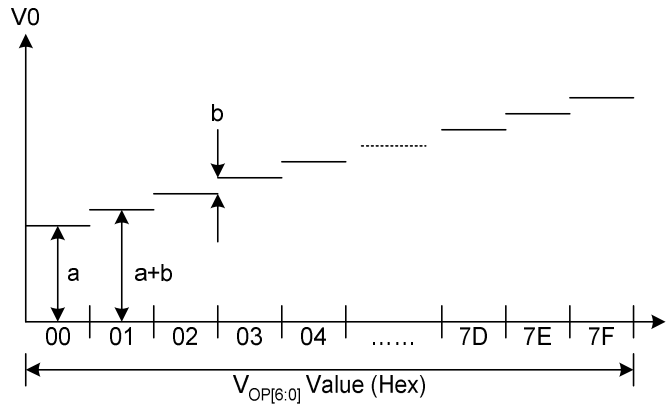
Set V0 voltage level into this register and the built-in voltage regulator will generate the V0.

A0	R/W(/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}

The V0 voltage can be calculated by this formula:

$$V0=(a + V_{OP[6:0]} \times b) \quad \text{.....(1)}$$

Figure 19 V0 voltage vs. $V_{OP[6:0]}$ value



The parameters in this formula are controlled by the hardware pin “PM” (Ta=25°C).

H/W Setting	a	b	Unit
PM=”L”	3.0	0.03	V
PM=”H”	4.5	0.03	V

Set Start Line (Vertical-Scroll)

Sets the line address of display RAM to determine the initial display line instruction. The RAM display data is displayed at the top of row (COM0) of LCD panel.

A0	R/W(/WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	S_5	S_4	S_3	S_2	S_1	S_0

S_5	S_4	S_3	S_2	S_1	S_0	Column address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
:	:	:	:	:	:	:
1	0	0	1	0	0	36
1	0	0	1	0	1	37
1	0	0	1	1	0	38

11. Instruction Sequence

This section introduces some reference instruction flows.

Power ON flow with built-in power circuits:

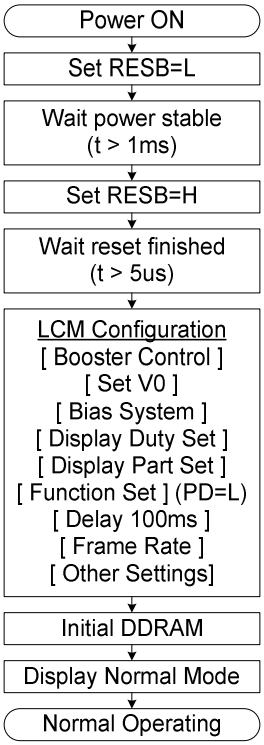
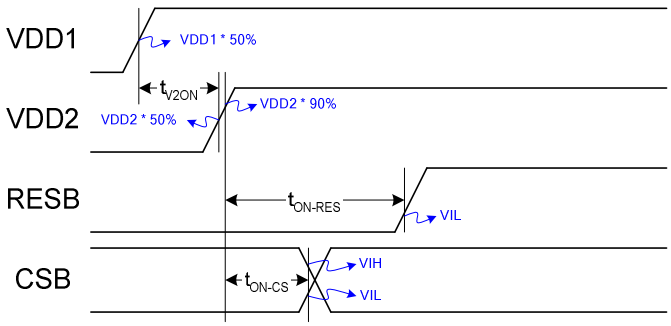


Figure 20 Initial flow with built-in Power Supply Circuits

POWER SEQUENCE

1. t_{V2ON}:
   Period between VDD and VDD2 turned ON.
   => 0 ms (min). No maximum value specified.
2. t_{ON-RES}:
   RESB has priority over CSB.
3. t_{ON-CS}:
   CSB can be input at any time after power is stable.



Power Saving flow with built-in power circuits

ENTERING THE POWER SAVE MODE

The power save mode is achieved by setting PD bit to be “1”. No specified instruction flow required.

EXITING THE POWER SAVE MODE

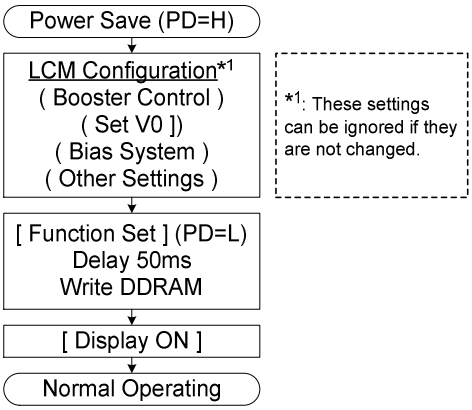
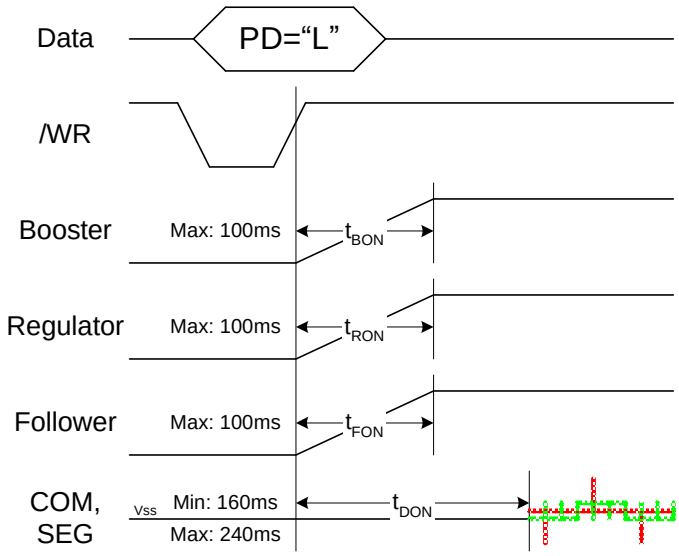


Figure 21 Exiting Power Save Mode

INTERNAL SEQUENCE of EXIT POWER SAVE MODE

After receiving the “PD” is “L”, the internal circuits (Power and COM/SEG) will starts the following procedure.



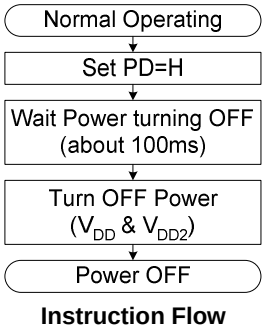
Note:

1. The power stable time is determined by LCD panel loading.
2. The power stable time in this figure is base on: LCD Panel Size = 1.4” with C1=1uF.

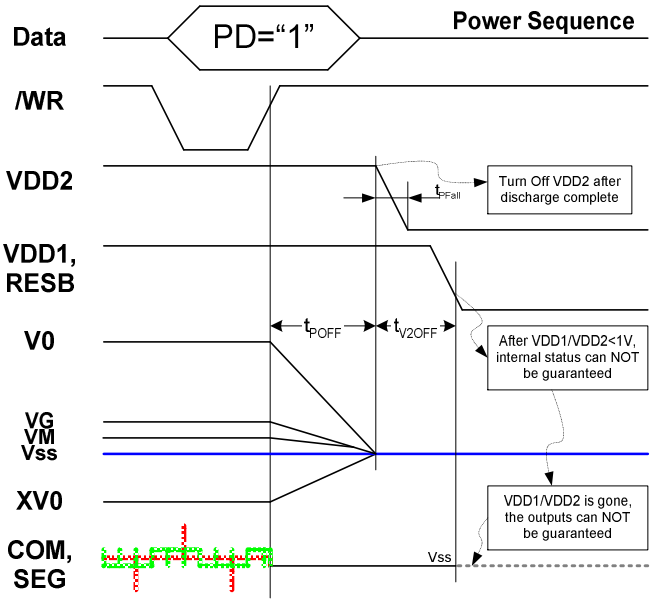
Power OFF flow with built-in power circuits

USING PD BIT

By setting PD="H", ST7577 will go into power save mode. The LCD driving outputs are all fixed to V_{SS} and the built-in power circuits are turned OFF. After the built-in power circuits are turned OFF, the power (V_{DD} and V_{DD2}) can be removed.



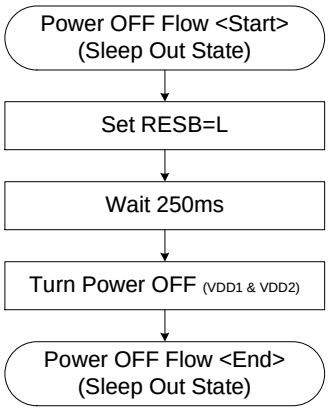
Instruction Flow



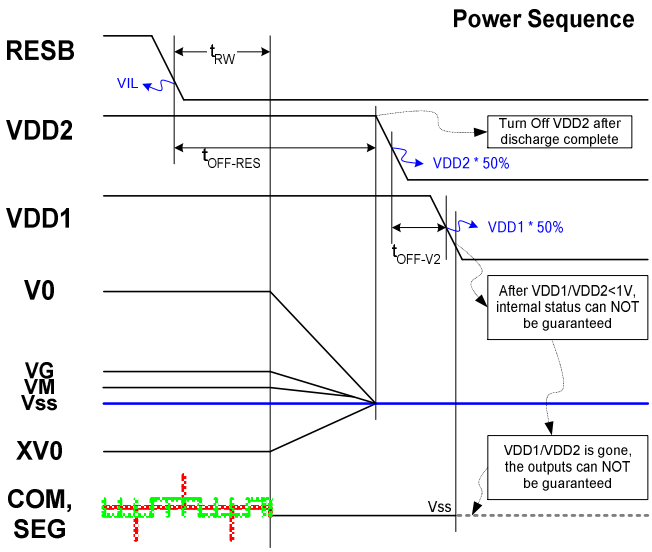
Note:

1. t_{IPOFF}: Internal Power discharge time. => 250ms (max).
2. t_{V2OFF}: Period between VDD and VDD2 OFF time. => 50 ms (max).
3. It is NOT recommended to turn VDD OFF before VDD2. Without VDD, the internal status cannot be guaranteed and internal discharge-process maybe stopped. The un-discharged power maybe polarizes the liquid crystal in panel.
4. IC will NOT be damaged if either VDD or VDD2 is OFF while another is ON.
5. The timing is dependent on panel loading and the external capacitor(s).
6. The timing in these figures is base on the condition that: LCD Panel Size = 1.5" with C1=1uF, C2=1uF.
7. Reset Low time after VDD2 is stable.
8. When turning VDD2 OFF, the falling time should follow the specification:
   300ms ≤ t_{PFall} ≤ 1sec

USING RESB



Instruction Flow



Note:

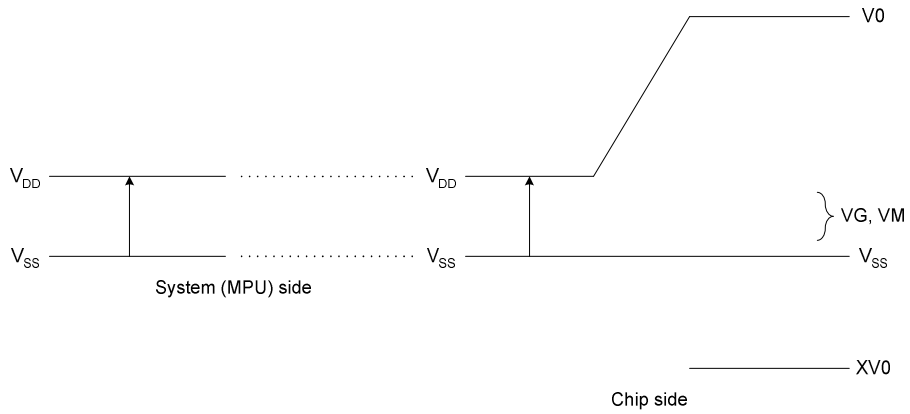
9. $t_{OFF-RES}$: Internal Power discharge time. => 250ms (max).
10. t_{OFF-V2}: Period between VDD and VDD2 OFF time. => 50 ms (max).
11. It is NOT recommended to turn VDD OFF before VDD2. Without VDD, the internal status cannot be guaranteed and internal discharge-process maybe stopped. The un-discharged power maybe polarizes the liquid crystal in panel.
12. IC will NOT be damaged if either VDD or VDD2 is OFF while another is ON.
13. The timing is dependent on panel loading and the external capacitor(s).
14. The timing in these figures is base on the condition that: LCD Panel Size = 1.4” with C1=1uF.

12 Absolutely Maximum Rating

In accordance with the Absolute Maximum Rating values; see notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Digital Power Supply Voltage	V_{DD}	-0.3 ~ 3.6	V
Analog Power supply voltage	V_{DD2}	-0.3 ~ 3.6	V
LCD Driver Power supply voltage	V0-XV0	-0.3 ~ 9.5	V
	VG, VM	-0.3 ~ V_{DD2}+0.3	V
Input voltage	VIN	-0.3 ~ V_{DD}+0.3	V
Operating temperature	TOPR	-30 to +85	°C
Storage temperature	TSTR	-65 to +150	°C

Figure 22 Voltage Range



Notes

1. Stresses over the Absolutely Maximum Rating may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise specified.
3. Make sure the voltage of the following pins follows the relation list below:
   $V0 \geq V_{DD2} \geq VG \geq VM \geq V_{SS} \geq XV0$

13. HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see “Handling MOS devices”).

14. DC CHARACTERISTICS

Unless otherwise specified, V_{DD} = 2.4V to 3.3V; V_{SS} = 0V; Tamb = -30°C to +85°C.

Item		Symbol	Condition		Rating			Unit	Applicable Pin
					Min.	Typ.	Max.		
Power	Operation Voltage (1)	V_{DD}			2.4	—	3.4	V	
	Operating Voltage (2)	V_{DD2}			2.4	—	3.4	V	
	V0-XV0	Vop			3.0	—	9.0	V	V0, XV0
	Internal VG Output	VGO			1.28		V_{DD2}		VGO
High-level Input Voltage		V_{IHC}			0.7 x V_{DD}	—	V_{DD}	V	
Low-level Input Voltage		V_{ILC}			V_{SS}	—	0.3 x V_{DD}	V	
High-level Output Voltage		V_{OHC}	I_{OUT}=-500uA; V_{DD}=2.4V		0.8 x V_{DD}	—	V_{DD}	V	
Low-level Output Voltage		V_{OLC}	I_{OUT}=500uA; V_{DD}=2.4V		V_{SS}	—	0.2 x V_{DD}	V	
Input leakage current		I_{LI}			-1.0	—	1.0	μA	
Output leakage current		I_{LO}			-3.0	—	3.0	μA	
Liquid Crystal Driver ON Resistance		R_{ON}	Ta = 25°C ΔV=10%	V0 = 6.0 V	—	0.8	—	KΩ	COMn
				VG = 2.4 V	—	0.8	—		SEGn
Frame Rate		FR	FR[2:0]=011b		65.7	73	80.3	Hz	

Dynamic Current Consumption: During Display, with Internal Power Supply ON, current consumed by whole chip (bare die)

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern SNOW	I_{SS}	V_{DD} = V_{DD2} = 2.8V, Frame Rate = 73Hz; Booster X4; V0 = 6.9 V; Bias=1/7; 1/39 Duty	—	85	—	μA	
Power Down	I_{SS}	V_{DD} = V_{DD2} = 2.8V, Ta = 25°C	—	0.5	10	μA	

Notes to the DC characteristics

1. The maximum V0 voltage may be generated will be limited by V_{DD2} , temperature and panel loading.
2. Power Down: During power down mode, all static currents are switched off.

15. TIMING CHARACTERISTICS

System Bus Read/Write Characteristics (For the 8080 Series MPU)

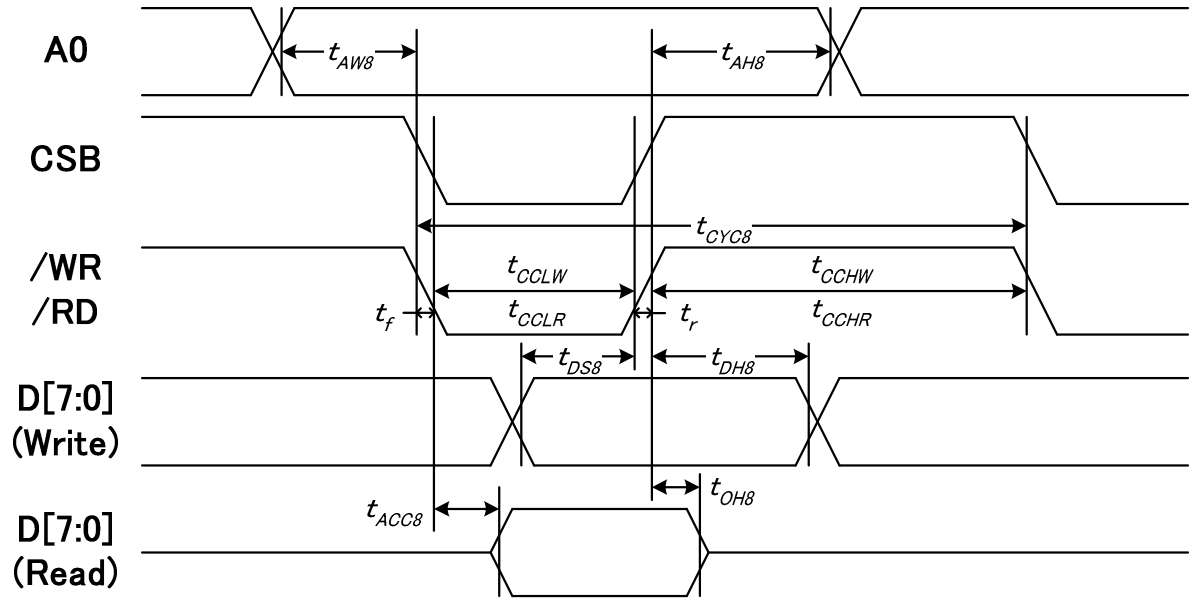


Figure 23

V_{DD} = 2.4~3.3V

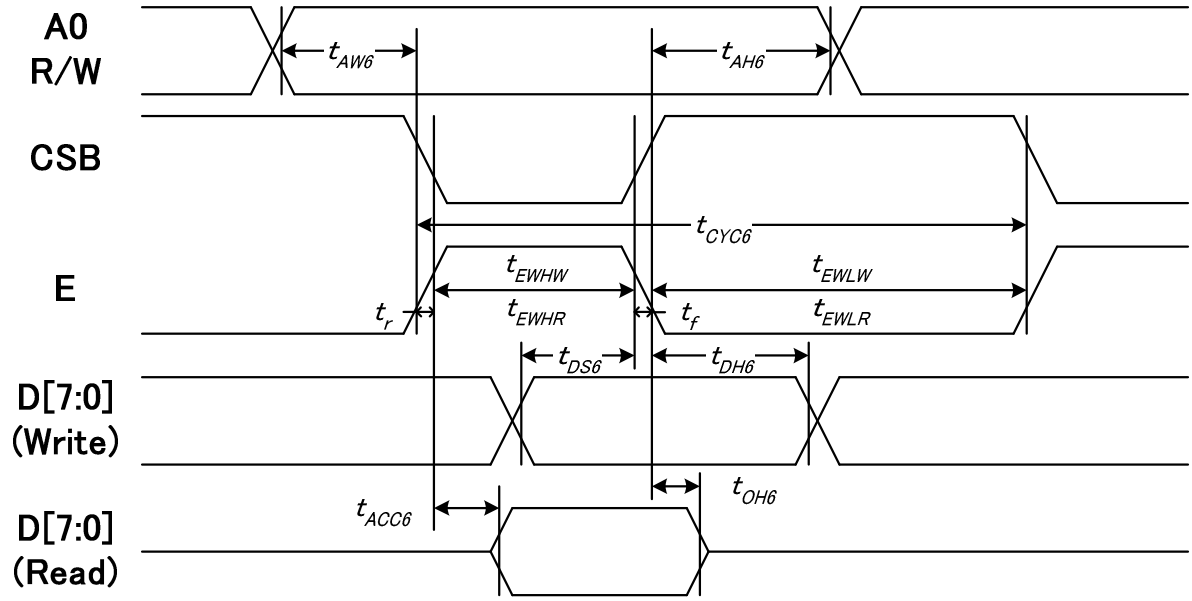
Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Address setup time	A0	t_{AW8}		15			ns
Address hold time		t_{AH8}		10			
System cycle time		t_{CYC8}		150			
/WR low pulse width	/WR	t_{CCLW}		80			
/WR high pulse width		t_{CCHW}		70			
/RD low pulse width	/RD	t_{CCLR}		243			
/RD high pulse width		t_{CCHR}		70			
WRITE Data setup time	D0 ~ D7	t_{DS8}		30			
WRITE Data hold time		t_{DH8}		35			
READ access time		t_{ACC8}		30		243	
READ output disable time		t_{OH8}				70	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.

*2 All timing is specified using 20% and 80% of V_{DD} as the reference.

*3 tCCLW and tCCLR are specified as the overlap between CSB being “L” and WR and RD being at the “L” level.

System Bus Read/Write Characteristics (For the 6800 Series MPU)



V_{DD} = 2.4~3.3V

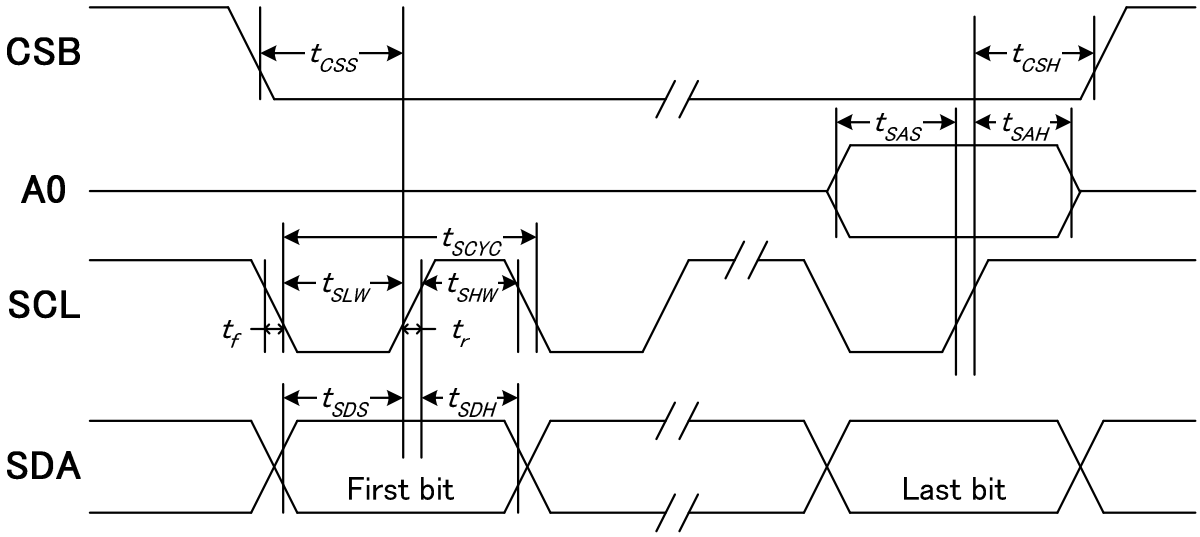
Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Address setup time	A0	t_{AW6}		45			ns
Address hold time		t_{AH6}		10			
System cycle time		t_{CYC6}		130			
Enable L pulse width (WRITE)	E/RD	t_{EWLW}		50			
Enable H pulse width (WRITE)		t_{EWHW}		80			
Enable L pulse width (READ)	E/RD	t_{EWLR}		245			
Enable H pulse width (READ)		t_{EWHR}		40			
WRITE Data setup time	D0 ~ D7	t_{DS6}		45			
WRITE Data hold time		t_{DH6}		45			
READ access time		t_{ACC6}		15		245	
READ output disable time		t_{OH6}				45	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≦ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≦ (tCYC6 – tEWLR – tEWHR) are specified.

*2 All timing is specified using 20% and 80% of V_{DD} as the reference.

*3 tEWLW and tEWLR are specified as the overlap between CSB being “L” and E.

Serial Interface (4-Line Interface)



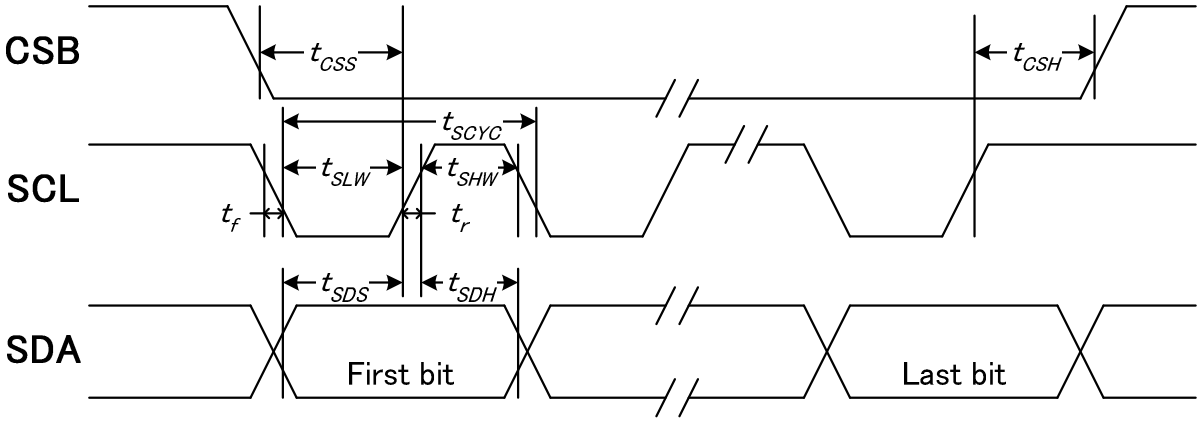
V_{DD} = 2.4~3.3V

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Serial Clock Period	SCL	t_{SCYC}		330			ns
SCL “H” pulse width		t_{SHW}		165			
SCL “L” pulse width		t_{SLW}		165			
Address setup time	A0	t_{SAS}		10			
Address hold time		t_{SAH}		60			
Data setup time	SI	t_{SDS}		10			
Data hold time		t_{SDH}		40			
CS-SCL time	CSB	t_{CSS}		10			
CS-SCL time		t_{CSH}		110			

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of V_{DD} as the standard.

Serial Interface (3-Line Interface)



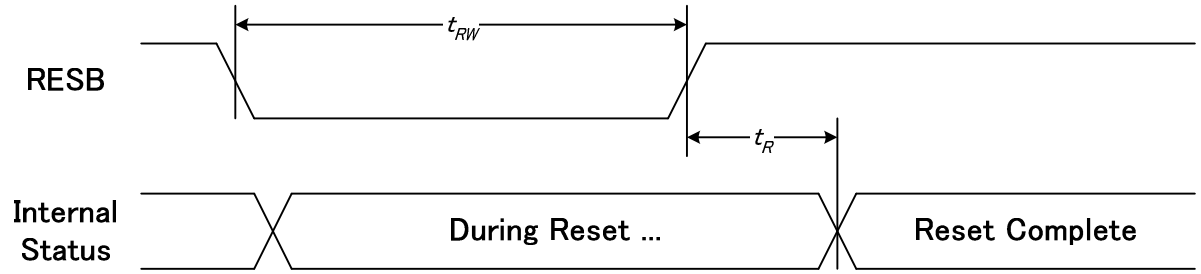
V_{DD} = 2.4~3.3V

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Serial Clock Period	SCL	t_{SCYC}		330			ns
SCL “H” pulse width		t_{SHW}		165			
SCL “L” pulse width		t_{SLW}		165			
Data setup time	SI	t_{SDS}		20			
Data hold time		t_{SDH}		30			
CS-SCL time	CSB	t_{CSS}		10			
CS-SCL time		t_{CSH}		120			

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of V_{DD} as the standard.

Reset Timing



V_{DD} = 2.4~3.3V

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R				2.0	μs
Reset "L" pulse width	RESB	t_{RW}		2.0			μs

16. APPLICATION NOTE

Selection of Application Voltage

Power Range Summary

- Positive Booster: (VDD2 x PCn x BE) ≥ V0 or (VDD2 x PCn x BE) ≥ Vop;
- Negative Booster: [-VDD2 x (PCn - 1) x BE] ≤ XV0 or [VDD2 x (PCn -1) x BE] ≥ (Vop-VG), where VG = Vop x 2 / N;
- Vop requirement: [VDD2 x (PCn - 1) x BE] ≥ [Vop x (N-2) / N] or Vop ≤ VDD2 x (PCn -1) x BE x N / (N-2).
- PCn is the booster stage and BE is the booster efficiency. Referential values are listed below: (assume VDD2=2.8V)
  Module Size ≤ 1.4": BE=80% (min);
  Module Size = 1.4"~1.8": BE = 76% (min).
  Actual BE should be determined by module loading and ITO resistance value.
- 1.28 ≤ VG ≤ VDD2-0.2V. Recommend VG is: VDD2-VG around 0.5~0.8V.
- VM=VG/2 and 0.64V ≤ VM < VDD2.
- The worse condition should be considered:
  Low temperature effect and display on with snow pattern on panel (max: 1.4").

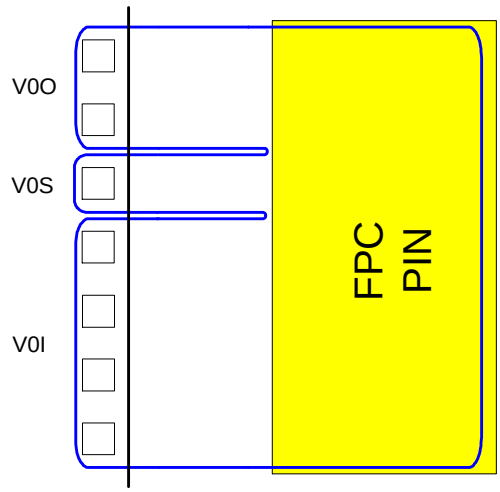
According to the Duty Size, the Recommend BIAS, Vop Range and Booster are listed below:

VDD2=2.8V

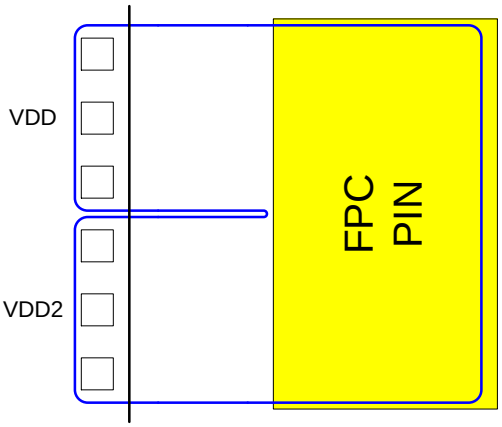
Duty	Recommend BIAS	Recommend Vop Range	Recommend Booster
39	1/7	6.5 ~ 7.5	X4
12	1/4	3.5 ~ 4.5	X3, X4
	1/5	4.5 ~ 5.5	X3, X4

- The V0 range Tables are base on: LCD Panel Size = 1.4" with C1=1uF.
- The actual V0 range depends on the Panel Size, Temperature Effect and Display Pattern.

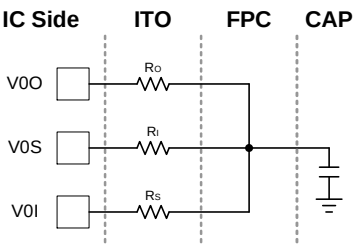
ITO Layout Reference (for Power)



Power Circuit Input, Output and Sensor ITO Layout
(for V0, XV0 and VG ITO layout)



Digital / Analog Power ITO Layout (Using Single Power)



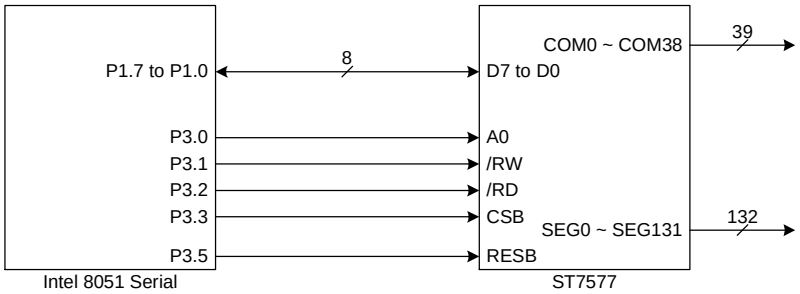
Equivalent Circuit

Note:

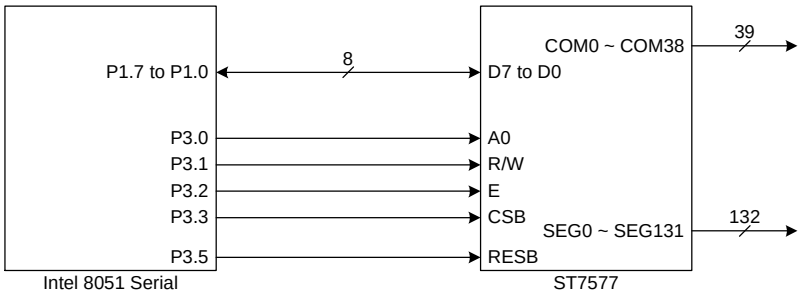
1. Total resistance value of VSS should be smaller than "VDD//VDD2".
2. Recommend ITO resistance value:
   $R_I \leq 150$ Ohm; $R_O \leq 200$ Ohm; $R_S \leq 250$ Ohm.
3. The relationship among input, output and sensor ITO(for V0, XV0 and VG) resistance value is $R_S > R_O > R_I$.

MPU Interface

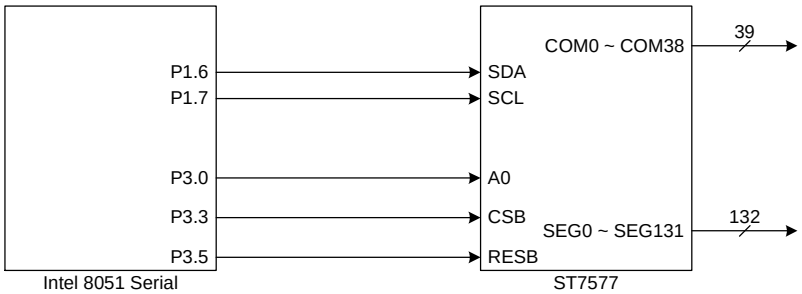
- Intel 8080 series MPU Interface (8-bit):



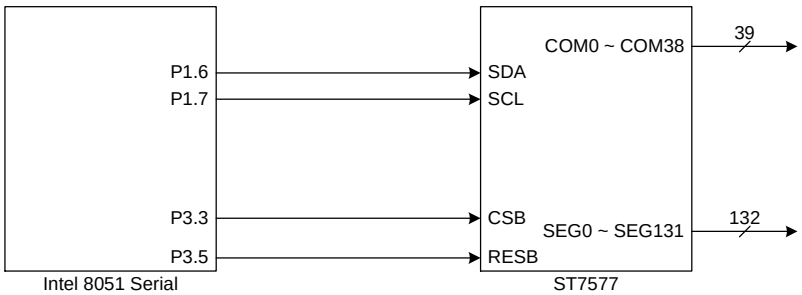
- Motorola 6800 series MPU Interface (8-bit):



- Serial 4-Line SPI Mode:



- Serial 3-Line SPI Mode:

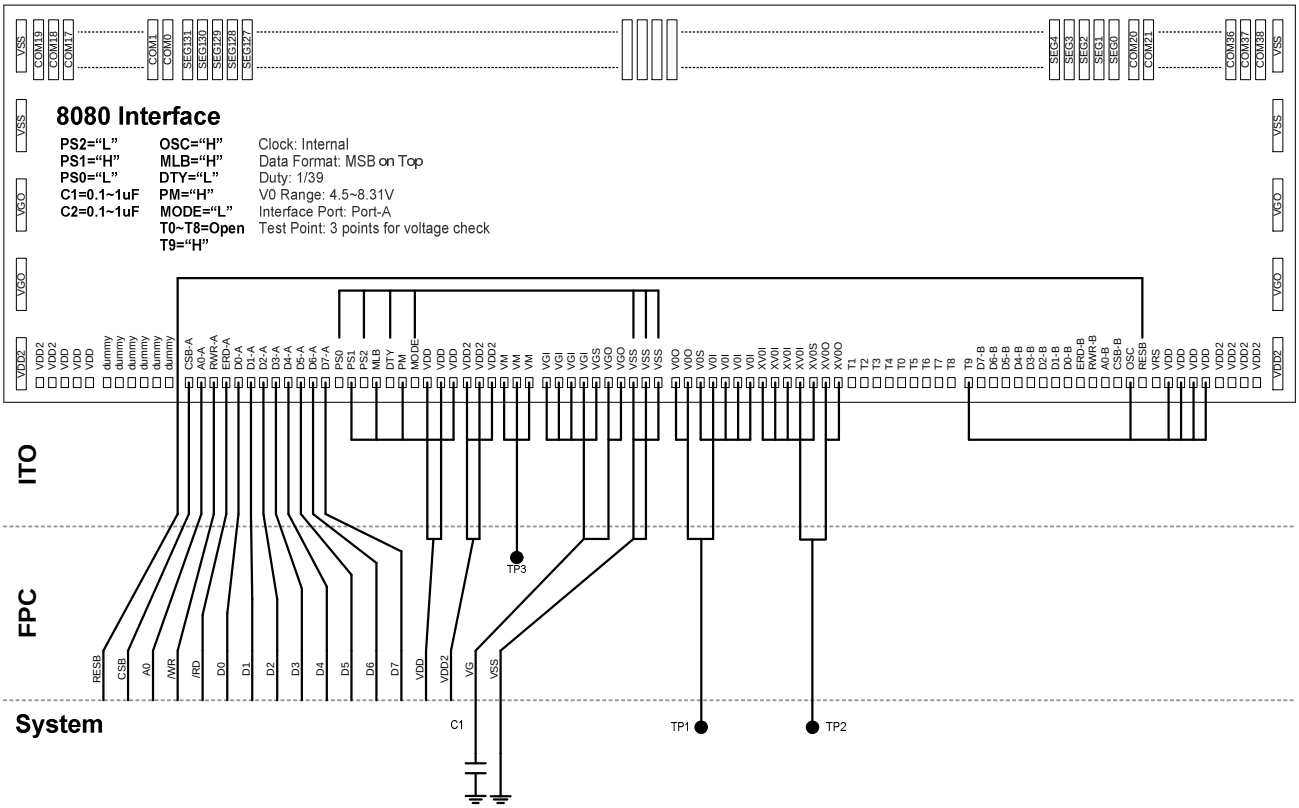


Note:

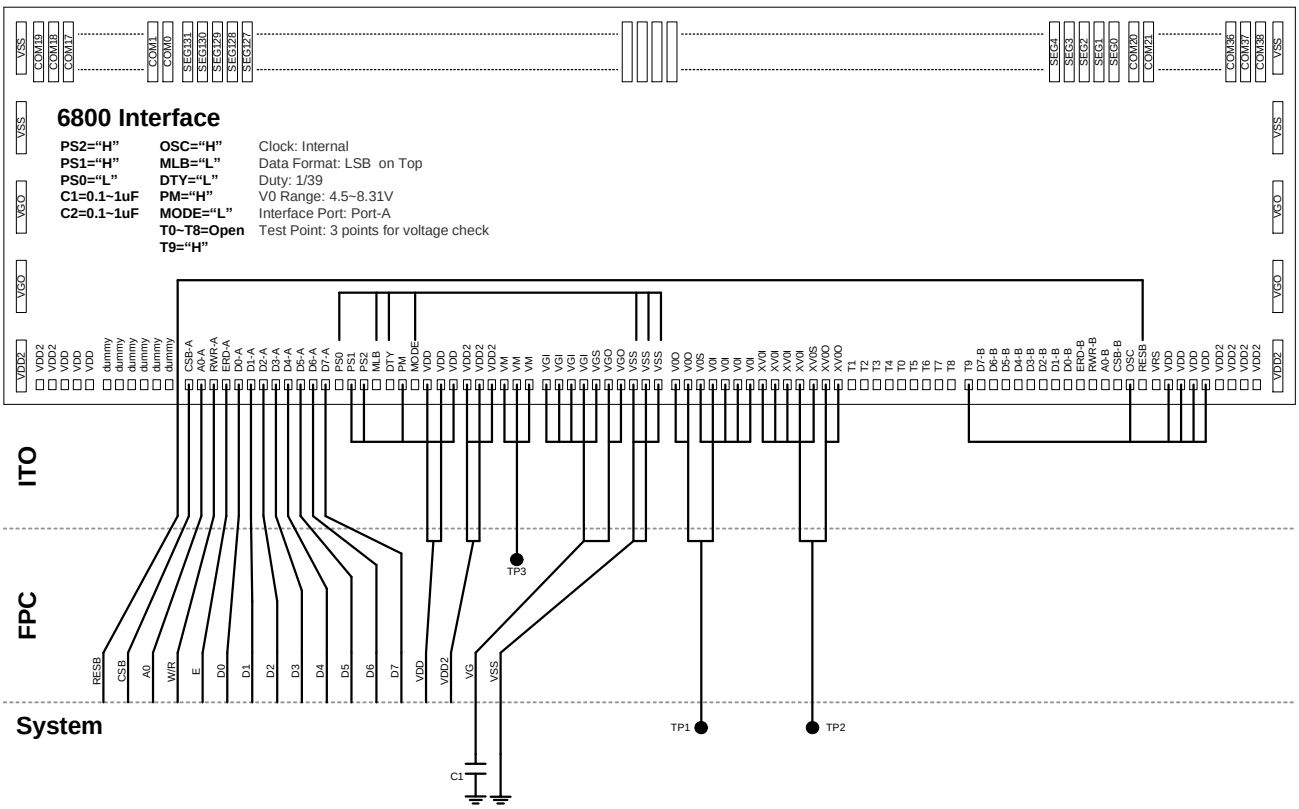
- The Microprocessor Interface pins should not be left floating under any operation mode.

Application Circuits

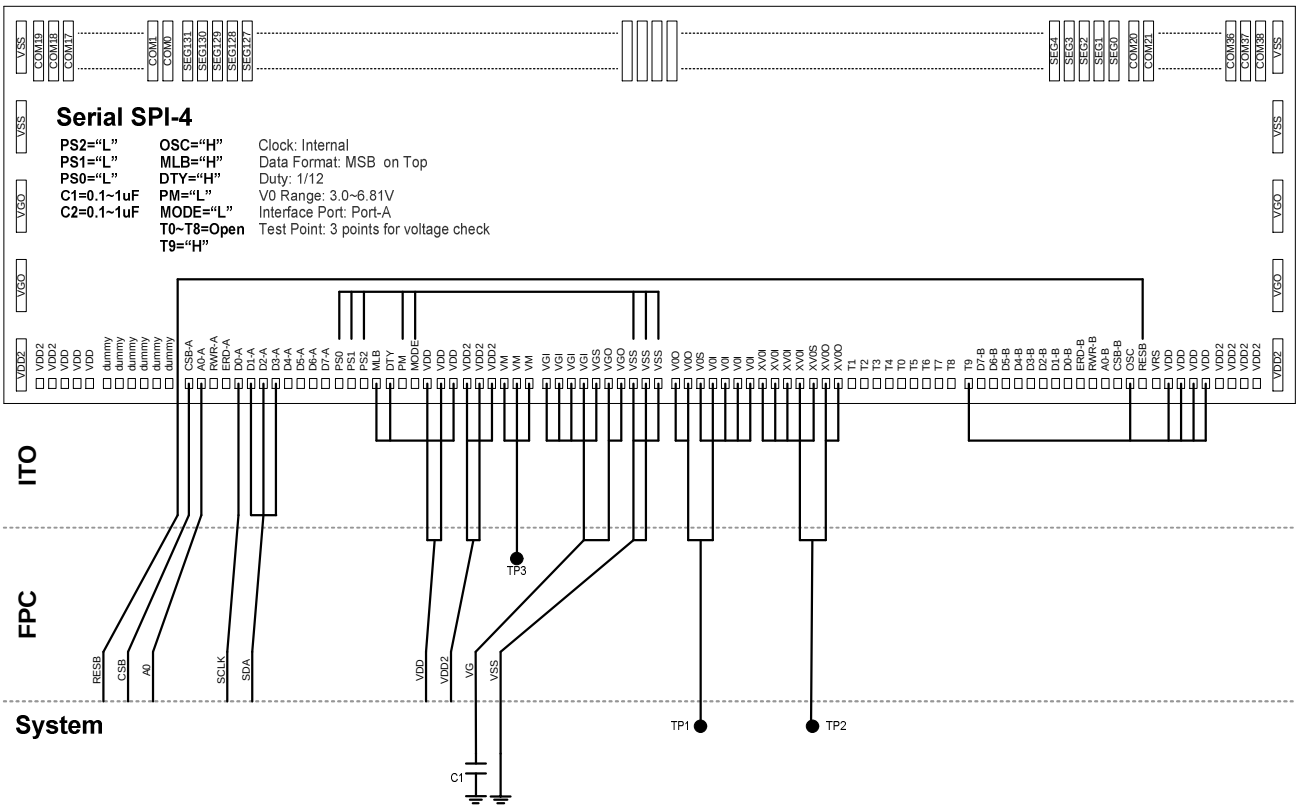
8080 Interface (Port-A)



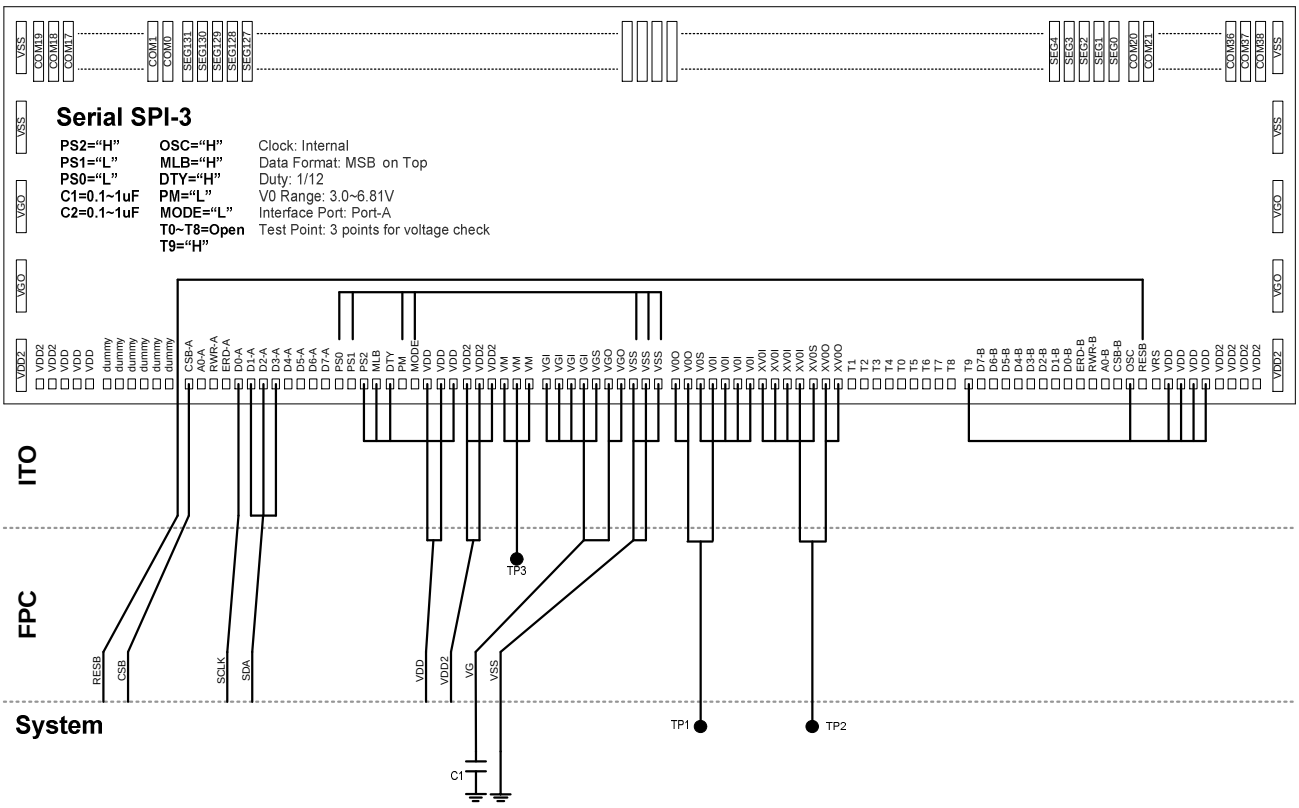
6800 Interface (Port-A)



Serial 4-Line SPI (Port-A)



Serial 3-Line SPI (Port-A)



Notes for all applications:

- Recommend short noisy nets by FPC (refer to Page 43, ITO Layout).
- The Microprocessor Interface pins should not be left floating under any operation mode.

Reversion History

Version	Description	Date
0.0	▪ Initial version	2007/04/24
0.1	▪ Modify Fig 12 ▪ Modify application circuit.	2007/07/24
1.0	▪ Modify external power part. ▪ Modify Power ON and OFF flow. ▪ Modify application circuit. ▪ Update reference timing.	2007/11/13
1.0a	▪ Update date	2008/02/14