Sitronix

ST7571

4 Gray Scale Dot Matrix LCD Controller/Driver

1. INTRODUCTION

ST7571 is a driver & controller LSI for 4-level gray scale graphic dot-matrix liquid crystal display systems. This chip is connected directly to a microprocessor, accepts Serial Peripheral Interface (SPI), I^2C or 8-bit parallel display data and stores in an on-chip display data RAM of 128 x 129 x 2 bits. It performs display data RAM write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

4-level (White, Light Gray, Dark Gray, Black) Gray Scale Display with PWM Method

DDRAM Data [2n : 2n+1]		Gray Scale
2n	2n + 1	
0	0	White
0	1	Light gray
1	0	Dark gray
1	1	Black

(Accessible column address, n = 0, 1, 2, ……, 125, 126, 127)

Driver Output Circuits

- 128 segment outputs / 128+1 common outputs

Applicable Duty Ratios

- Various partial display
- Partial window moving & data scrolling

On-chip Display Data RAM

- Capacity: 128 x 129 x 2= 33,024 bits

Microprocessor Interface

- 8-bit parallel interface supports 6800-series or 8080-series MCU
- 4-line serial interface (4-Line SPI)
- 3-line serial interface (3-Line 8-bit SPI)
- I^2C serial interface

On-chip Low Power Analog Circuits

- On-chip oscillator circuit
- Build-in Voltage converter (x8)
- Voltage regulator (temperature gradient: -0.13%/°C)
- On-chip contrast control function (64 steps x 8)
- Voltage follower (LCD bias : 1/5 to 1/12)

Operating Voltage Range

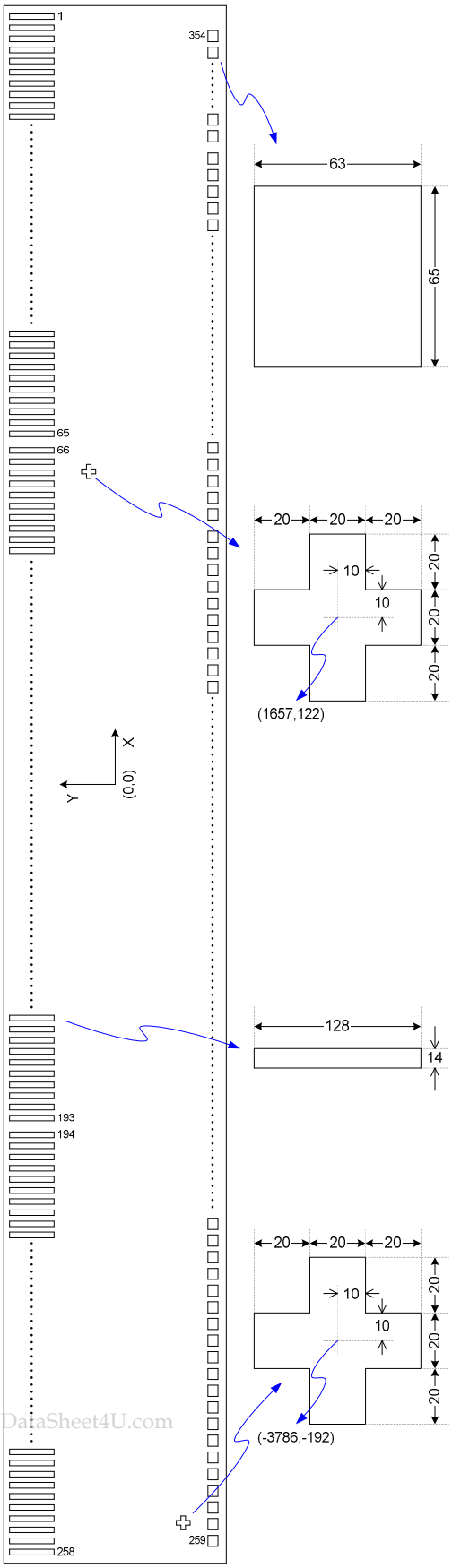
- Digital Power (VDD1): 1.8V~3.3V (cover 1.7V~3.4V)
- Analog Power (VDD2, VDD3): 2.7V~3.3V (cover 2.6V~3.4V)

Package Type

- Application for COG

ST7571	**6800 , 8080 , 4-Line , 3-Line interface (without I^2C interface)**	ST
ST7571i	**I^2C interface**	I^2C BUS

3. PAD ARRANGEMENT (COG)



- Chip Size : 7956um X 780um
- Bump Pitch :
  I/O PAD : 80um
  COM PAD : 33um
  SEG PAD : 27um
- Bump Size :
  I/O PAD : 65um X 63 um
  COM/SEG PAD : 14um X 128um
- Bump Height : 15um
- Chip Thickness : 300 um

Fig. 1 IC Pad Arrangement

4. PAD CENTER COORDINATES

PAD No.	Pin Name	X	Y
1	COM[126]	3896.50	283.00
2	COM[124]	3863.50	283.00
3	COM[122]	3830.50	283.00
4	COM[120]	3797.50	283.00
5	COM[118]	3764.50	283.00
6	COM[116]	3731.50	283.00
7	COM[114]	3698.50	283.00
8	COM[112]	3665.50	283.00
9	COM[110]	3632.50	283.00
10	COM[108]	3599.50	283.00
11	COM[106]	3566.50	283.00
12	COM[104]	3533.50	283.00
13	COM[102]	3500.50	283.00
14	COM[100]	3467.50	283.00
15	COM[98]	3434.50	283.00
16	COM[96]	3401.50	283.00
17	COM[94]	3368.50	283.00
18	COM[92]	3335.50	283.00
19	COM[90]	3302.50	283.00
20	COM[88]	3269.50	283.00
21	COM[86]	3236.50	283.00
22	COM[84]	3203.50	283.00
23	COM[82]	3170.50	283.00
24	COM[80]	3137.50	283.00
25	COM[78]	3104.50	283.00
26	COM[76]	3071.50	283.00
27	COM[74]	3038.50	283.00
28	COM[72]	3005.50	283.00
29	COM[70]	2972.50	283.00
30	COM[68]	2939.50	283.00
31	COM[66]	2906.50	283.00
32	COM[64]	2873.50	283.00
33	COM[62]	2840.50	283.00
34	COM[60]	2807.50	283.00
35	COM[58]	2774.50	283.00

PAD No.	Pin Name	X	Y
36	COM[56]	2741.50	283.00
37	COM[54]	2708.50	283.00
38	COM[52]	2675.50	283.00
39	COM[50]	2642.50	283.00
40	COM[48]	2609.50	283.00
41	COM[46]	2576.50	283.00
42	COM[44]	2543.50	283.00
43	COM[42]	2510.50	283.00
44	COM[40]	2477.50	283.00
45	COM[38]	2444.50	283.00
46	COM[36]	2411.50	283.00
47	COM[34]	2378.50	283.00
48	COM[32]	2345.50	283.00
49	COM[30]	2312.50	283.00
50	COM[28]	2279.50	283.00
51	COM[26]	2246.50	283.00
52	COM[24]	2213.50	283.00
53	COM[22]	2180.50	283.00
54	COM[20]	2147.50	283.00
55	COM[18]	2114.50	283.00
56	COM[16]	2081.50	283.00
57	COM[14]	2048.50	283.00
58	COM[12]	2015.50	283.00
59	COM[10]	1982.50	283.00
60	COM[8]	1949.50	283.00
61	COM[6]	1916.50	283.00
62	COM[4]	1883.50	283.00
63	COM[2]	1850.50	283.00
64	COM[0]	1817.50	283.00
65	COMS1	1784.50	283.00
66	SEG[0]	1714.50	283.00
67	SEG[1]	1687.50	283.00
68	SEG[2]	1660.50	283.00
69	SEG[3]	1633.50	283.00
70	SEG[4]	1606.50	283.00

PAD No.	Pin Name	X	Y
71	SEG[5]	1579.50	283.00
72	SEG[6]	1552.50	283.00
73	SEG[7]	1525.50	283.00
74	SEG[8]	1498.50	283.00
75	SEG[9]	1471.50	283.00
76	SEG[10]	1444.50	283.00
77	SEG[11]	1417.50	283.00
78	SEG[12]	1390.50	283.00
79	SEG[13]	1363.50	283.00
80	SEG[14]	1336.50	283.00
81	SEG[15]	1309.50	283.00
82	SEG[16]	1282.50	283.00
83	SEG[17]	1255.50	283.00
84	SEG[18]	1228.50	283.00
85	SEG[19]	1201.50	283.00
86	SEG[20]	1174.50	283.00
87	SEG[21]	1147.50	283.00
88	SEG[22]	1120.50	283.00
89	SEG[23]	1093.50	283.00
90	SEG[24]	1066.50	283.00
91	SEG[25]	1039.50	283.00
92	SEG[26]	1012.50	283.00
93	SEG[27]	985.50	283.00
94	SEG[28]	958.50	283.00
95	SEG[29]	931.50	283.00
96	SEG[30]	904.50	283.00
97	SEG[31]	877.50	283.00
98	SEG[32]	850.50	283.00
99	SEG[33]	823.50	283.00
100	SEG[34]	796.50	283.00
101	SEG[35]	769.50	283.00
102	SEG[36]	742.50	283.00
103	SEG[37]	715.50	283.00
104	SEG[38]	688.50	283.00
105	SEG[39]	661.50	283.00

PAD No.	Pin Name	X	Y
106	SEG[40]	634.50	283.00
107	SEG[41]	607.50	283.00
108	SEG[42]	580.50	283.00
109	SEG[43]	553.50	283.00
110	SEG[44]	526.50	283.00
111	SEG[45]	499.50	283.00
112	SEG[46]	472.50	283.00
113	SEG[47]	445.50	283.00
114	SEG[48]	418.50	283.00
115	SEG[49]	391.50	283.00
116	SEG[50]	364.50	283.00
117	SEG[51]	337.50	283.00
118	SEG[52]	310.50	283.00
119	SEG[53]	283.50	283.00
120	SEG[54]	256.50	283.00
121	SEG[55]	229.50	283.00
122	SEG[56]	202.50	283.00
123	SEG[57]	175.50	283.00
124	SEG[58]	148.50	283.00
125	SEG[59]	121.50	283.00
126	SEG[60]	94.50	283.00
127	SEG[61]	67.50	283.00
128	SEG[62]	40.50	283.00
129	SEG[63]	13.50	283.00
130	SEG[64]	-13.50	283.00
131	SEG[65]	-40.50	283.00
132	SEG[66]	-67.50	283.00
133	SEG[67]	-94.50	283.00
134	SEG[68]	-121.50	283.00
135	SEG[69]	-148.50	283.00
136	SEG[70]	-175.50	283.00
137	SEG[71]	-202.50	283.00
138	SEG[72]	-229.50	283.00
139	SEG[73]	-256.50	283.00
140	SEG[74]	-283.50	283.00

PAD No.	Pin Name	X	Y
141	SEG[75]	-310.50	283.00
142	SEG[76]	-337.50	283.00
143	SEG[77]	-364.50	283.00
144	SEG[78]	-391.50	283.00
145	SEG[79]	-418.50	283.00
146	SEG[80]	-445.50	283.00
147	SEG[81]	-472.50	283.00
148	SEG[82]	-499.50	283.00
149	SEG[83]	-526.50	283.00
150	SEG[84]	-553.50	283.00
151	SEG[85]	-580.50	283.00
152	SEG[86]	-607.50	283.00
153	SEG[87]	-634.50	283.00
154	SEG[88]	-661.50	283.00
155	SEG[89]	-688.50	283.00
156	SEG[90]	-715.50	283.00
157	SEG[91]	-742.50	283.00
158	SEG[92]	-769.50	283.00
159	SEG[93]	-796.50	283.00
160	SEG[94]	-823.50	283.00
161	SEG[95]	-850.50	283.00
162	SEG[96]	-877.50	283.00
163	SEG[97]	-904.50	283.00
164	SEG[98]	-931.50	283.00
165	SEG[99]	-958.50	283.00
166	SEG[100]	-985.50	283.00
167	SEG[101]	-1012.50	283.00
168	SEG[102]	-1039.50	283.00
169	SEG[103]	-1066.50	283.00
170	SEG[104]	-1093.50	283.00
171	SEG[105]	-1120.50	283.00
172	SEG[106]	-1147.50	283.00
173	SEG[107]	-1174.50	283.00
174	SEG[108]	-1201.50	283.00
175	SEG[109]	-1228.50	283.00

PAD No.	Pin Name	X	Y
176	SEG[110]	-1255.50	283.00
177	SEG[111]	-1282.50	283.00
178	SEG[112]	-1309.50	283.00
179	SEG[113]	-1336.50	283.00
180	SEG[114]	-1363.50	283.00
181	SEG[115]	-1390.50	283.00
182	SEG[116]	-1417.50	283.00
183	SEG[117]	-1444.50	283.00
184	SEG[118]	-1471.50	283.00
185	SEG[119]	-1498.50	283.00
186	SEG[120]	-1525.50	283.00
187	SEG[121]	-1552.50	283.00
188	SEG[122]	-1579.50	283.00
189	SEG[123]	-1606.50	283.00
190	SEG[124]	-1633.50	283.00
191	SEG[125]	-1660.50	283.00
192	SEG[126]	-1687.50	283.00
193	SEG[127]	-1714.50	283.00
194	COM[1]	-1784.50	283.00
195	COM[3]	-1817.50	283.00
196	COM[5]	-1850.50	283.00
197	COM[7]	-1883.50	283.00
198	COM[9]	-1916.50	283.00
199	COM[11]	-1949.50	283.00
200	COM[13]	-1982.50	283.00
201	COM[15]	-2015.50	283.00
202	COM[17]	-2048.50	283.00
203	COM[19]	-2081.50	283.00
204	COM[21]	-2114.50	283.00
205	COM[23]	-2147.50	283.00
206	COM[25]	-2180.50	283.00
207	COM[27]	-2213.50	283.00
208	COM[29]	-2246.50	283.00
209	COM[31]	-2279.50	283.00
210	COM[33]	-2312.50	283.00

PAD No.	Pin Name	X	Y
211	COM[35]	-2345.50	283.00
212	COM[37]	-2378.50	283.00
213	COM[39]	-2411.50	283.00
214	COM[41]	-2444.50	283.00
215	COM[43]	-2477.50	283.00
216	COM[45]	-2510.50	283.00
217	COM[47]	-2543.50	283.00
218	COM[49]	-2576.50	283.00
219	COM[51]	-2609.50	283.00
220	COM[53]	-2642.50	283.00
221	COM[55]	-2675.50	283.00
222	COM[57]	-2708.50	283.00
223	COM[59]	-2741.50	283.00
224	COM[61]	-2774.50	283.00
225	COM[63]	-2807.50	283.00
226	COM[65]	-2840.50	283.00
227	COM[67]	-2873.50	283.00
228	COM[69]	-2906.50	283.00
229	COM[71]	-2939.50	283.00
230	COM[73]	-2972.50	283.00
231	COM[75]	-3005.50	283.00
232	COM[77]	-3038.50	283.00
233	COM[79]	-3071.50	283.00
234	COM[81]	-3104.50	283.00
235	COM[83]	-3137.50	283.00
236	COM[85]	-3170.50	283.00
237	COM[87]	-3203.50	283.00
238	COM[89]	-3236.50	283.00
239	COM[91]	-3269.50	283.00
240	COM[93]	-3302.50	283.00
241	COM[95]	-3335.50	283.00
242	COM[97]	-3368.50	283.00
243	COM[99]	-3401.50	283.00
244	COM[101]	-3434.50	283.00
245	COM[103]	-3467.50	283.00

PAD No.	Pin Name	X	Y
246	COM[105]	-3500.50	283.00
247	COM[107]	-3533.50	283.00
248	COM[109]	-3566.50	283.00
249	COM[111]	-3599.50	283.00
250	COM[113]	-3632.50	283.00
251	COM[115]	-3665.50	283.00
252	COM[117]	-3698.50	283.00
253	COM[119]	-3731.50	283.00
254	COM[121]	-3764.50	283.00
255	COM[123]	-3797.50	283.00
256	COM[125]	-3830.50	283.00
257	COM[127]	-3863.50	283.00
258	COMS2	-3896.50	283.00
259	PS0	-3858.00	-315.50
260	VSS1	-3778.00	-315.50
261	PS1	-3698.00	-315.50
262	VDD1	-3618.00	-315.50
263	PS2	-3538.00	-315.50
264	VSS1	-3458.00	-315.50
265	CSB	-3378.00	-315.50
266	RST	-3298.00	-315.50
267	A0	-3218.00	-315.50
268	RWR	-3138.00	-315.50
269	ERD	-3058.00	-315.50
270	D0	-2978.00	-315.50
271	D1	-2898.00	-315.50
272	D2	-2818.00	-315.50
273	D3	-2738.00	-315.50
274	D4	-2658.00	-315.50
275	D5	-2578.00	-315.50
276	D6	-2498.00	-315.50
277	D7	-2418.00	-315.50
278	RST	-2338.00	-315.50
279	CSB	-2258.00	-315.50
280	VDD1	-2178.00	-315.50

PAD No.	Pin Name	X	Y
281	VDD1	-2098.00	-315.50
282	VDD1	-2018.00	-315.50
283	VDD2	-1938.00	-315.50
284	VDD2	-1858.00	-315.50
285	VDD2	-1778.00	-315.50
286	VDD2	-1698.00	-315.50
287	VDD3	-1618.00	-315.50
288	VDD3	-1538.00	-315.50
289	VSS3	-1458.00	-315.50
290	VSS3	-1378.00	-315.50
291	VSS2	-1298.00	-315.50
292	VSS2	-1218.00	-315.50
293	VSS2	-1138.00	-315.50
294	VSS2	-1058.00	-315.50
295	VSS1	-978.00	-315.50
296	VSS1	-898.00	-315.50
297	VSS1	-818.00	-315.50
298	VSS1	-738.00	-315.50
299	VDD2	-658.00	-315.50
300	VDD2	-578.00	-315.50
301	VDD2	-498.00	-315.50
302	VDD2	-418.00	-315.50
303	VDD3	-338.00	-315.50
304	VDD3	-258.00	-315.50
305	MF2	-178.00	-315.50
306	MF1	-98.00	-315.50
307	MF0	-18.00	-315.50
308	DS0	62.00	-315.50
309	DS1	142.00	-315.50
310	VMO	222.00	-315.50
311	VMO	302.00	-315.50
312	VMO	382.00	-315.50
313	VSS2	462.00	-315.50
314	V0I	542.00	-315.50
315	V0I	622.00	-315.50

PAD No.	Pin Name	X	Y
316	V0I	702.00	-315.50
317	V0I	782.00	-315.50
318	V0S	862.00	-315.50
319	V0O	942.00	-315.50
320	V0O	1022.00	-315.50
321	XV0O	1102.00	-315.50
322	XV0O	1182.00	-315.50
323	XV0S	1262.00	-315.50
324	XV0I	1385.00	-315.50
325	XV0I	1465.00	-315.50
326	XV0I	1545.00	-315.50
327	XV0I	1625.00	-315.50
328	VDD1	1705.00	-315.50
329	VEXT	1785.00	-315.50
330	OSC1	1865.00	-315.50
331	DCPS	1945.00	-315.50
332	VSS1	2025.00	-315.50
333	CSEL	2105.00	-315.50
334	VD1I	2185.00	-315.50
335	VD1I	2265.00	-315.50
336	VD1O	2345.00	-315.50
337	VGO	2425.00	-315.50
338	VGO	2505.00	-315.50
339	VGS	2585.00	-315.50
340	VGI	2665.00	-315.50
341	VGI	2745.00	-315.50
342	VGI	2825.00	-315.50
343	VGI	2905.00	-315.50
344	VPP	2985.00	-315.50
345	VPP	3065.00	-315.50
346	VPP	3145.00	-315.50
347	VE	3225.00	-315.50
348	DUMMY1	3341.00	-315.50
349	DUMMY2	3421.00	-315.50
350	DUMMY3	3501.00	-315.50

PAD No.	Pin Name	X	Y
351	DUMMY4	3581.00	-315.50
352	DUMMY5	3661.00	-315.50
353	DUMMY6	3741.00	-315.50
354	DUMMY7	3821.00	-315.50

Note:

1. CSEL=H.
2. Unit: um.

5. BLOCK DIAGRAM

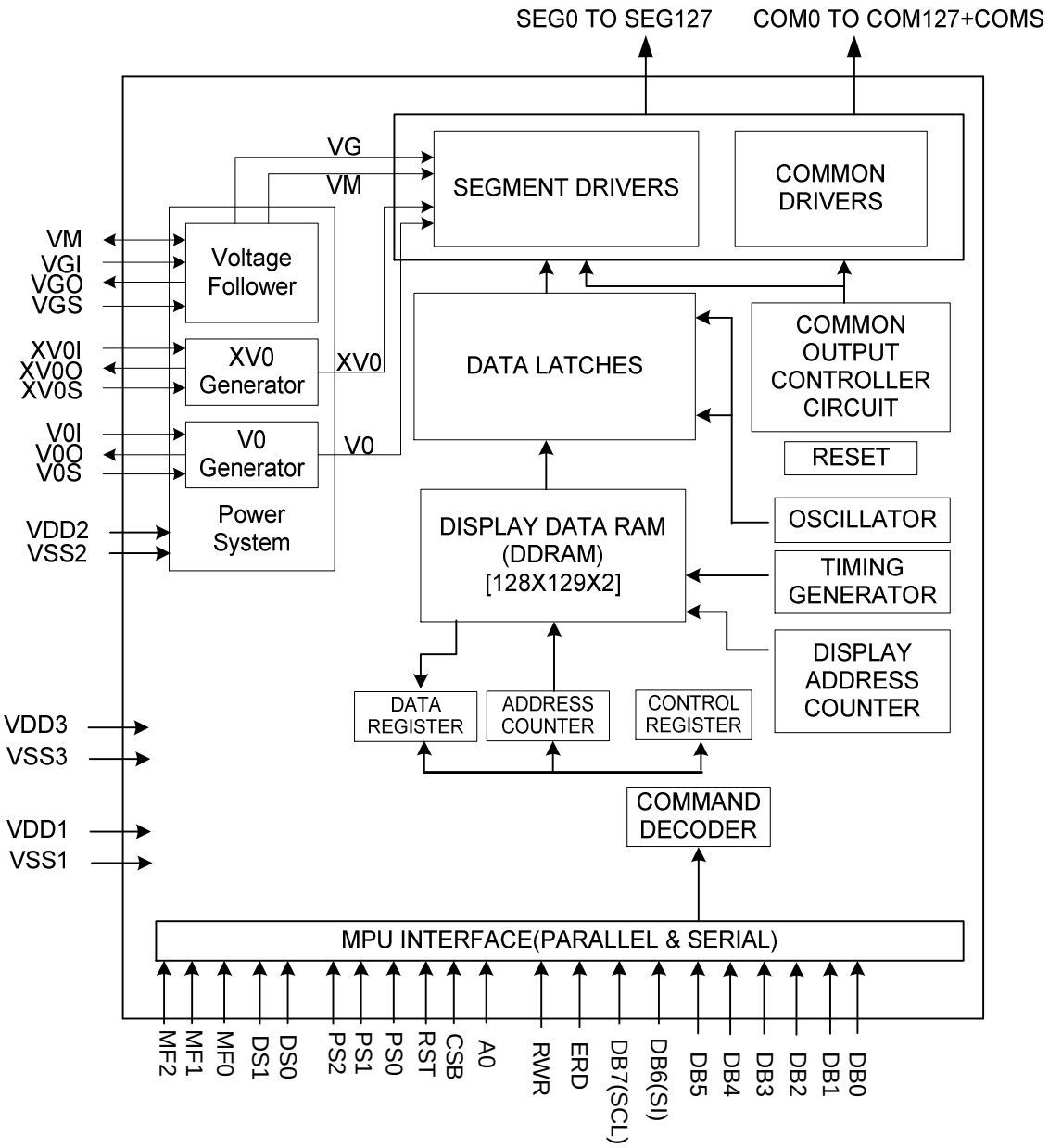


Fig.2 Block diagram

6. PIN DESCRIPTION

6.1 POWER SUPPLY

Power Supply Pin Description

Name	I/O	Description
VDD1	Power	Power supply for digital circuit. If VDD1 is the same level as VDD2, they can be connected together by FPC.
VDD2	Power	Power supply for analog circuit (booster).
VDD3	Power	Power supply for sensitive circuit (internal Vref regulator). VDD3 is the same level as VDD2, and they should be connected together by FPC.
VSS1	Power	Ground for digital circuit. VSS1, VSS2 & VSS3 should be connected together by FPC.
VSS2	Power	Ground for analog circuit (booster), it should be connected together by FPC.
VSS3	Power	Ground for sensitive circuit (Vref regulator), it should be connected together by FPC.

6.2 LCD DRIVER SUPPLY

LCD Driver Supply Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>V0O
V0I
V0S</td><td>Power</td><td>V0 is the LCD driving voltage for common circuits at negative frame.
V0O is the output of V0 regulator. V0S is the feedback of V0 regulator.
V0I is the V0 input of common circuits.
Be sure that: V0 ≥ VG > VM > VSS ≥ XV0 (under operation).
V0O, V0I & V0S should be connected together by FPC.</td></tr>
<tr><td>XV0O
XV0I
XV0S</td><td>Power</td><td>XV0 is the LCD driving voltage for common circuits at positive frame.
XV0O is the output of XV0 regulator. XV0S is the feedback of XV0 regulator.
XV0I is the XV0 input of common circuits.
XV0O, XV0I & XV0S should be connected together by FPC.</td></tr>
<tr><td>VGO
VGI
VGS</td><td>Power</td><td>VG is the LCD driving voltage for segment circuits.
A storage capacitor on FPC or system for VG is required.
VGO is the output of VG regulator. VGS is the feedback of VG regulator.
VGI is the VG input of segment circuits.
VGO, VGI & VGS should be connected together by FPC.
Be aware that: 1.8V ≤ VG < VDD2.</td></tr>
<tr><td>VMO</td><td>Power</td><td>VMO is the output of VM, which is the LCD driving voltage for common circuits.
A storage capacitor on FPC or system for VM is required.
Be aware that: 0.7V < VM < VDD2.
When the internal power circuit is active, the VG and VM are generated according to the bias setting as shown below:
<table>
<tr><td>LCD bias</td><td>VG</td><td>VM</td></tr>
<tr><td>1/N bias</td><td>(2/N) x V0</td><td>(1/N) x V0</td></tr>
</table>
NOTE: N = 5 to 12</td></tr>
</table>

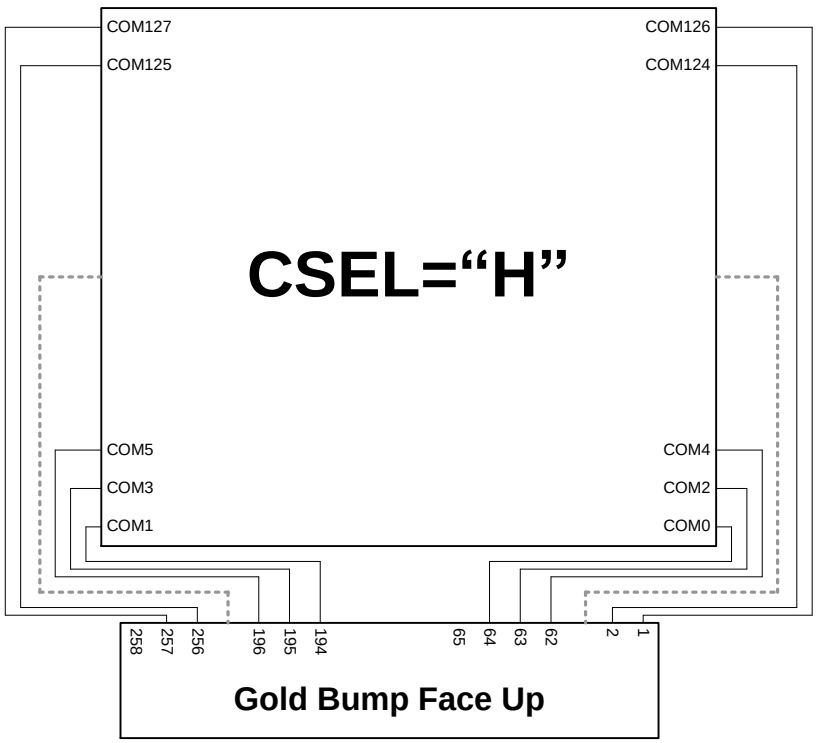
6.3 SYSTEM CONTROL

System Control Pin Description

Name	I/O	Description
VEXT	O	Reserved for testing, must set with floating.
OSC1	I	Connect OSC1 to VDD1.
DCPS	I	This pin selects the supply voltage source of the digital circuit. If system VDD1 is 3.0V ~ 3.3V, set DCPS=L to select Internal Regulator as digital circuit power. If system VDD1 is 1.8V ~ 2.8V, set DCPS=H to select VDD1 as digital circuit power.
CSEL	I	Select COM output sequence. Fix CSEL=H to enable “Interlace” mode (recommended). In interlace mode, COM2n (even number) is in the one side, COM(2n+1) (odd number) is in the opposite side.
VD1I VD1O	O	Short VD1I with VD1O externally by ITO or FPC. VD1I is the power supply pin of the internal digital circuits. When DCPS=L, VD1O is the output of the internal digital power regulator. When DCPS=H, VD1O is provided by VDD1.
VE	I	When writing EEPROM, VE should be pull-high externally.
VPP	I	When writing EEPROM, it needs external power supply voltage.
MF[2:0]	I	Reserve for testing only, recommend setting to [MF2,MF1,MF0 = 0,0,0].
DS[1:0]	I	Reserve for testing only, recommend setting to [DS1,DS0 = 0,0].

Notes:

1. When system control pin set to “H”, it should be connected to VDD1.
2. When system control pin set to “L”, it should be connected to VSS1.
3. CSEL function is illustrated as the figure below:



6.4 MICROPROCESSOR INTERFACE

Microprocessor Interface Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RST</td><td>I</td><td>Reset input pin.
When RST is “L”, initialization is executed.</td></tr>
<tr><td>PS[2:0]</td><td>I</td><td>PS[2:0] select the microprocessor interface:
<table>
<tr><th>PS2</th><th>PS1</th><th>PS0</th><th>Selected Interface Mode</th></tr>
<tr><td>L</td><td>L</td><td>H</td><td>Parallel 8080 MPU Interface</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>Parallel 6800 MPU Interface</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>Serial 3-Line Interface</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>Serial 4-Line Interface</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>Serial I^2C Interface</td></tr>
</table>
* NOTE: It is impossible to read data from the on-chip DDRAM.
For detailed interface connection, please refer to Section 7.1 and Application Circuits.</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip select input pin.
The interface is enabled only when CSB is "L" (except I^2C Interface).
When CSB is non-active, DB[7:0] are high impedance.
CSB is not used in I^2C interface; it is recommended to fix CSB at “H” by VDD1.</td></tr>
<tr><td>A0</td><td>I</td><td>Register select input pin.
A0 = “H”: DB0 to DB7 are display data.
A0 = “L”: DB0 to DB7 are control command.
A0 is not used in serial 3-Line and I^2C interface; it is recommended to fix A0 at “H” by VDD1.</td></tr>
<tr><td>RWR</td><td>I</td><td>Write execution control pin.
<table>
<tr><th>PS2</th><th>PS1</th><th>PS0</th><th>MPU Type</th><th>RWR</th><th>Description</th></tr>
<tr><td>L</td><td>H</td><td>H</td><td>6800-series</td><td>R/W</td><td>Write control input pin.
Keep this pin at “L” level.</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>8080-series</td><td>/WR</td><td>The data on DB[7:0] are latched at the rising edge of the /WR signal.</td></tr>
</table></td></tr>
<tr><td>ERD</td><td>I</td><td>Read / Write execution control pin.
<table>
<tr><th>PS2</th><th>PS1</th><th>PS0</th><th>MPU Type</th><th>ERD</th><th>Description</th></tr>
<tr><td>L</td><td>H</td><td>H</td><td>6800-series</td><td>E</td><td>The data on DB[7:0] are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>8080-series</td><td>/RD</td><td>Keep this pin at “H” level.</td></tr>
</table></td></tr>
</table>

Name	I/O	Description
DB[7:0]	I	**When using parallel interface:** DB[7:0] are 8-bit data bus. DB[7:0] are connected to the 8-bit data bus of a standard microprocessor. When chip select is not active (CSB=H), DB[7:0] are high impedance.
	I	**When using 3-Line/4-Line serial interface:** DB7: serial input data (SID). DB6: serial input clock (SCLK). DB[5:0] are high impedance and must be fixed to “H”. When chip select is not active (CSB=H), DB[7:0] are high impedance.
	I/O	**When using I^2C interface:** DB7: SCL, serial clock input. DB[6:4]: SDA_IN, serial input data. DB[3:2]: SDA_OUT, output the acknowledge signal of the I^2C interface protocol. **DB[6:2] must be connected together (SDA).** *1 DB[1:0]: SA[1:0], I^2C slave address bits of ST7571. Must connect to VDD1 or VSS1.

1. By connecting SDA_OUT to SDA_IN externally, the SDA line becomes fully I^2C interface compatible. Separating acknowledge-output from serial data input is advantageous for chip-on-glass (COG) applications. In COG applications, the ITO resistance and the pull-up resistor will form a voltage divider, which affects acknowledge-signal level. Larger ITO resistance will raise the acknowledged-signal level and system cannot recognize this level as a valid logic “0” level. By separating SDA_IN from SDA_OUT, the IC can be used in a mode that ignores the acknowledge-bit. For applications which check acknowledge-bit, it is necessary to minimize the ITO resistance of the SDA_OUT trace to guarantee a valid low level.
2. After VDD1 is turned ON, any MPU interface pins cannot be left floating.

6.5 LCD DRIVER OUTPUTS

LCD Driver Output Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>SEG0
to
SEG127</td><td>O</td><td>LCD segment driver outputs. The display data and frame signal control the output .
<table>
<tr><td rowspan="2">Display Data</td><td rowspan="2">Frame</td><td colspan="2">Segment Driver Output Voltage</td></tr>
<tr><td>Normal Display</td><td>Reverse Display</td></tr>
<tr><td>H</td><td>Positive</td><td>VG</td><td>VSS</td></tr>
<tr><td>H</td><td>Negative</td><td>VSS</td><td>VG</td></tr>
<tr><td>L</td><td>Positive</td><td>VSS</td><td>VG</td></tr>
<tr><td>L</td><td>Negative</td><td>VG</td><td>VSS</td></tr>
<tr><td colspan="2">Display off / Power save mode</td><td>VSS</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COM0
to
COM127</td><td>O</td><td>LCD common driver outputs. The internal scan signal and frame signal control the output voltage.
<table>
<tr><td>Scan Signal</td><td>Frame</td><td>Common Driver Output Voltage</td></tr>
<tr><td>H</td><td>Positive</td><td>XV0</td></tr>
<tr><td>H</td><td>Negative</td><td>V0</td></tr>
<tr><td>L</td><td>Positive</td><td>VM</td></tr>
<tr><td>L</td><td>Negative</td><td>VM</td></tr>
<tr><td colspan="2">Display off / Power save mode</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COMS2
COMS1</td><td>O</td><td>Common output for the icons.
The outputs at COMS1 and COMS2 are the same. When not used, these pins should be left open.</td></tr>
</table>

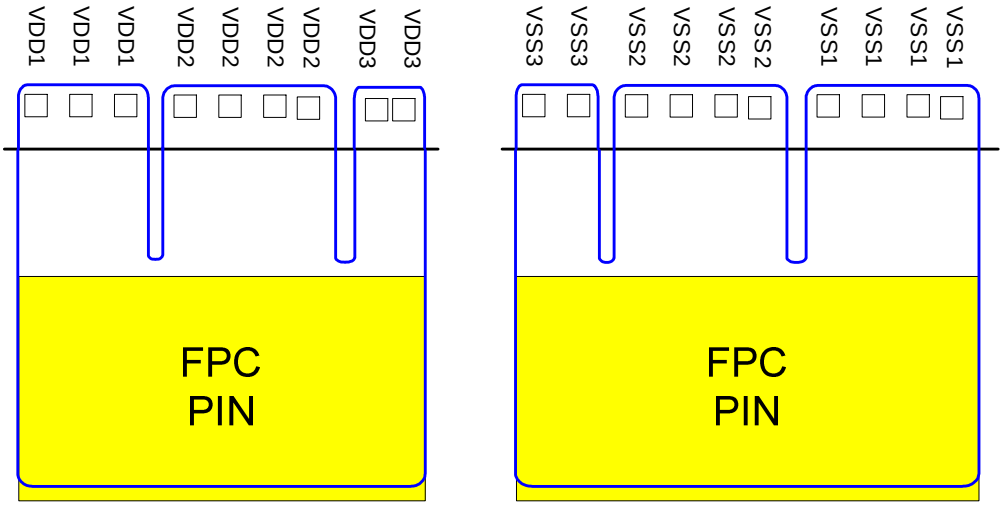
Recommend I/O Resistance

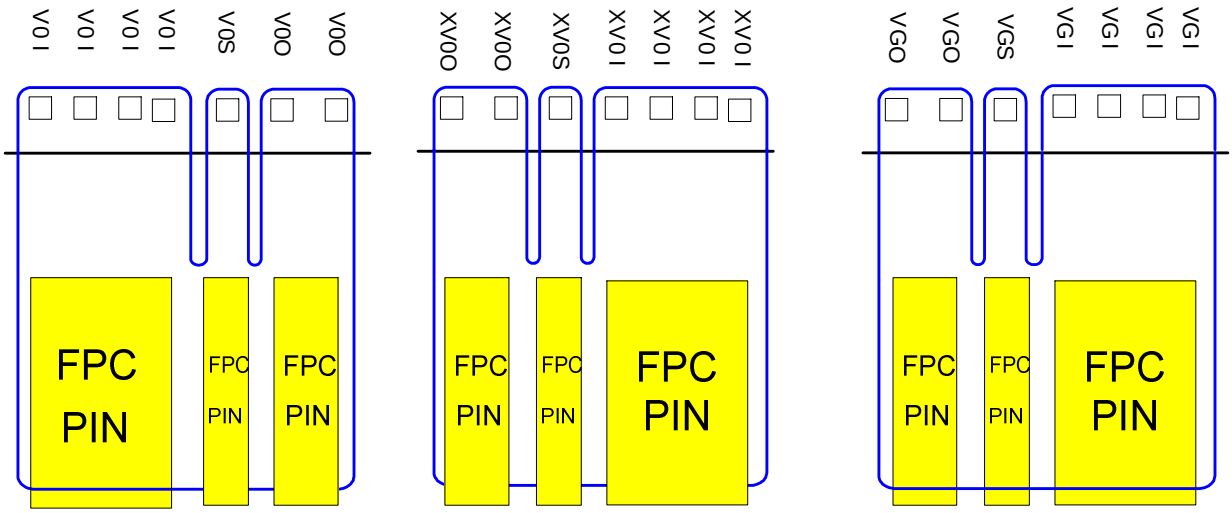
PIN Name	ITO Resister
PS[2:0], OCS1, VEXT, DCPS, MF[2:0], DS[1:0]	<5KΩ
VDD1, VDD2, VDD3, VSS1, VSS2, VSS3, VPP, VD1I, VD1O	<100Ω
CSB , ERD, RWR, A0, DB[7:0], VE	<1KΩ
V0, VG, VM, XV0, VD1	<500Ω
RST	<10KΩ

Note:

1. These Limitations include the bottleneck of ITO layout.
2. Keep the ITO resistance of COM0 ~ COM127 be equal, and so it is of SEG0 ~ SEG127.
3. If using I^2C interface mode, the resistance of SDA signal is recommended to be lower than 300Ω (if the system pull up resistor is 4.7KΩ).
4. If LCD panel size is larger than 1.5”, the resistance limitations will be lower.
5. To avoid the noise in different power system affect other power system, please separate different power source on ITO layout. Please refer to the ITO Layout Reference.
6. The V0, XV0 and VG power circuits have output pins, input pins and a sensor input. To avoid the power noise affects the sensor of the power circuits. The trace should be separated by ITO and should be connected together by FPC.

ITO Layout Reference





7. FUNCTIONAL DESCRIPTION

7.1 MICROPROCESSOR INTERFACE

Chip Select Input

CSB pin is used for chip selection. ST7571 can interface with an MPU when CSB is “L”. When CSB is “H”, the inputs of A0, ERD and RWR with any combination will be ignored and DB[7:0] are high impedance. In 3-Line and 4-Line serial interface, the internal shift register and serial counter are reset when CSB is “H”.

Parallel / Serial Interface

ST7571 has types of interface for kinds of MPU. The MPU interface is selected by PS[2:0] pins as shown in Table 1. The read-function is not available.

Table 1 Parallel / Serial Interface Mode

PS2	PS1	PS0	Type	CSB	A0	ERD	RWR	MPU Interface
L	L	H	Parallel	CSB	A0	/RD	/WR	8080-series parallel interface
L	H					E	R/W	6800-series parallel interface
L	L	L	Serial	CSB	---	---	---	3-Line SPI interface
L	H				A0			4-Line SPI interface
H	L	L		---	---	---	---	I^2C Interface

Note: The un-used pins are marked as “---” and should be fixed to “H” by VDD1.

Parallel Interface (PS2 = “L” & PS0 = “H”)

The 8-bit data bus is used in parallel interface and the type of MPU is selected by PS1 as shown in Table 2. The type of data transfer is determined by signals at A0, ERD and RWR as shown in Table 3.

Table 2 Microprocessor Selection for Parallel Interface

PS1	CSB	A0	ERD	RWR	DB[7:0]	MPU bus
L	CSB	A0	/RD	/WR	DB[7:0]	8080-series
H	CSB	A0	E	R/W	DB[7:0]	6800-series

Table 3 Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	ERD (E)	RWR (R/W)	ERD (/RD)	RWR (/WR)	
L	H	L	H	L	Writes to internal register (instruction)
H	H	L	H	L	Display data write

Serial Interface Selection

By setting PS[2:0], one of the Serial Interfaces can be selected. In 3-Line or 4-Line SPI mode, the internal 8-bit shift register and 3-bit counter are reset when IC is not active (CSB=“H”).

Serial mode	PS[2:0]	CSB	A0	ERD	RWR	DB[7:0]
3-Line SPI	L, L, L	CSB	---	---	---	DB7=SID, DB6=SCLK
4-Line SPI	L, H, L	CSB	A0	---	---	DB[5:0]= ---
I^2C SPI	H, L, L	---	---	---	---	Refer to I^2C Interface. DB7=SCL, DB[6:4]=SDA_IN, DB[3:2]=SDA_OUT, DB[1:0]=SA[1:0]

Note: The un-used pins are marked as “---” and should be fixed to “H” by VDD1.

Note:

1. The pin setting to be “H” should connect to VDD1.
2. The pin setting to be “L” should connect to VSS1.

4-Line SPI Mode (PS0 = "L", PS1 = "H", PS2 = "L")

When IC is active (CSB="L"), serial data (SID) and serial clock (SCLK) inputs are enabled. When ST7571 is not active (CSB="H"), the internal 8-bit shift register and 3-bit counter are reset. The display data/command indication is controlled by the register selection pin (A0). The signals transferred on data bus will be display data when A0 is high and will be instruction when A0 is low. The read feature is not supported. Serial data on SID is latched at the rising edge of serial clock on SCLK. After the 8th serial clock, the serial data will be processed as 8-bit parallel data. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access.

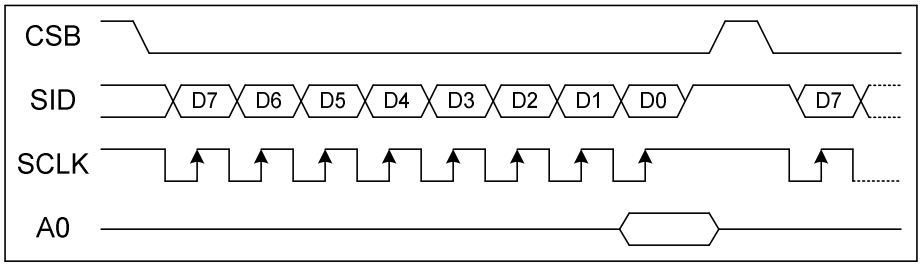
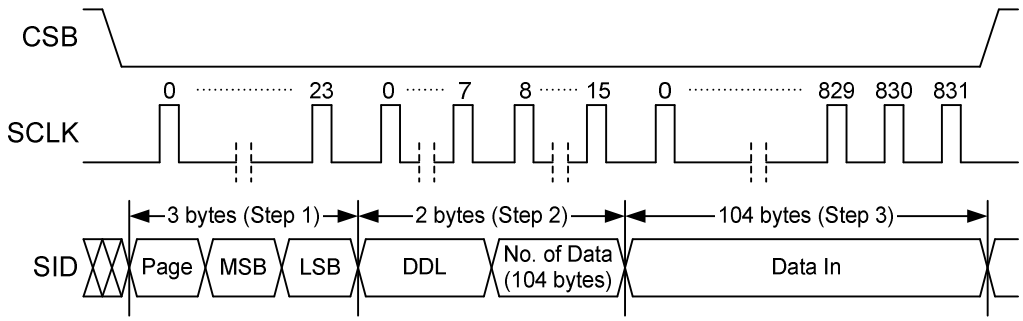


Fig. 3 4-line SPI Timing

3-Line SPI Mode (PS0 = "L", PS1 = "L", PS2= "L")

In 3-Line mode, default message from MCU is command. The Display Data Length command (2 bytes command) must be set before writing display data into Display Data RAM, after the display data is sent over, the next message is turned to be command. Signals on SID are latched at the rising edge of SCLK. After receiving 8-bit display data, the column address pointer of DDRAM will be increased by one automatically.



(1) Set Page and Column Address.

Command	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Set Page Address	1	0	1	1	P3	P2	P1	P0
Set Column Address MSB	0	0	0	1	0	X7	X6	X5
Set Column Address LSB	0	0	0	0	X4	X3	X2	X1

(2) Set Display Data Length (DDL) command and No. of Data Bytes.

Command	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Set Display Data Length (DDL)	1	1	1	0	1	0	0	0
Set No. of Data Bytes	Display Data Length (bytes)							

(3) This figure is an example for 104 Data bytes to be transferred.

Fig. 4 3-Line SPI Timing (A0 is not used)

"Set Display Data Length" is used in 3-Line SPI mode only. It is 2-byte instruction: the first one informs the LCD driver and the second one sets the counter of input data (in bytes). After these two commands, the following messages will be data, till the data counter is cleared. If data is stopped during transmitting, it is not a valid data. A new data (8 bits) must write again. NOTE: If CSB is "H" before the end of a transmission, it stops this transfer and the next access should be re-initialized.

I²C Interface (PS0= "L", PS1= "L", PS2= "H")

The I²C Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCLK). Both lines must be connected with a pull-up resistor which drives SDA and SCLK to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.

The I²C interface of ST7571 supports write access and read of acknowledge-bit. The I²C interface receives and executes the commands sent via the I²C Interface. It also receives RAM data and sends it to the Display RAM.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated in Fig 5.

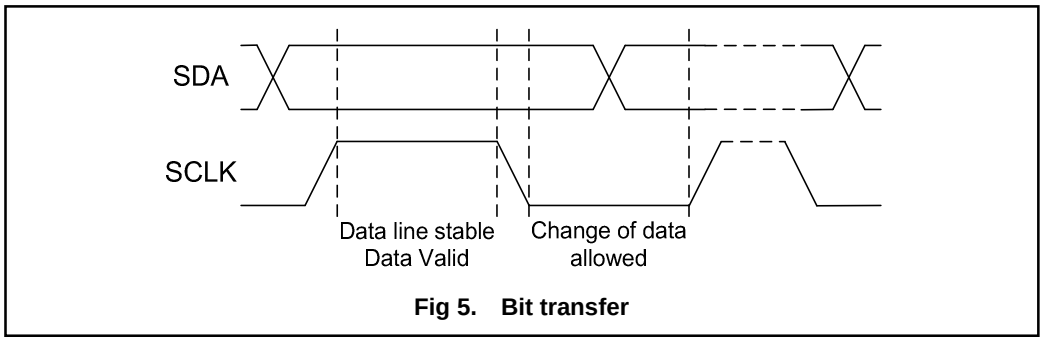


Fig 5. Bit transfer

START AND STOP CONDITIONS

Both SDA and SCLK lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA, while SCLK is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCLK is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig 6.

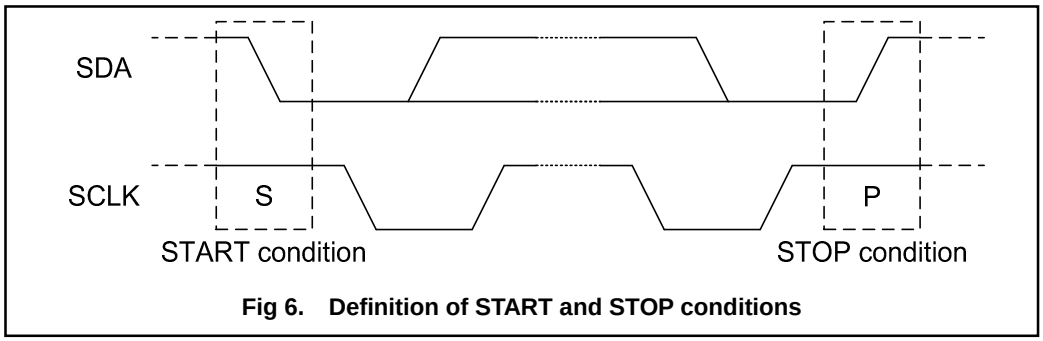


Fig 6. Definition of START and STOP conditions

SYSTEM CONFIGURATION

The system configuration is illustrated in Fig 7 and some word-definitions are explained below:

- Transmitter: the device which sends the data to the bus.
- Receiver: the device which receives the data from the bus.
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer.
- Slave: the device which is addressed by a master.
- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: the procedure to ensure that, if more than one master tries to control the bus simultaneously, only one is allowed to do so and the message is not corrupted.
- Synchronization: procedure to synchronize the clock signals of two or more devices.

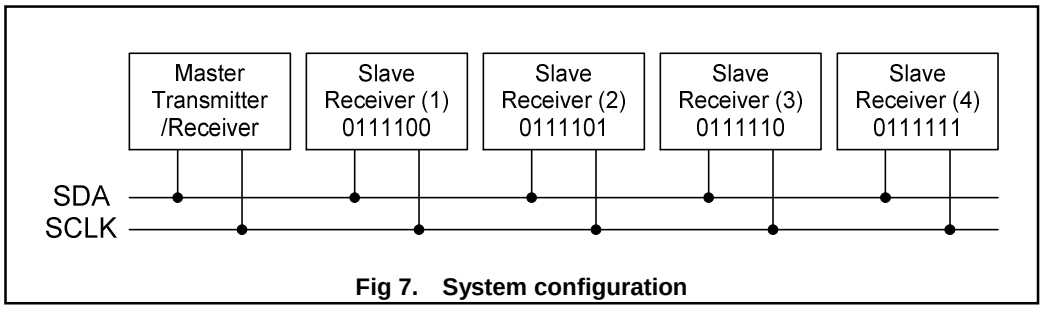


Fig 7. System configuration

ACKNOWLEDGEMENT

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on SDA by the transmitter during the time when the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge-bit after the reception of each byte. A master receiver must also generate an acknowledge-bit after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the slave transmitter by not generating a acknowledge-bit on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I^2C Interface is illustrated in Fig 8.

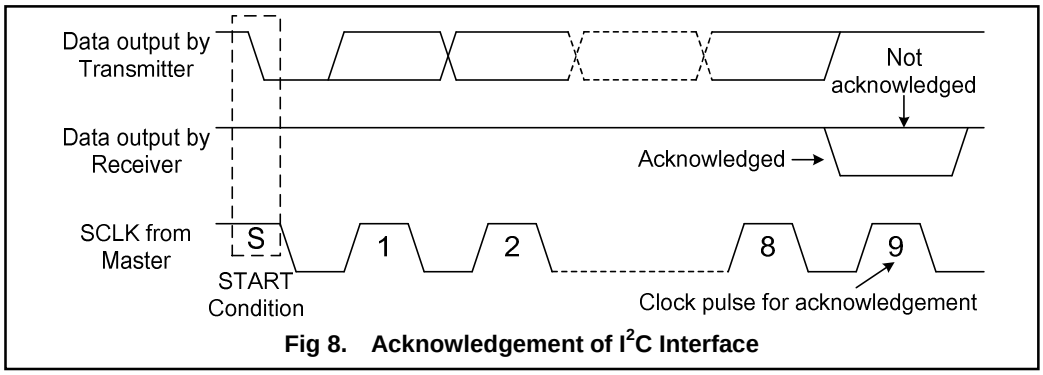


Fig 8. Acknowledgement of I^2C Interface

I^2C INTERFACE PROTOCOL

ST7571 supports command/data write to addressed slaves on the bus.

Before any data is transmitted on the I^2C Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111100, 0111101, 0111110 and 0111111) are reserved for ST7571. The least significant 2 bits of the slave address is set by connecting SA0 and SA1 to either logic 0 (VSS1) or logic 1 (VDD1).

The I^2C Interface protocol is illustrated in Fig 9.

The sequence is initiated with a START condition (S) from the I²C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C Interface transfer. After acknowledgement, one or more command words are followed and define the status of the addressed slaves. A command word consists of a control byte, which defines Co and A0, and a data byte.

The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data byte(s) will follow. The state of the A0 bit defines whether the following data bytes are interpreted as commands or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte either a series of display data bytes or command data bytes may follow (depending on the A0 bit setting).
If the A0 bit of the last control byte is set to logic 1, these data bytes (display data bytes) will be stored in the display RAM at the address specified by the internal data pointer. The data pointer is automatically updated and the data is directed to the intended ST7571 device.
If the A0 bit of the last control byte is set to logic 0, these data bytes (command data byte) will be decoded and the setting of ST7571 will be changed according to the received commands.

Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

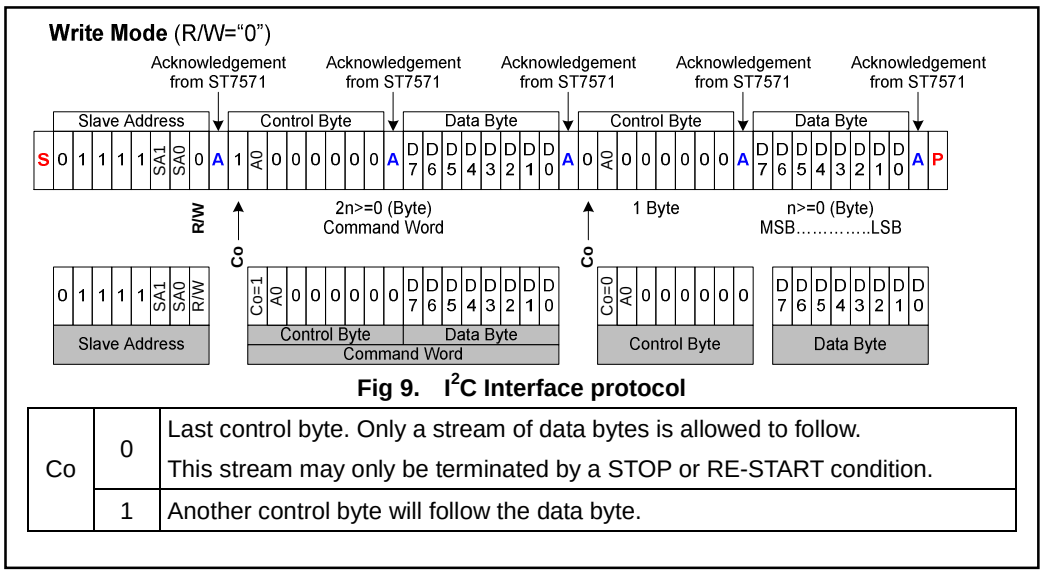


Fig 9. I²C Interface protocol

Co	0	Last control byte. Only a stream of data bytes is allowed to follow. This stream may only be terminated by a STOP or RE-START condition.
	1	Another control byte will follow the data byte.

Data Transfer

ST7571 uses bus holder and internal data bus for data transfer by the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in Fig. 10 and Fig. 11.

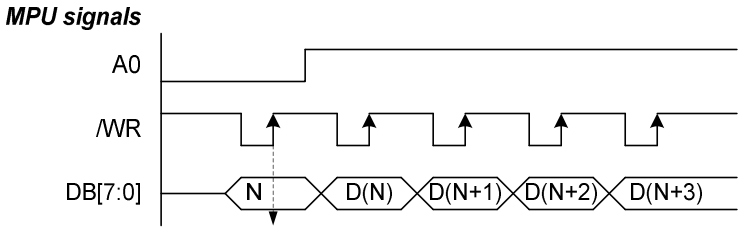


Fig. 10 External Timing from MPU

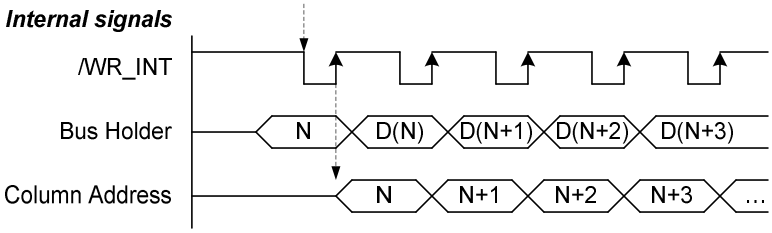


Fig. 11 Internal Timing of IC

7.2 DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 129-row by 128-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 129 rows are divided into 16 pages of 8 lines and the 17th page with a single line (DB0 only). Data is written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines. The LCD controller and MPU interface operate independently, data can be written into RAM at the same time when data is being displayed without flicker on LCD.

Page Address Circuit

It incorporates 4-bit Page Address register changed by only the “Set Page” instruction. Page Address 16 is a special RAM area for the icons and display data DB0 is only valid. The page address is set from 0 to 15, and Page 16 is for Icon page.

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM. It incorporates 7-bit Line Address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 128-bit RAM data to the display data latch circuit. When icon is enabled by setting icon control register, display data of icons are not scrolled because the MPU can not access Line Address of icons.

Column Address Circuit

When set Column Address MSB / LSB instruction is issued, 7-bit (X[7:1]) are set and lowest bit (X0) is set to “0”. The internal column address (X[7:0]) is increased by 1 automatically after each byte of data access (write data). After sequential access twice, the column address (X[7:1]) will point to the next column address. Please refer to Fig. 12.

Segment Control Circuit

This circuit controls the display data by the display ON / OFF, reverse display ON / OFF and entire display ON / OFF instructions without changing the data in the Display Data RAM.

SEG Output	SEG 0		SEG 1		SEG 2		SEG 3		…	SEG 124		SEG 125		SEG 126		SEG 127	
Column Address X[7:1]	00H		01H		02H		03H		…	7CH		7DH		7EH		7FH	
Internal column address X[7:0]	00	01	02	03	04	05	06	07	…	F8	F9	FA	FB	FC	FD	FE	FF
Display Data (MX=0)	1	1	1	0	0	1	0	0	…	1	1	1	0	0	1	0	0
LCD panel display									…								
Display data (MX=1)	0	0	0	1	1	0	1	1	…	0	0	0	1	1	0	1	1
LCD panel display									…								

Fig. 12 The Relationship between the Column Address and The Segment Outputs

7.3 LCD DISPLAY CIRCUITS

Oscillator

This is on-chip Oscillator without external resistor. When the internal oscillator is used, this pin must connect to VDD1; when the external oscillator is used, this pin could be input pin. This oscillator signal is used in the voltage converter and display timing generation circuit.

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL (internal), generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 128-bit display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (FR) which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Fig. 13.

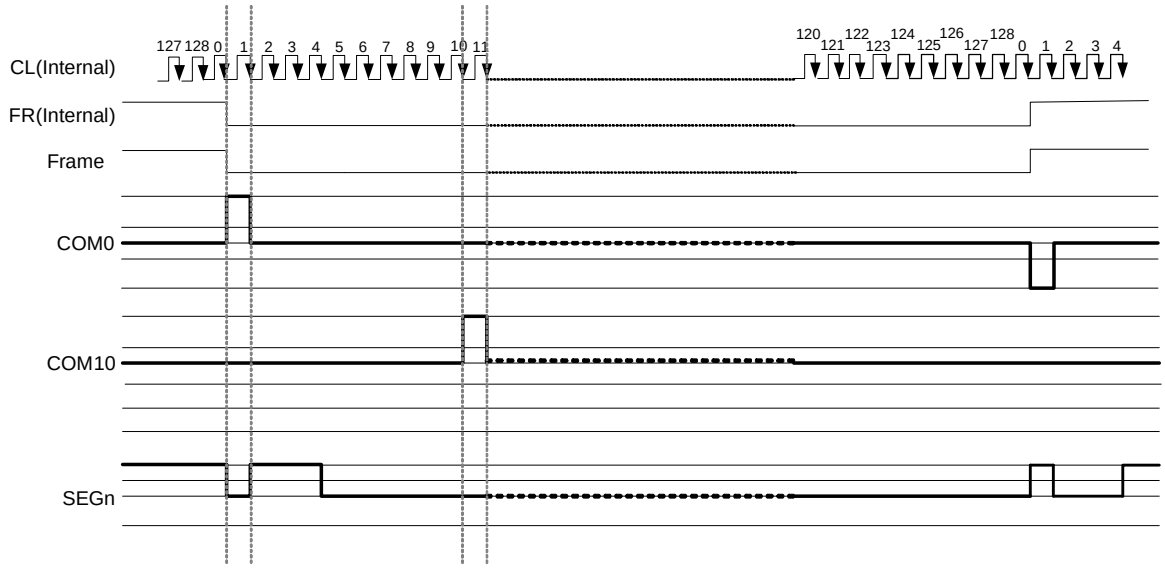


Fig. 13 Frame AC Driving Waveform (Duty Ratio: 1/129)

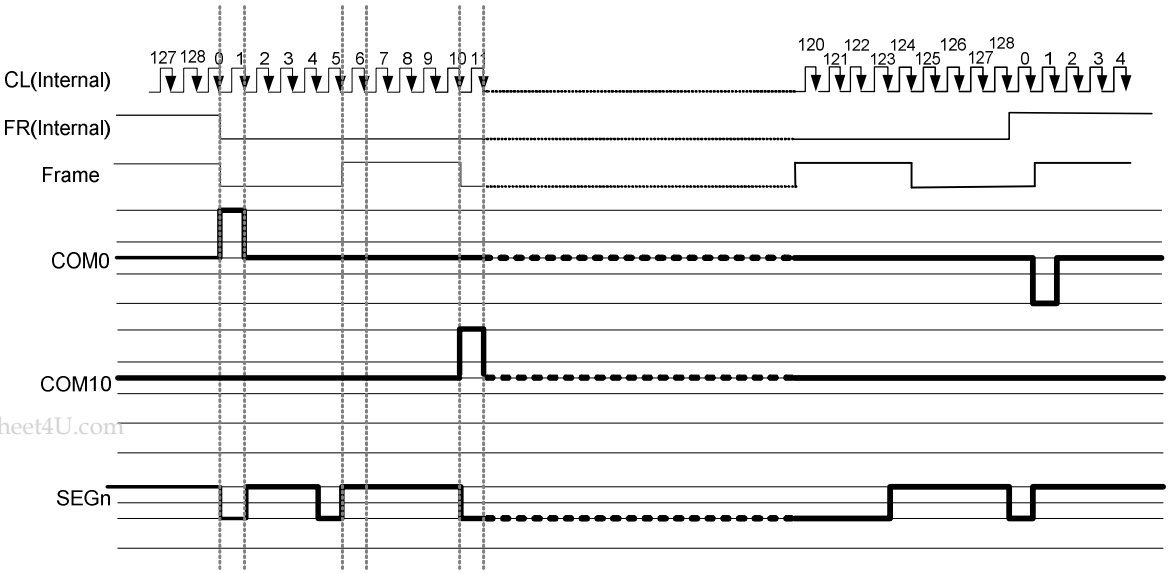


Fig. 14 N-Line Inversion Driving Waveform (N=5,Duty Ratio=1/129)

Partial Display on LCD

The ST7571 realizes the Partial Display function on LCD with low-duty driving for saving power consumption and showing the various display duty. To show the various display duty on LCD, LCD driving duty and bias are programmable via the instruction. And, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages. The partial display duty ratio could be set from 16 ~ 128.

If the partial display region is out of the Max. Display range, it would be no operation.

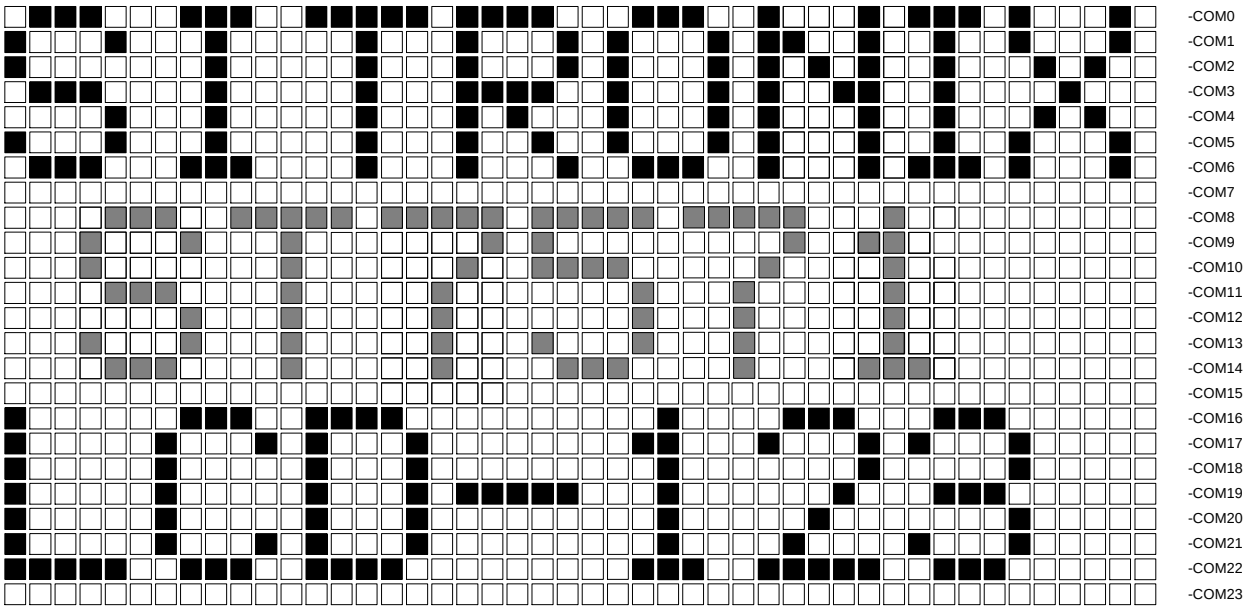


Fig. 15 Reference Example for Partial Display

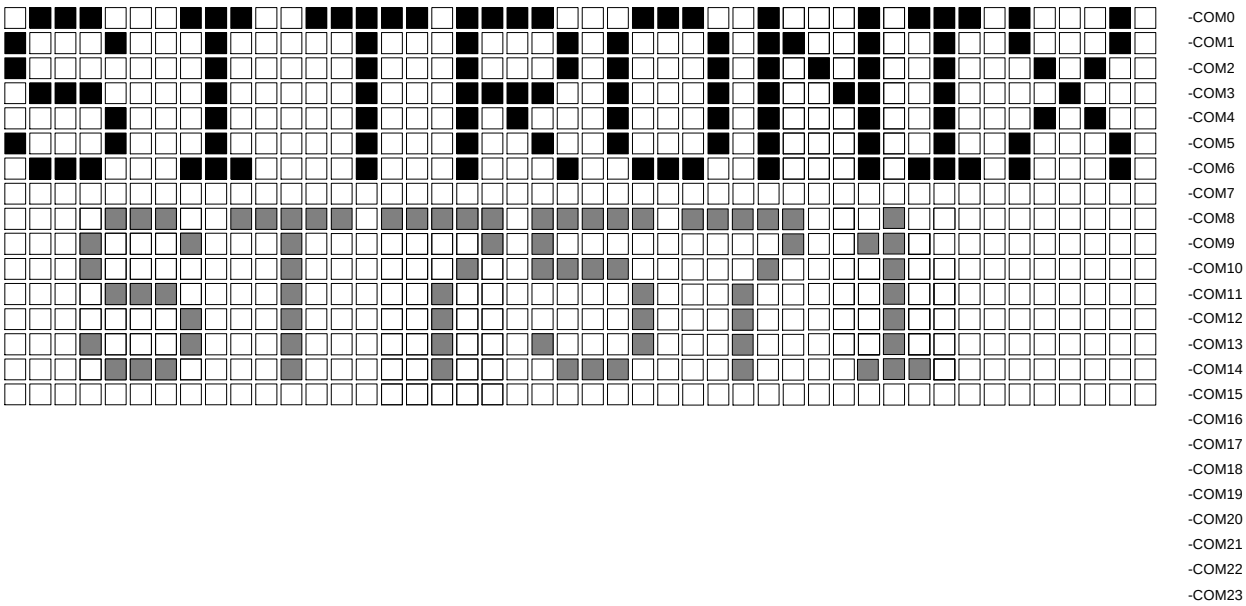


Fig. 16 Partial Display (Partial Display Duty=16, initial COM0=0)

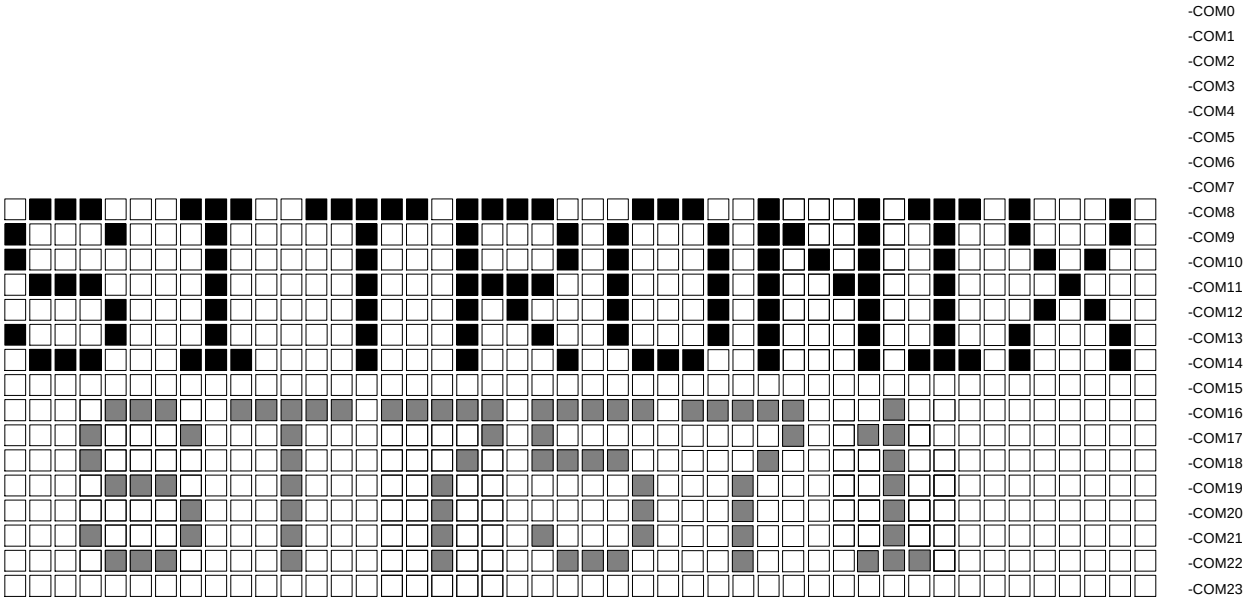


Fig. 17 Moving Display (Partial Display Duty=16, initial COM0=8)

7.4 POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction.

Voltage Regulator Circuits

The internal Voltage Regulator circuit provides the liquid crystal operating voltage (V0) by adjusting resistors (SRR and EV).

The parameter “SRR” can be set by “Select Regulator Register”.

The parameter “EV” can be set by “Set Electronic Volume Register”, and the range of EV is 0~63.

$$V0 = SRR \times \left(1 - \frac{(63 - EV)}{210}\right) \times 2.1$$

Table 5 Internal Regulator Ratio depending on 3-bit Data (R2 R1 R0)

	3-bit data settings (R2 R1 R0)							
	0 0 0	**0 0 1**	**0 1 0**	**0 1 1**	**1 0 0**	**1 0 1**	**1 1 0**	**1 1 1**
SRR (Select Regulator Ratio)	2.3	3.0	3.7	4.4	5.1	5.8	6.5	7.2

Fig. 18 shows V0 voltage measured by adjusting regulator register ratio and 6-bit electronic registers for each temperature coefficient at Ta = 25°C. **The recommended range of EV setting is level 16 ~ 47**.

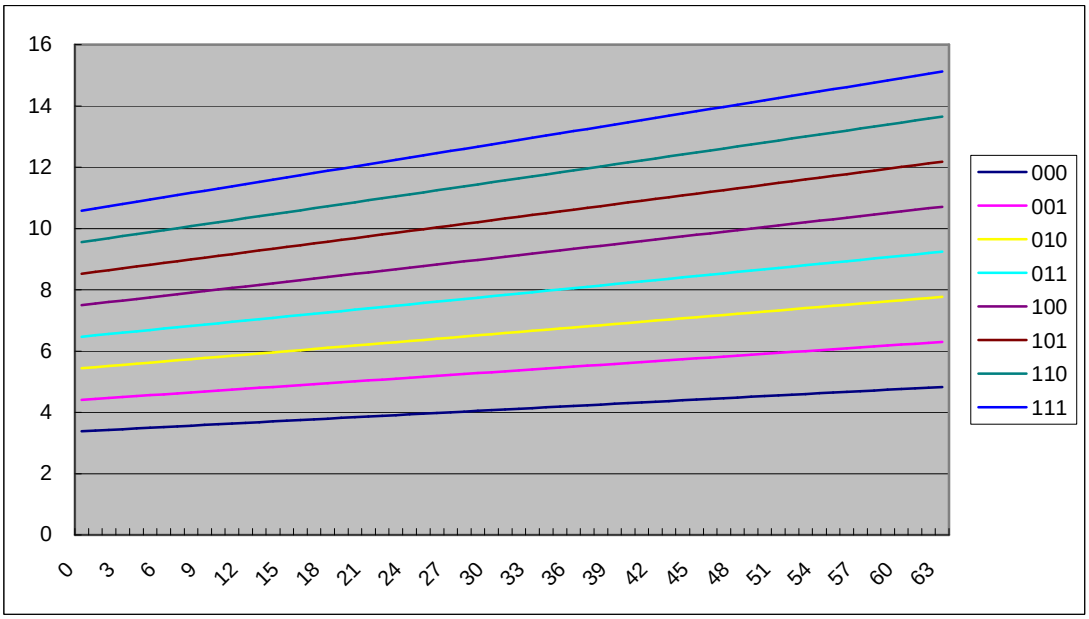


Fig. 18 Electronic Volume Level (25°C)

Voltage Follower Circuits

V0 is resistively divided into two voltage levels (VG, VM), and those output impedance are converted by the Voltage Follower for increasing drive capability. Table 6 shows the relationship between VG to VM level and each duty ratio.

Table 6 The Relationship between V1 to V4 Level and Each Duty Ratio

LCD Bias	VG	VM	Remarks
1/N	2/N x V0	1/N x V0	N = 5 to 12

Booster Efficiency

The Booster Efficiency Command could be used to choose the best Booster performance. Booster Efficiency (Level1~4) can easily set the best Booster performance with suitable current consumption. If the Booster Efficiency is set to a higher level (level2 is higher than level1), the Boost Efficiency is better than lower level, and it just needs few more power consumption current. When the LCD Panel loading is heavier, the performance of Booster Efficiency will be lower. We could select higher BE level to improve the efficiency with just few more current increased.

7.5 RESET CIRCUITS

Setting RST to “L” can initialize internal function. RST pin is connected to the reset pin of MPU and initialization by RST pin is essential before operating. Please note the hardware reset is not same as the software reset. When RST becomes “L”, the hardware reset procedure will start. When RESET instruction is executed, the software reset procedure will start. The procedure is listed below:

Procedure	Hardware Reset	Software Reset
Clear Serial Counter and Shift Register (if using Serial Interface)	V	V
Page Address, P[3:0]=0 (Page 0)	V	V
Column Address, X[7:0]=00h (Column 0)	V	V
Display ON/OFF, D=0 (Display OFF)	V	X
Reverse Display, REV=0 (Normal)	V	X
Entire Display ON, EON=0 (Normal)	V	X
Icon Control, ION=0 (OFF)	V	X
Start Line, S[6:0]=0 (1st line of DDRAM)	V	V
COM0, C[6:0]=0 (COM0 Pin)	V	X
Display Duty, L[7:0]=0 (1/129)	V	X
N-Line, N[4:0]=0 (N-Line OFF)	V	X
Power Control, VC=0, VR=0, VF=0 (Internal Power OFF)	V	X
Booster Efficiency, BE[1:0]=0,1 (Level 2)	V	X
Regulator Resistor, R[2:0]=0,0,0	V	V
Contrast Control, EV[5:0]=20h	V	V
LCD Bias, BS[2:0]=1,1,1 (1/12 bias)	V	X
Frame Rate, FR[3:0]=0,0,0,0 (77Hz)	V	X
COM Scan Direction, MY=0 (Normal)	V	X
SEG Scan Direction, MX=0 (Normal)	V	X
Oscillator Circuit: OFF	V	X
Power-Save Mode, P=0 (Release)	V	X
Display Data Length, DL[7:0]=00h (for 3-Line serial interface only)	V	V

After power-on, RAM data are undefined and the display status is “Display OFF”. It’s recommended to initialize the whole DDRAM (ex: fill all 00h or write a display pattern) before turning the Display ON (including the ICON RAM as well). Besides, the system power is not stable at the time that the power is just turned ON. After the system power is stable, a hardware reset is required to initialize internal registers.

8. INSTRUCTIONS

Instruction	A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Section
Set Mode	0	0	0	0	1	1	1	0	0	0	2-byte instruction	9.1.1
	0	0	FR3	FR2	FR1	FR0	BE1	BE0	--	0	FR[3:0]: Set frame frequency BE[1:0]: Set booster efficiency	
Write Display Data	1	0	Write data								Write data into DDRAM	9.1.2
Set Icon	0	0	1	0	1	0	0	0	1	ION	ION=0: Disable Icon function ION=1: Enable Icon function and set Page Address = 16	9.1.3
Set Page Address	0	0	1	0	1	1	P3	P2	P1	P0	Set Page Address	9.1.4
Set Column Address (MSB)	0	0	0	0	0	1	0	X7	X6	X5	Set MSB of Column Address	9.1.5
Set Column Address (LSB)	0	0	0	0	0	0	X4	X3	X2	X1	Set LSB of Column Address	9.1.6
Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=0: Display OFF D=1: Display ON	9.1.7
Set Display Start Line	0	0	0	1	0	0	0	0	--	--	2-byte instruction. Specify Line Address for the 1st display line of DDRAM (vertical scrolling).	9.1.8
	0	0	--	S6	S5	S4	S3	S2	S1	S0		
Set COM0	0	0	0	1	0	0	0	1	--	--	2-byte instruction. Specify a COM pin to be COM0 (moving partial display window).	9.1.9
	0	0	--	C6	C5	C4	C3	C2	C1	C0		
Set Display Duty	0	0	0	1	0	0	1	0	--	--	2-byte instruction. Set display duty	9.1.10
	0	0	L7	L6	L5	L4	L3	L2	L1	L0		
Set N-line Inversion	0	0	0	1	0	0	1	1	--	--	2-byte instruction. Set N-line inversion counter	9.1.11
	0	0	--	--	--	N4	N3	N2	N1	N0		
Release N-line Inversion	0	0	1	1	1	0	0	1	0	0	Exit N-line inversion mode	9.1.12
Reverse Display	0	0	1	0	1	0	0	1	1	REV	REV=0: Normal display REV=1: Reverse display	9.1.13
Entire Display ON	0	0	1	0	1	0	0	1	0	EON	EON=0: Normal display EON=1: Entire display ON	9.1.14

Instruction	A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Section
Power Control	0	0	0	0	1	0	1	VC	VR	VF	Set internal power ON/OFF	9.1.15
Select Regulator Register	0	0	0	0	1	0	0	R2	R1	R0	Select internal Regulator resistor	9.1.16
Set Contrast	0	0	1	0	0	0	0	0	0	1	2-byte instruction. Select EV for internal Regulator's reference	9.1.17
	0	0	--	--	EV5	EV4	EV3	EV2	EV1	EV0		
Select LCD bias	0	0	0	1	0	1	0	B2	B1	B0	Select LCD bias	9.1.18
Set COM Scan Direction	0	0	1	1	0	0	MY	--	--	--	Set COM scan direction: MY=0: Normal direction MY=1: Reverse direction	9.1.19
Set SEG Scan Direction	0	0	1	0	1	0	0	0	0	MX	Set SEG scan direction: MX=0: Normal direction MX=1: Reverse direction	9.1.20
Oscillator ON	0	0	1	0	1	0	1	0	1	1	Turn ON internal Oscillator	9.1.21
Set Power-Save Mode	0	0	1	0	1	0	1	0	0	P	P=0: Normal mode P=1: Enable Power-Save mode	9.1.22
Release Power-Save Mode	0	0	1	1	1	0	0	0	0	1	Exit Power-Save mode	9.1.23
RESET	0	0	1	1	1	0	0	0	1	0	Software reset	9.1.24
Set Display Data Length	--	--	1	1	1	0	1	0	0	0	2-byte instruction. Set the data counter in 3-Line SPI only	9.1.25
	--	--	DL7	DL6	DL5	DL4	DL3	DL2	DL1	DL0		
NOP	0	0	1	1	1	0	0	0	1	1	No operation	9.1.26
Reserved	0	0	1	1	1	0	0	0	0	0	Do NOT use	--
Reserved	0	0	1	1	1	0	1	1	1	0	Do NOT use	--
Reserved	0	0	1	1	1	1	--	--	--	--	Reserved for testing	--
Extension Command Set1	0	0	1	1	1	1	1	1	0	TE1	TE1=1: Enter extension Mode1	9.1.27
Extension Command Set2	0	0	1	1	0	1	0	0	0	TE2	TE2=1: Enter extension Mode2	9.1.28
Extension Command Set3	0	0	0	1	1	1	1	0	1	TE3	TE3=1: Enter extension Mode3	9.1.29

Instruction	A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
EXTENSION COMMAND SET 1											
Increase Vop offset	0	0	0	1	0	1	0	0	0	1	Increase vop offset by 1step
Decrease Vop offset	0	0	0	1	0	1	0	0	1	0	Decrease vop offset by 1 step
Return normal mode	0	0	0	0	0	0	0	0	0	0	Return normal mode
EXTENSION COMMAND SET 2											
Disable autoread	0	0	1	0	1	0	1	0	1	0	Disable autoread
Enter EEPROM mode	0	0	0	0	0	1	0	0	1	1	Enter EEPROM mode
Enable read mode	0	0	0	0	1	0	0	0	0	0	Enable read mode
Set read pulse	0	0	0	1	1	1	0	0	0	1	Set read pulse width
Exit EEPROM mode	0	0	1	0	0	0	0	0	1	1	Exit EEPROM mode
Enable erase mode	0	0	0	1	0	0	1	0	1	0	Enable erase mode
Set erase pulse	0	0	0	1	0	1	0	1	0	1	Set erase pulse width
Enable write mode	0	0	0	0	1	1	0	1	0	1	Enable write mode
Set write pulse	0	0	0	1	1	0	1	0	1	0	Set write pulse width
Return normal mode	0	0	0	0	0	0	0	0	0	0	Return normal mode
EXTENSION COMMAND SET 3											
Set Color Mode	0	0	0	0	0	1	0	0	0	B/G	Select Black/White or Gray mode B/G=1: Black/White mode; B/G=0: Gray mode (default)
Return normal mode	0	0	0	0	0	0	0	0	0	0	Return normal mode

Note: Do NOT use non-specified instructions in any extension command mode.

9. INSTRUCTION DESCRIPTION

9.1.1 Set Mode

This 2-byte instruction specifies frame frequency (FR[3:0]) and booster efficiency (BE[1:0])

The 1st Instruction

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	0	0

The 2nd Instruction

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	FR3	FR2	FR1	FR0	BE1	BE0	x'	0

Frame Frequency

FR[3:0] specifies the frame frequency:

FR3	FR2	FR1	FR0	Frame Frequency
0	0	0	0	77 Hz ±10%
0	0	0	1	51 Hz ±20%
0	0	1	0	55 Hz ±20%
0	0	1	1	58 Hz ±20%
0	1	0	0	63 Hz ±20%
0	1	0	1	67 Hz ±20%
0	1	1	0	68 Hz ±20%
0	1	1	1	70 Hz ±20%
1	0	0	0	73 Hz ±20%
1	0	0	1	75 Hz ±20%
1	0	1	0	80 Hz ±20%
1	0	1	1	85 Hz ±20%
1	1	0	0	91 Hz ±20%
1	1	0	1	102 Hz ±20%
1	1	1	0	113 Hz ±20%
1	1	1	1	123 Hz ±20%

Booster Efficiency

The efficiency of internal Booster is configurable by BE[1:0]. **The optimized setting is Level-3**.

BE1	BE0	Description
0	0	Booster Efficiency Level 1
0	1	Booster Efficiency Level 2
1	0	Booster Efficiency Level 3
1	1	Booster Efficiency Level 4

9.1.2 Write Display Data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

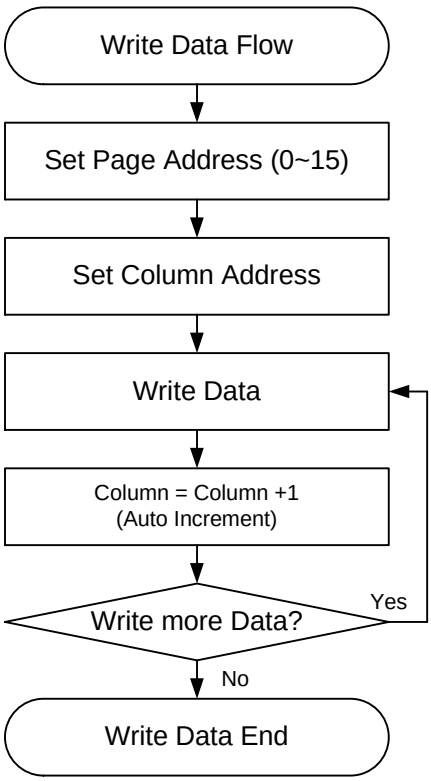


Fig. 20 Sequence for Writing Display Data

9.1.3 Set Icon

This instruction makes Icon function enable or disable. After reset, the Icon function is disabled (ION=0). When ION="1", Icon display is enabled and the page address is set to "16" for updating icon data (it is impossible to set page address to "16" by Set Page Address instruction). Therefore, when writing data for icons, "Set Icon" instruction is necessary before writing icon data. It set the page address to "16" before writing icon data. When "ION" is "0", Icon display function is not available.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	ION

ION	Description
0	Disable Icon function
1	Enable Icon display and set Page Address to "16".

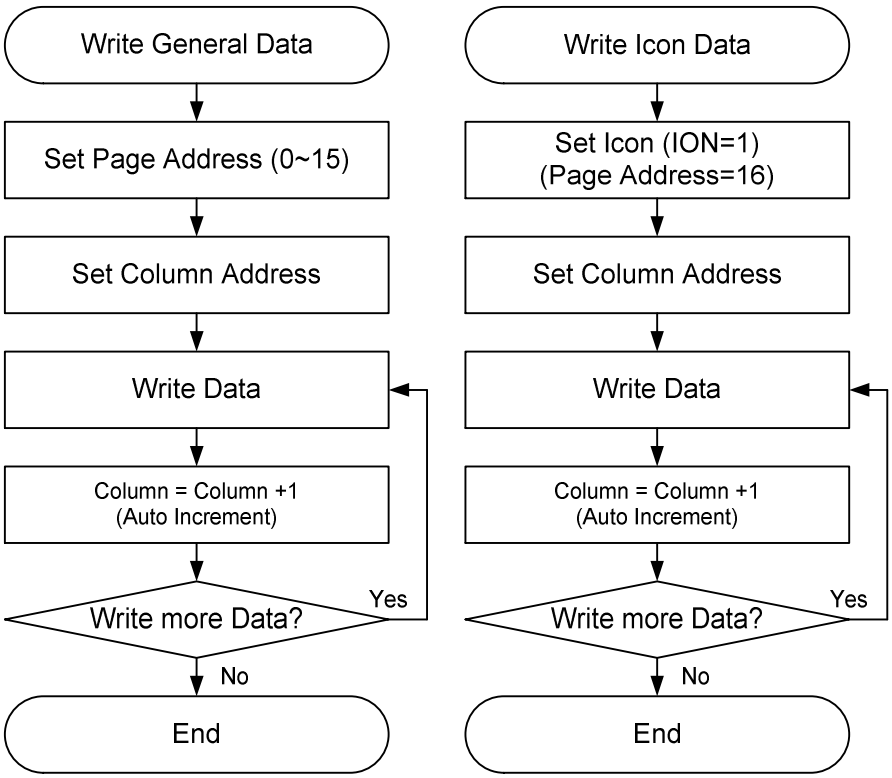


Fig. 20 Sequence for Writing Display Data

9.1.4 Set Page Address

This instruction sets the Page Address of display data RAM from the microprocessor into the page address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write display data. Changing the Page Address doesn't affect the display status. Set Page Address instruction can not be used to set the page address to "16". Use ICON control register ON/OFF instruction to set the page address to "16".

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
1	1	1	0	14
1	1	1	1	15

9.1.5 & 9.1.6 Set Column Address

These instructions set the specified column address of DDRAM into the internal Column Address register. The internal Column Address register points to the address of DDRAM for accessing display data. The Column Addresses register is automatically increased by 1 when the microprocessor accesses the display data in DDRAM.

Set Column Address (MSB)

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	X7	X6	X5

Set Column Address (LSB)

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X4	X3	X2	X1

X7	X6	X5	X4	X3	X2	X1	Column Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

9.1.7 Display ON / OFF

This instruction turns the display ON or OFF. It has priority over Entire Display ON/OFF and Reverse Display ON/OFF.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1: display ON

DON = 0: display OFF

9.1.8 Set Display Start Line

This 2-byte instruction sets the line address of DDRAM to determine the first display line. The display data of the selected line will be displayed at the top of row (COM0) on the LCD panel.

The 1st Instruction

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	0	x	x

The 2nd Instruction

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	S6	S5	S4	S3	S2	S1	S0

S6	S5	S4	S3	S2	S1	S0	Line address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:
1	1	1	1	1	0	0	124
1	1	1	1	1	0	1	125
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

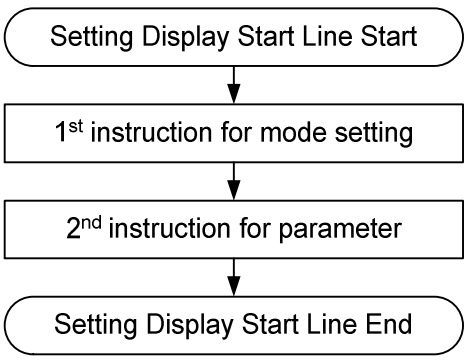


Fig. 21 Sequence for Setting Display Start Line

9.1.9 Set COM0

This 2-byte instruction set the initial row (COM) of the LCD panel. By using this instruction, it is possible to realize the window moving without the change of display data.

The 1st Instruction

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	1	x	x

The 2nd Instruction

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	C6	C5	C4	C3	C2	C1	C0

C6	C5	C4	C3	C2	C1	C0	Initial COM0
0	0	0	0	0	0	0	COM0
0	0	0	0	0	0	1	COM1
0	0	0	0	0	1	0	COM2
0	0	0	0	0	1	1	COM3
:	:	:	:	:	:	:	:
1	1	1	1	1	0	0	COM124
1	1	1	1	1	0	1	COM125
1	1	1	1	1	1	0	COM126
1	1	1	1	1	1	1	COM127

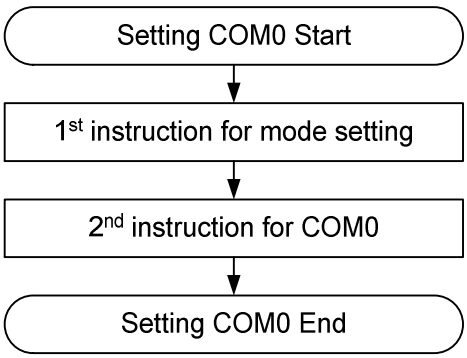


Fig. 22 Sequence for Setting COM0

9.1.10 Set Display Duty

This 2-byte instruction sets the display duty within the range of 1/(16+1) to 1/(128+1) to realize partial display.

The 1st Instruction

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	0	x	x

The 2nd Instruction

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	L7	L6	L5	L4	L3	L2	L1	L0

L7	L6	L5	L4	L3	L2	L1	L0	Selected Partial Duty Ratio
0	0	0	0	0	0	0	0	No Operation
:	:	:	:	:	:	:	:	
0	0	0	0	1	1	1	1	
0	0	0	1	0	0	0	0	1/(16+1)
0	0	0	1	0	0	0	1	1/(17+1)
:	:	:	:	:	:	:	:	:
0	1	1	0	0	1	0	0	1/(100+1)
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	1/(127+1)
1	0	0	0	0	0	0	0	1/(128+1)
1	0	0	0	0	0	0	1	No Operation
:	:	:	:	:	:	:	:	
1	1	1	1	1	1	1	1	

NOTE: The duty includes the duty for ICON.

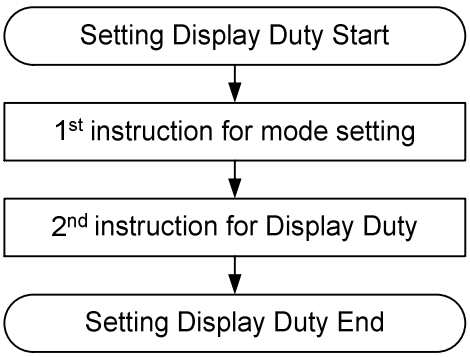


Fig. 23 Sequence for Setting Display Duty

9.1.11 Set N-line Inversion (recommended 12-line inversion for full duty, 1/129 duty)

This 2-byte instruction sets the inverted line number within range of 3 to 33 to improve the display quality by controlling the phase of the internal Frame signal. The DC bias maybe occurred if the N-line is not set well. Be sure to confirm this factor after choosing a value of N.

The 1st Instruction

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	1	x	x

The 2nd Instruction

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	x	x	N4	N3	N2	N1	N0

N4	N3	N2	N1	N0	Selected n-line inversion
0	0	0	0	0	0-line inversion (frame inversion)
0	0	0	0	1	3-line inversion
0	0	0	1	0	4-line inversion
0	0	0	1	1	5-line inversion
:	:	:	:	:	:
0	1	0	1	0	12-line inversion **(Recommend)**
					:
1	1	1	0	1	31-line inversion
1	1	1	1	0	32-line inversion
1	1	1	1	1	33-line inversion

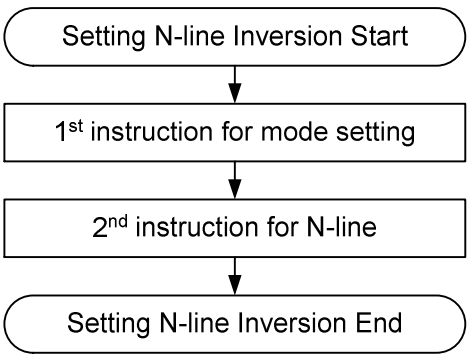


Fig. 24 Sequence for N-line Inversion

9.1.12 Release N-line Inversion

This instruction makes the inversion mode back to the frame inversion from the N-line inversion.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	0	0

9.1.13 Reverse Display

This instruction reverses the display status on LCD panel without rewriting new contents into DDRAM.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	Pixel Data in DDRAM			
	“00” (White)	“01” (Light Gray)	“10” (Dark Gray)	“11” (Black)
0 (normal)	White	Light Gray	Dark Gray	Black
1 (reverse)	Black	Dark gray	Light gray	White

9.1.14 Entire Display ON

This instruction forces the whole LCD pixels to be turned ON, regardless of the contents in DDRAM. The contents in DDRAM are not changed. This instruction has priority over the Reverse Display instruction.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

EON	Pixel Data in DDRAM			
	“00” (White)	“01” (Light Gray)	“10” (Dark Gray)	“11” (Black)
0 (normal)	White	Light Gray	Dark Gray	Black
1 (entire ON)	Black	Black	Black	Black

9.1.15 Power Control

This instruction selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Internal Power Supply Circuits	Status
0 1			Internal voltage converter circuit	OFF ON
	0 1		Internal voltage regulator circuit	OFF ON
		0 1	Internal voltage follower circuit	OFF ON

9.1.16 Select Regulator Resister

This instruction selects resistance ratio of the internal regulator resistors. Refer to the voltage regulator circuits in power supply circuit section.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	1+ (Rb / Ra)
0	0	0	2.3
0	0	1	3.0
0	1	0	3.7
0	1	1	4.4
1	0	0	5.1
1	0	1	5.8
1	1	0	6.5
1	1	1	7.2

9.1.17 Set Electronic Volume Register

This is 2-byte Instruction. The 1st instruction enters Reference Voltage mode, and the 2nd one updates the contents of the reference voltage register. After 2nd instruction, Reference Voltage mode is released.

The 1st Instruction: Set Reference Voltage Select Mode

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd Instruction: Set Reference Voltage Register

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	x	EV5	EV4	EV3	EV2	EV1	EV0

EV5	EV4	EV3	EV2	EV1	EV0	EV Value
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

9.1.18 Select LCD Bias

This instruction selects LCD bias ratio for the internal voltage follower to drive the LCD.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	0	B2	B1	B0

B2	B1	B0	LCD bias
0	0	0	1/5
0	0	1	1/6
0	1	0	1/7
0	1	1	1/8
1	0	0	1/9
1	0	1	1/10
1	1	0	1/11
1	1	1	1/12

9.1.19 Set COM Scan Direction

This instruction selects the COM output scanning direction and determines the LCD driver output status.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	x	x	x

SHL = 0: normal direction (COM0 ~ COM127)

SHL = 1: reverse direction (COM127 ~ COM0)

9.1.20 Set SEG Scan Direction

This instruction changes the relationship between the DDRAM column address and the segment driver. The SEG scan direction can be reversed by this instruction. This feature makes IC layout more flexible for LCD module assembly.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0: normal direction (SEG0 ~ SEG127)

ADC = 1: reverse direction (SEG127 ~ SEG0)

9.1.21 Oscillator ON Start

This instruction enables the built-in oscillator circuit.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1

9.1.22 & 9.1.23 Power Save

ST7571 enters Power-Save mode and reduces the power consumption to the static power consumption. It returns to the normal operation mode by the Release Power Save Mode instruction.

Set Power Save Mode

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	P

P = 0: normal mode

P = 1: power-save mode (sleep mode)

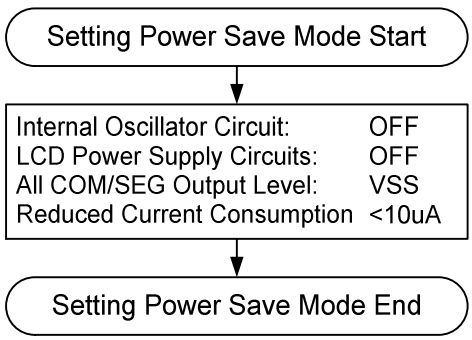


Fig. 25 Internal Procedure of Power Save

Release Power Save Mode

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	1

9.1.24 RESET

This is software reset. It resets internal registers. The software reset is different with a hardware reset. This instruction cannot initialize the LCD power supply, which is initialized by a hardware reset (refer to section 7.5 RESET CIRCUITS).

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

9.1.25 Set Display Data Length (only for 8-bit 3-Line SPI Mode)

This 2-byte instruction is used in 3-Line SPI mode only. In 3-Line SPI mode, A0 is not used and “Set Display Data Length” instruction is used to indicate the number of display data bytes which are going to be transmitted. The 1st byte sets the mode, and the 2nd byte sets the data bytes, which will be written, into internal counter. The next byte after the display data string is handled as instruction. The 3-Line SPI mode supports write-access only.

The 1st Instruction: Set Display Data Length Command (Only Write Mode)

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
x	x	1	1	1	0	1	0	0	0

The 2nd Instruction: Set Display Data Length Counter

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
x	x	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	Display Data Length
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	1	254
1	1	1	1	1	1	1	0	255
1	1	1	1	1	1	1	1	256

9.1.26 NOP

No operation

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

9.1.27 Extension Command Set1

This instruction enables the extension command set-1.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	1	1	0	1

9.1.28 Extension Command Set2

This instruction enables the extension command set-2.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	1	0	0	0	1

9.1.29 Extension Command Set3

This instruction enables the extension command set-3.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	1	0	1	1

Extension Command Set 1

After entering the extension mode-1, the extension command set-1 is enabled. These commands are valid only in this mode. Always remember to return back to normal mode for correct operation.

Increase Vop Offset

This instruction increases the Vop offset (Vof[4:0]) by 1.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	0	0	0	1

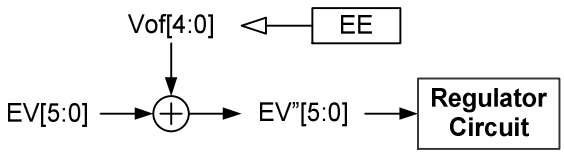
Decrease Vop Offset

This instruction decreases the Vop offset (Vof[4:0]) by 1.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	0	0	1	0

Fine Tune Vop

The “Increase Vop Offset” and “Decrease Vop Offset” instructions fine tune the voltage of Vop. The relation is shown below:



Note:

1. The range is limited. If continuously setting “Increase Vop Offset”, Vof[4:0] will increase. When Vof[4:0] is 0x0F and followed by a “Increase Vop Offset” command, Vof[4:0] will become 0x10. As the result, Vop changes from +15 step to -16 step. Software programmer should add a software protection to prevent that an operator maybe presses the “Increase Button” too many times accidentally.
2. EV”[5:0] = EV[5:0] + Vof[4:0] and EV”[5:0] ≤ 0x3F. If EV[5:0] + Vof[4:0] > 0x3F, EV”[5:0] will truncate the invalid bit.

Return to Normal Mode

This instruction returns IC into normal mode and the general commands are available.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0

Extension Command Set 2

After entering the extension mode-2, the extension command set-2 is enabled. These commands are valid only in this mode. Always remember to return back to normal mode for correct operation.

Disable auto-Read

This instruction disables the EEPROM auto-read function and lets the related registers can be set manually.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	0

Enter EEPROM Mode

This instruction enters EEPROM mode.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	0	1	1

Enable Read Mode

This instruction enables the manually-read function.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	0	0	0

Set Read Pulse

This instruction generates one read cycle to read the contents in EEPROM.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	0	0	0	1

Exit EEPROM Mode

This instruction exits EEPROM mode.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	1	1

Enable ERASE Mode

This instruction enables manually-erase function.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	0	1	0

Set ERASE Pulse

This instruction generates one erase cycle to erase the contents in EEPROM.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	0	1	0	1

Enable Write Mode

This instruction enables manually-write function.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	0	1	0	1

Set Write Pulse

This instruction generates one write cycle to write parameters into EEPROM.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	1	0	1	0

Return to Normal Mode

This instruction returns IC into normal mode and the general commands are available.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0

Extension Command Set 3

After entering the extension mode-3, the extension command set-3 is enabled. These commands are valid only in this mode. Always remember to return back to normal mode for correct operation.

Set Color Mode

This instruction controls the gray-scale mode.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	0	0	B/G

Flag	Description
B/G	B/G=0 : IC is in Gray-Scale mode (write 2-byte for 8-pixel). B/G=1 : IC is in Black/White mode (write 1-byte for 8-pixel).

Return to Normal Mode

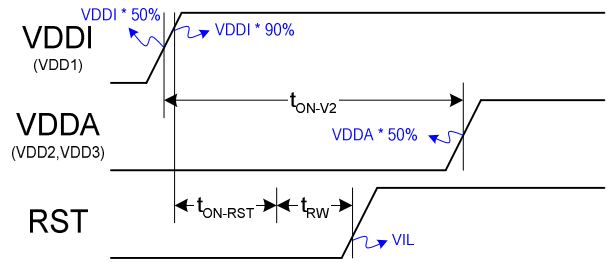
This instruction returns IC into normal mode and the general commands are available.

A0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0

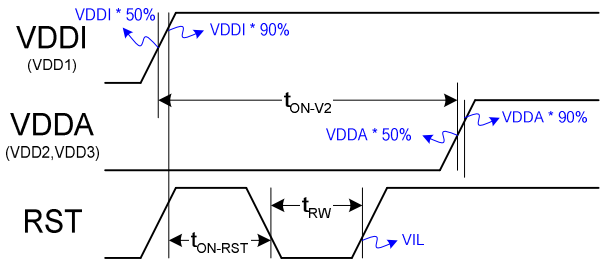
10. OPERATION FLOW

10.1 Power ON Sequence

Case 1: RST=L while Power ON (Recommended)



Case 2: RST=H while Power ON



Timing Requirement:

Item	Symbol	Requirement	Note
RST input time	t_{ON-RST}	Recommend $0 \le t_{ON-RST} \le 50$ ms	l After VDDI is stable, a successful hardware reset by RST is required. l RST=L can be input at any time after power is stable. l t_{RW} & t_R should match the timing specification of RST. l The recommended time just prevents abnormal display (customer can use Case 1 instead).
VDD2 power delay	t_{ON-V2}	$0 \le t_{ON-V2}$	l Applying VDDI and VDDA in any order will not damage IC. l If VDDI and VDDA are separated, it is recommend to turn ON VDDI first, followed by a success hardware reset, and the VDDA is the last one.

Note:

1. IC will NOT be damaged if either VDDI or VDDA is OFF while another is ON.
   The specification listed below just wants to prevent abnormal display on LCD module.
2. Power stable is defined as the time that the later power (VDDI or VDDA) reaches 90% of its rated voltage. The power stable time depends on system and the time is not included in this specification (customer should consider this factor).
3. It is recommended to keep the interface pins (A0, RWR, ERD, CSB and DB[7:0]), except RST, at “High” level before the internal reset procedure is finished.
4. Internal VD1 generator will generate VD1 when DCPS is set to “L”. The VD1 rising time is controlled by ITO resistance and the external capacitor. Before VD1 is stable, internal logic state is unstable and large current maybe occurred. This current will not damage IC. This period can be reduced by reduce the ITO resistance or the external capacitor value.

10.2 Referential Operation Flow : Initializing with internal power system

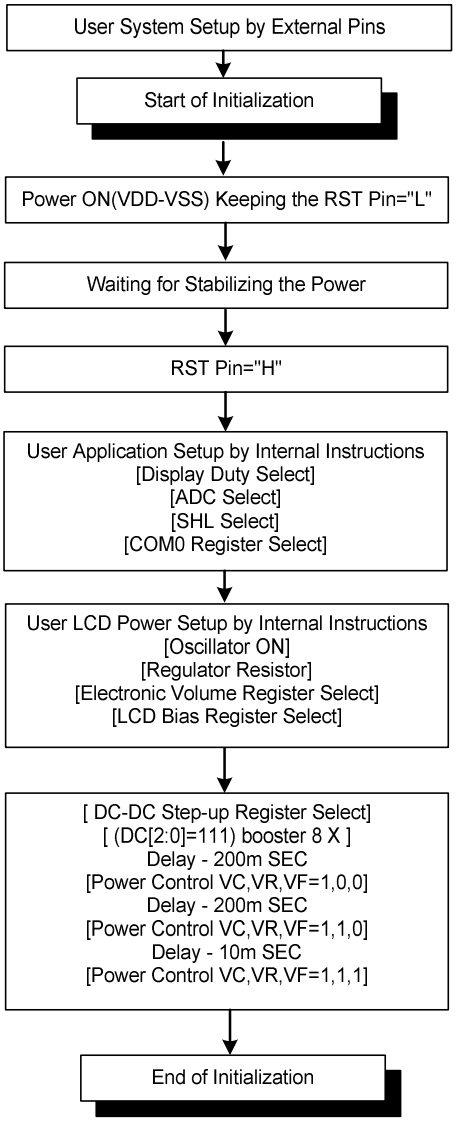


Fig. 26 Initializing with the Built-in Power Supply Circuits

Referential Initial Code

The referential initial code is shown below. In order to be compatible with ST7541, some instructions are still included, such as the instructions with gray background). These instructions will not operate in ST7571 (just like NOP).

```
void Initial_ST7571(void)
{
      Reset( );
       Delay (100);                          // Delay 100ms for stable VDD1/VDD2/VDD3
       Write(COMMAND, 0xAE);                 // Display OFF
       Write(COMMAND, 0x38);                 // MODE SET
       Write(COMMAND, 0xB8);                 // FR=1011 => 85Hz
                                             // BE[1:0]=1,0 => booster efficiency Level-3
       Write(COMMAND, 0xA1);                 // ADC select, ADC=1 =>reverse direction
       Write(COMMAND, 0xC8);                 // SHL select, SHL=1 => reverse direction
       Write(COMMAND, 0x44);                 // Set initial COM0 register
       Write(COMMAND, 0x00);                 //
       Write(COMMAND, 0x40);                 // Set initial display line register
       Write(COMMAND, 0x00);                 //

       Write(COMMAND, 0xAB);                 // OSC. ON
       Write(COMMAND, 0x67);                 // DC-DC step up, 8 times boosting circuit
       Write(COMMAND, 0x25);                 // Select regulator register(1+(Ra+Rb))
       Write(COMMAND, 0x81);                 // Set Reference Voltage
       Write(COMMAND, 0x23);                 // EV=35    => Vop =10.556V
       Write(COMMAND, 0x54);                 // Set LCD Bias=1/9 V0
       Write(COMMAND, 0xF3);                 // Release Bias Power Save Mode
       Write(COMMAND, 0x04);                 //

       Write(COMMAND, 0x93);                 // Set FRC and PWM mode (4FRC & 15PWM)
       Write(COMMAND, 0x2C);                 // Power Control, VC: ON    VR: OFF    VF: OFF
       Delay (200);                          // Delay 200ms
       Write(COMMAND, 0x2E);                 // Power Control, VC: ON    VR: ON    VF: OFF
       Delay (200);                          // Delay 200ms
       Write(COMMAND, 0x2F);                 // Power Control, VC: ON     VR: ON    VF: ON
       Delay (10);                           // Delay 10ms
       Write(COMMAND, 0xAF);                 // Display ON
}
```

Note:

The initial code is for reference only. An optimized initial code should be checked on customer's system and LCD module.

10.3 Referential Operation Flow : Displaying Data

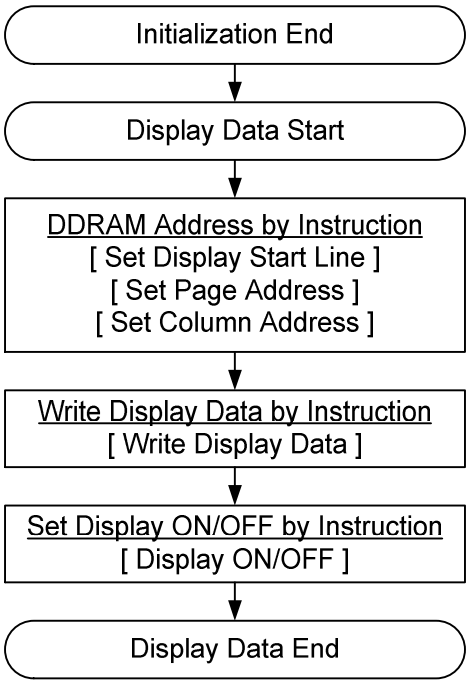
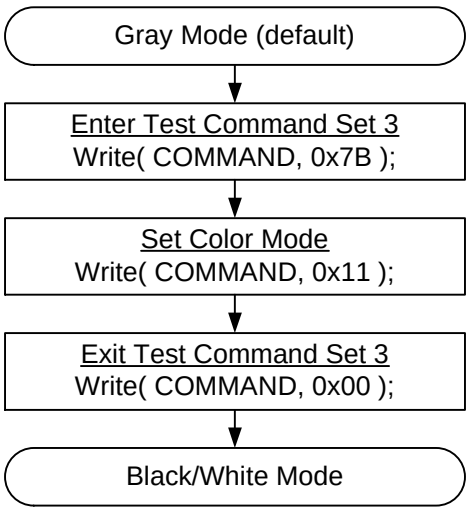


Fig. 27 Data Displaying Flow

10.4 Referential Operation Flow : Set Color Mode (Black/White Mode)



10.5 Referential Operation Flow : Power-OFF

By setting 0xA9, ST7571 will go into power save mode. The LCD driving outputs are fixed to VSS, built-in power circuits are turned OFF and a discharge process starts.

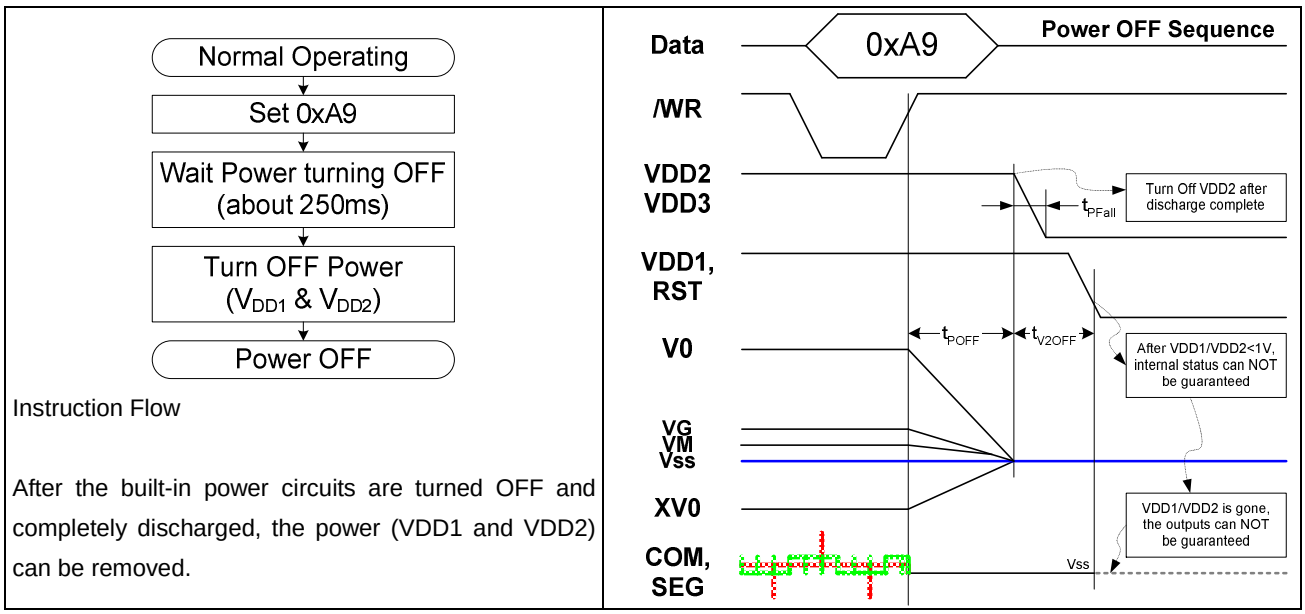


Fig. 28 Power off instruction flow

Note:

1. t_{POFF}: Internal Power discharge time. => 250ms (max).
2. t_{V2OFF}: Period between VDD1 and VDD2 OFF time. => 0 ms (min).
3. It is NOT recommended to turn VDD1 OFF before VDD2. Without VDD1, the internal status cannot be guaranteed and internal discharge-process maybe stopped. The un-discharged power maybe flows into COM/SEG output(s) and the liquid crystal in panel maybe polarized.
4. IC will NOT be damaged if either VDD1 or VDD2 is OFF while another is ON.
5. The timing is dependent on panel loading and the external capacitor(s).
6. The timing in these figures is base on the condition that: LCD Panel Size = 1.8” and C=1uF.
7. When turning VDD2 OFF, the falling time should follow the specification:
   300ms ≤ t_{PFall} ≤ 1sec

10.6 Referential Operation Flow : Burning EEPROM

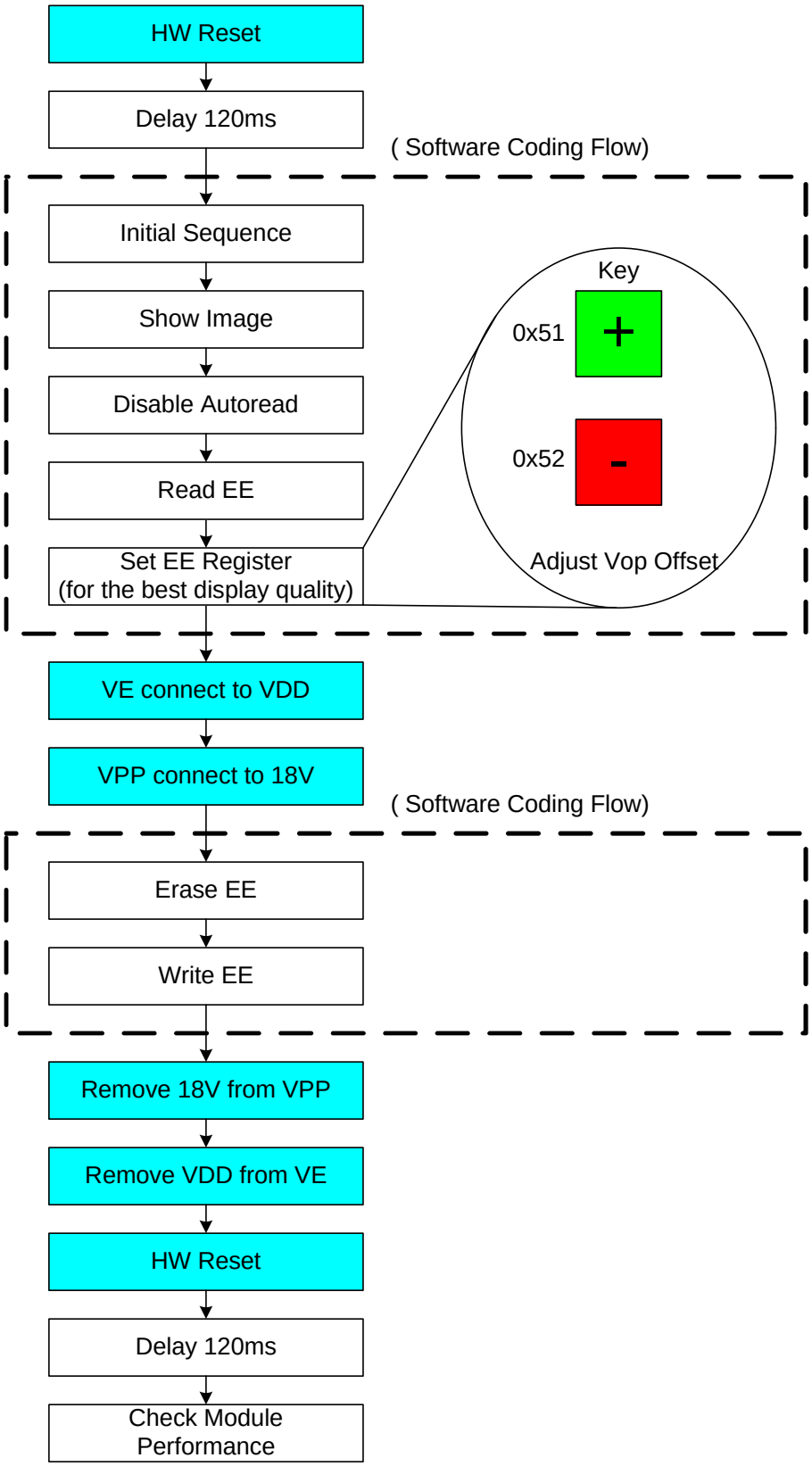


Fig. 19 EE Burning flow chart

Referential Software Functions

```
void Disable_autoread(void)
{
        Write(COMMAND, 0xD1);                   //Enter test command set 2
        Write(COMMAND, 0xAA);                   //Disable auto-read
        Write(COMMAND, 0x00);                   //Enter normal mode
}

void Read_EE (void)
{
        Write(COMMAND, 0xD1);                   //Enter test command set 2
        Write(COMMAND, 0xAA);                   //Auto-read disable
        Write(COMMAND, 0x13);                   //Enter EEPROM mode
        Write(COMMAND, 0x20);                   //Enable read mode
        Delay(200);                             //Delay 200ms
        Write(COMMAND, 0x71);                   //Set read pulse
        Delay(200);                             //Delay 200ms
        Write(COMMAND, 0x83);                   //Exit EEPROM mode
        Write(COMMAND, 0x00);                   //Enter normal mode
}

void Set_EE _Register (void)
{     // Adjust Vop offset here
// Command 0x51 and 0x52 can be set 16 times for adjusting a suitable Vop
// Maxmum adjusting ranges are +/-16 levels.
        Write(COMMAND, 0xFD);                   //Enter test command set 1
        Write(COMMAND, 0x8C);                   //Set Vop offset highest bit Vop_j[4]=0
        Write(COMMAND, 0x90);                   //Set Vop offset    Vop_j[3:0]=0
        Write(COMMAND, 0x51);                   //0x51 for increase Vop offset by 1 level
        or
        Write(COMMAND, 0x52);                   //0x52 for decrease Vop offset by 1 level
        Write(COMMAND, 0x00);                   //Enter normal mode
}
```

```
void Erase_EE (void)
{
        Write(COMMAND, 0xD1);                   //Enter test command set 2
        Write(COMMAND, 0x13);                   //Enter EEPROM mode
        Write(COMMAND, 0x4A);                   //Enable erase mode
        Delay(200);                             //Delay 200ms
        Write(COMMAND, 0x55);                   //Set erase pulse
        Delay(200);                             //Delay 200ms
        Write(COMMAND, 0x83);                   //Exit EEPROM mode
        Write(COMMAND, 0x00);                   //Enter normal mode
}

void Write_EE (void)
{
        Write(COMMAND, 0xD1);                   //Enter test command set 2
        Write(COMMAND, 0x13);                   //Enter EEPROM mode
        Write(COMMAND, 0x35);                   //Enable write mode
        Delay(200);                             //Delay 200ms
        Write(COMMAND, 0x6A);                   //Set write pulse
        Delay(200);                             //Delay 200ms
        Write(COMMAND, 0x83);                   //Exit EEPROM mode
        Write(COMMAND, 0x00);                   //Enter normal mode
}
```

11. LIMITING VALUES

In accordance with the Absolute Maximum Rating System; see notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Digital Power Supply Voltage	VDD1	–0.3 ~ 3.6	V
Analog Power supply voltage	VDD2	–0.3 ~ 3.6	V
Analog Power supply voltage	VDD3	–0.3 ~ 3.6	V
LCD Power supply voltage	V0-XV0	–0.3 ~ 15	V
LCD Power supply voltage	VG, VM	–0.3 ~ VDD2	V
Input Voltage	VIN	–0.3 ~ VDD1+0.3	V
Operating temperature	TOPR	–30 to +85	°C
Storage temperature	TSTR	–40 to +125	°C

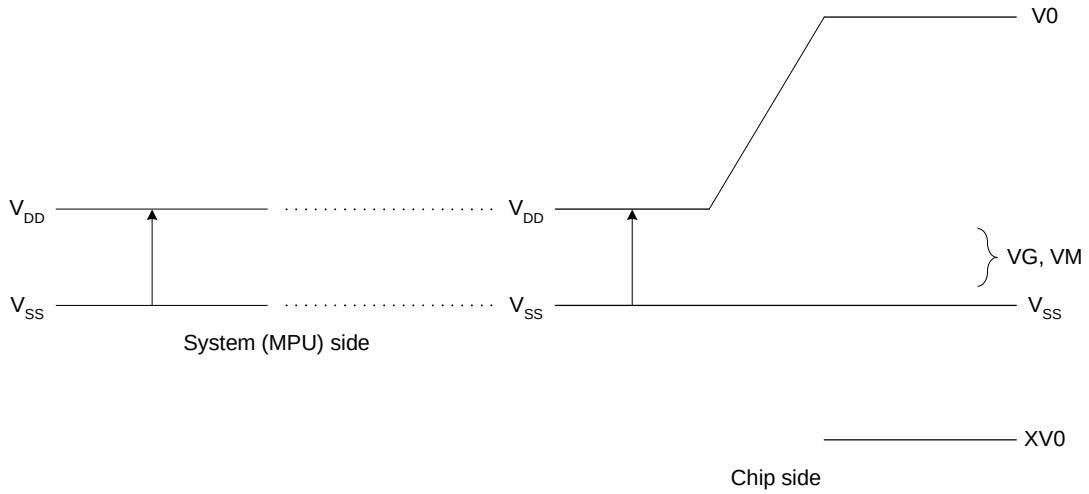


Fig. 30

Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.
3. Insure the voltage levels of V0, VDD2, VG, VM, VSS and XV0 always match the correct relation:
   V0 ≥ VDD2 > VG > VM > VSS ≥ XV0

12. DC CHARACTERISTICS

Item	Symbol	Condition		Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Digital Operating Voltage	VDD1			1.7	—	3.4	V	VDD1
Analog Operating Voltage	VDD2			2.6	—	3.4	V	*2
Analog Operating Voltage	VDD3			2.6	—	3.4	V	*2
High-level Input Voltage	VIHC			0.7 x VDD1	—	VDD1	V	*1
Low-level Input Voltage	VILC			VSS	—	0.3 x VDD1	V	*1
Input leakage current	ILI	VIN = VDD1 or VSS		–1.0	—	1.0	μA	*3
Output leakage current	ILO	VIN = VDD1 or VSS		–3.0	—	3.0	μA	*4
LCD Driver ON Resistance	R_{ON}	Ta =25°C	Vop=12V ΔV=1.2V	—	0.7		KΩ	SEGn COMn *5
			VG=2V ΔV=0.2V	—	0.7			
Frame Frequency	f_{FR}	VDD1~3 = 2.8V, 1/129 duty, N-line=0, Ta = 25°C FR[3:0]=0000(77Hz)		70	77	84	Hz	

1. **VSS1 = VSS2 = VSS3 = 0 V unless otherwise specified.**

Bare Dice Current Consumption

Using Internal Power Circuits and applying external operating voltage (VDD1, VDD2 & VDD3).

Item	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display ON Pattern: SNOW	ISS	VDD1=1.8V, VDD2=VDD3=2.8V Ta = 25°C, Vop=10.5V, 8X booster, 1/9 Bias, N-Line=0x01, 1/129 duty, FR[3:0]=0000(77Hz)	—	450	600	μA	*6
Power Save	ISS	VDD1=1.8V, VDD2=VDD3=2.8V , Ta = 25°C	—	5	10	μA	*6

Note:

1. The A0, D0 to D5, D6 (SI), D7 (SCL), /RD (E), /WR (R/W), CSB, IMS, OSC, P/S, /DOF, RESB, and MODE terminals.
2. Used by internal analog circuits.
3. The A0, /RD (E), /WR, /(R/W), CSB, IMS, OSC, P/S, /DOF, RESB and MODE terminals.
4. Applies when the D0 to D5, D6 (SI), D7 (SCL) terminals are in a high impedance state.
5. These are the resistance values for when a specified voltage difference is applied between the output terminals (SEGn/COMn) and the various power supply terminals (V0, XV0, VG & VM).
   $R_{ON} = \Delta V / \Delta I$ ....(ΔV is the specified voltage difference; ΔI is the current when applying ΔV between output and power)
6. It indicates the current consumed by Bare Chip alone.

Internal Power Circuits

The operation ranges of the internal power circuits are shown below:

Item	Symbol	Condition	Rating			Units	Applicable Pin
			Min.	Typ.	Max.		
Vop	V0-XV0		—	—	15	V	
Voltage follower output voltage	VM		0.7	VG/2	VDD2-0.7	V	
VG output voltage range	VG		1.8	—	VDD2	V	

Internal Power Application Notes

- Positive Booster: ***(VDD2 x 8 x BE) ≥ V0*** or ***(VDD2 x 8 x BE) ≥ Vop***;
- Negative Booster: ***[–VDD2 x (8 – 1) x BE] ≤ XV0*** or ***[VDD2 x (8 – 1) x BE] ≥ (Vop – VG)***, where VG = Vop x 2 / N;
- Vop requirement: ***[VDD2 x (8 – 1) x BE] ≥ [Vop x (N – 2) / N]*** or ***[Vop ≤ VDD2 x (8 – 1) x BE x N / (N – 2)]***.
- "8" is the booster stage and BE is the booster efficiency. Actual BE should be determined by module loading and ITO resistance value.
- 1.8V ≤ VG < VDD2. Recommend VG setting is: (VDD2-VG) = 0.5~0.8V.
- VM=VG/2 and 0.7V ≤ VM < VDD2.
- The worse condition should be considered. Furthermore, it should reserve some range for the temperature compensation and the contrast control (for end-customer).

Internal Power Application Summary (Recommend LCD Module Setting)

For quick reference, the following table lists some recommended settings for LCD module.

VDD1=1.8V, VDD2=2.8V, N-Line=12 (0x0A), Panel Size=1.5"

Duty	Vop	Bias
1/129	10V ~ 12V	1/9
1/81	9V ~ 11V	1/9
1/65	8.5V ~ 10.5V	1/9

Note:

1. It is recommended to reserve some range for user adjustment and temperature effect.
2. The value listed above is in the IC point of view. The liquid crystal display status should be checked by customer.

13. TIMING CHARACTERISTICS

System Bus Write Characteristics

8080 Series MPU

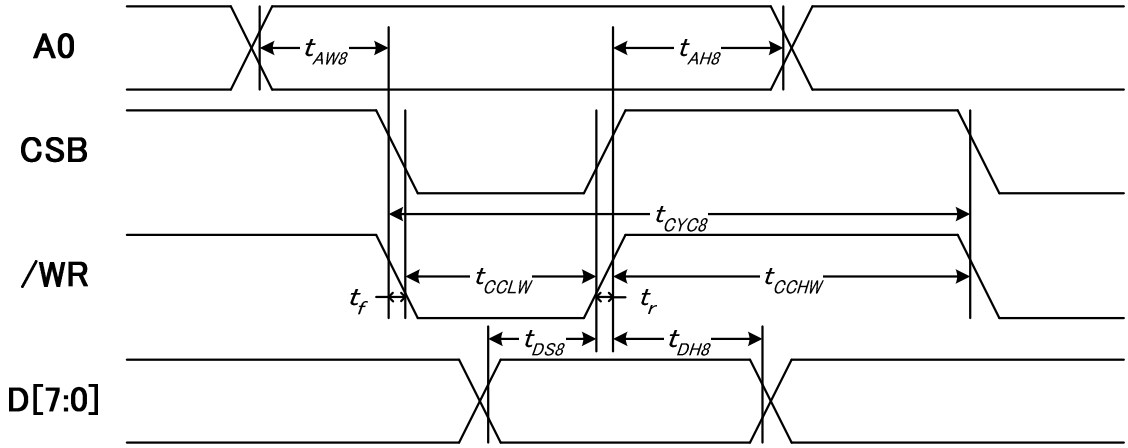


Fig. 31

(VDD1 = 1.8V~3.3V, Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time	/WR	tCYC8		500	—	
Write L pulse width		tCCLW		250	—	
Write H pulse width		tCCHW		250	—	
WRITE Data setup time	DB[7:0]	tDS8		80	—	
WRITE Data hold time		tDH8		30	—	

- The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC8 – tCCLW – tCCHW) is specified.
- All timing is specified using 20% and 80% of VDD1 as the reference.
- tCCLW is specified as the overlap between CSB being “L” and /WR being at the “L” level.

6800 Series MPU

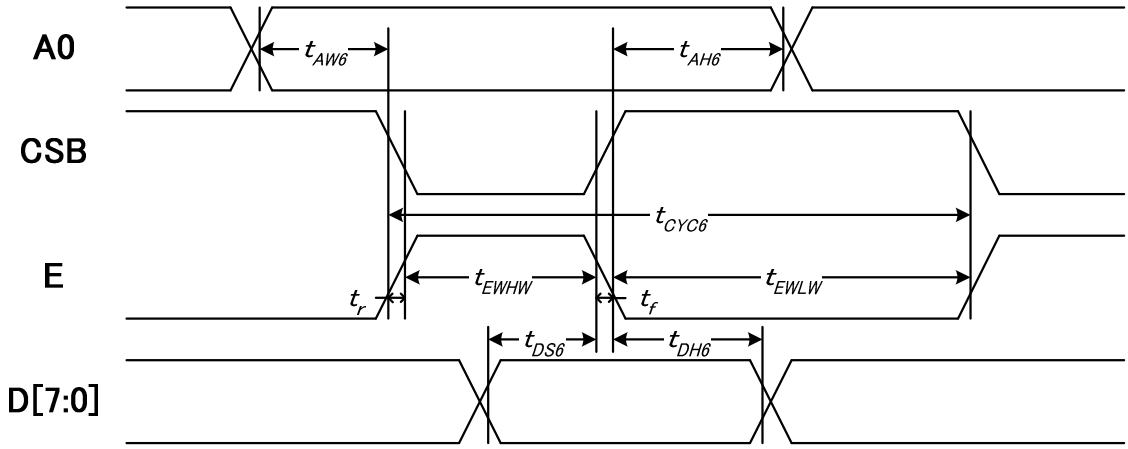


Fig. 32

(VDD1 = 1.8V~3.3V, Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time	E	tCYC6		500	—	
Enable L pulse width (Write)		tEWLW		250	—	
Enable H pulse width (Write)		tEWHW		250	—	
WRITE Data setup time	DB[7:0]	tDS6		80	—	
WRITE Data hold time		tDH6		30	—	

- The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC6 – tEWLW – tEWHW) is specified.
- All timing is specified using 20% and 80% of VDD1 as the reference.
- tEWLW is specified as the overlap between CSB being “H” and E being “L”.
- R/W signal is always “H”.

Serial 4-Line Interface

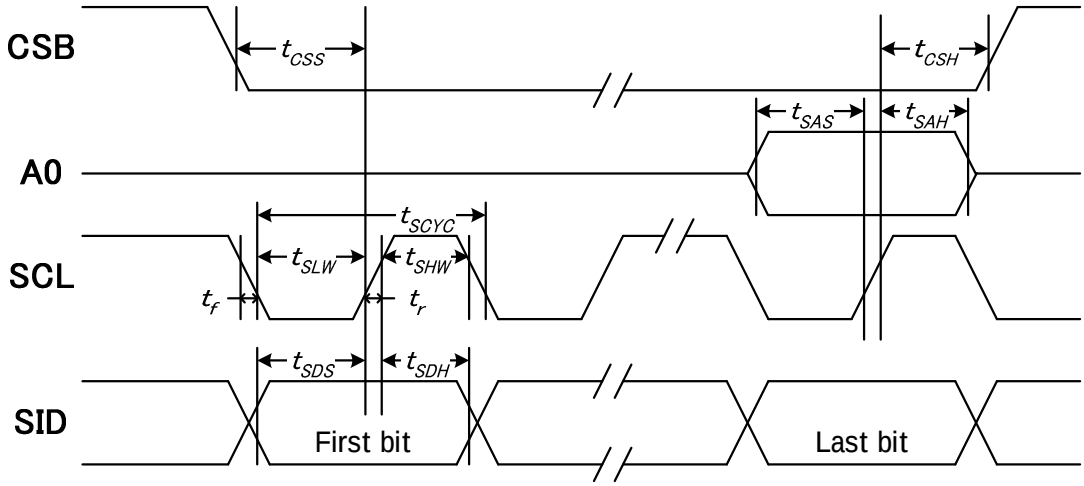


Fig. 33

(VDD1 = 1.8V~3.3V, Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		200	—	ns
SCL “H” pulse width		tSHW		80	—	
SCL “L” pulse width		tSLW		80	—	
Address setup time	A0	tSAS		60	—	
Address hold time		tSAH		30	—	
Data setup time	SID	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		100	—	

- The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
- All timing is specified using 20% and 80% of VDD1 as the standard.

Serial 3-Line Interface

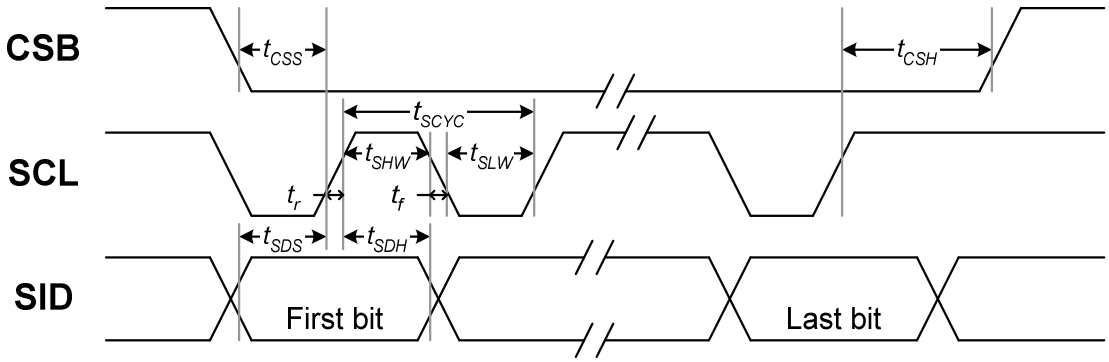


Fig. 34

(VDD1 = 1.8V~3.3V, Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		200	—	ns
SCL “H” pulse width		tSHW		80	—	
SCL “L” pulse width		tSLW		80	—	
Data setup time	SID	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		100	—	

- The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
- All timing is specified using 20% and 80% of VDD1 as the standard.

Serial I²C Interface

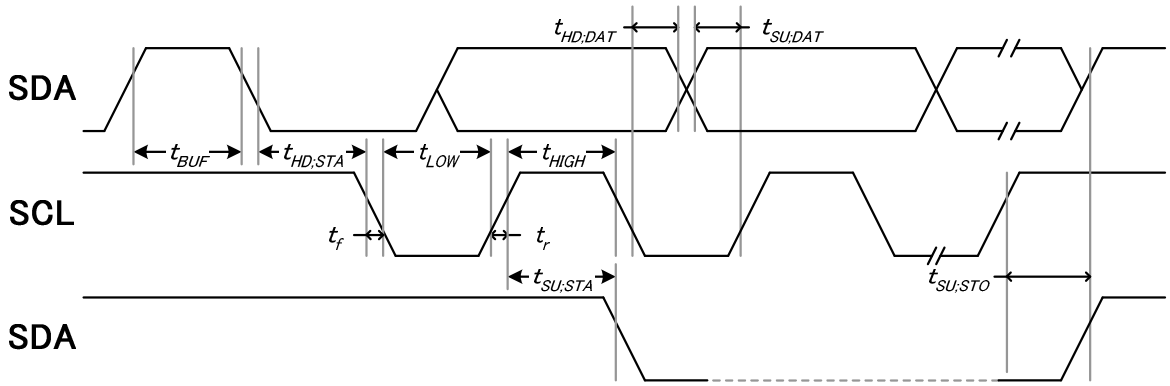


Fig. 35

(VDD1 = 3.3V, Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
SCL clock frequency	SCL	FSCLK		-	400	kHZ
SCL clock low period	SCL	TLOW		1.3	-	us
SCL clock high period	SCL	THIGH		0.6	-	us
Data set-up time	SDA	TSU;Data		100	-	ns
Data hold time	SDA	THD;Data		0	0.9	us
SCL,SDA rise time	SCL	TR		20+0.1Cb	300	ns
SCL,SDA fall time	SCL	TF		20+0.1Cb	300	ns
Capacitive load represented by each bus line		Cb		-	400	pF
Setup time for a repeated START condition	SDA	TSU;SUA		0.6	-	us
Start condition hold time	SDA	THD;STA		0.6	-	us
Setup time for STOP condition		TSU;STO		0.6	-	us
Tolerable spike width on bus		TSW		-	50	ns
BUS free time between a STOP and START condition	SCL	TBUF		1.3		us

Note:

- All timing is specified using 20% and 80% of VDD1 as the standard.
- It is recommended to operate the I²C interface with VDD1 higher than 2.6V.

Reset Timing

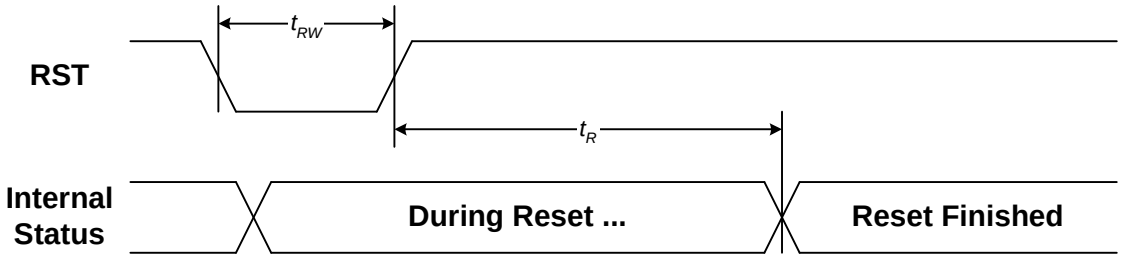


Fig. 36

(VDD1 = 1.8V~3.3V, Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		120	—	—	ms
Reset “L” pulse width	RST	tRW		2.0	—	—	us

14. EXTERNAL COMPONENTS

The pinning of the ST7571 is optimized for single plane wiring e.g. for chip-on-glass display modules.

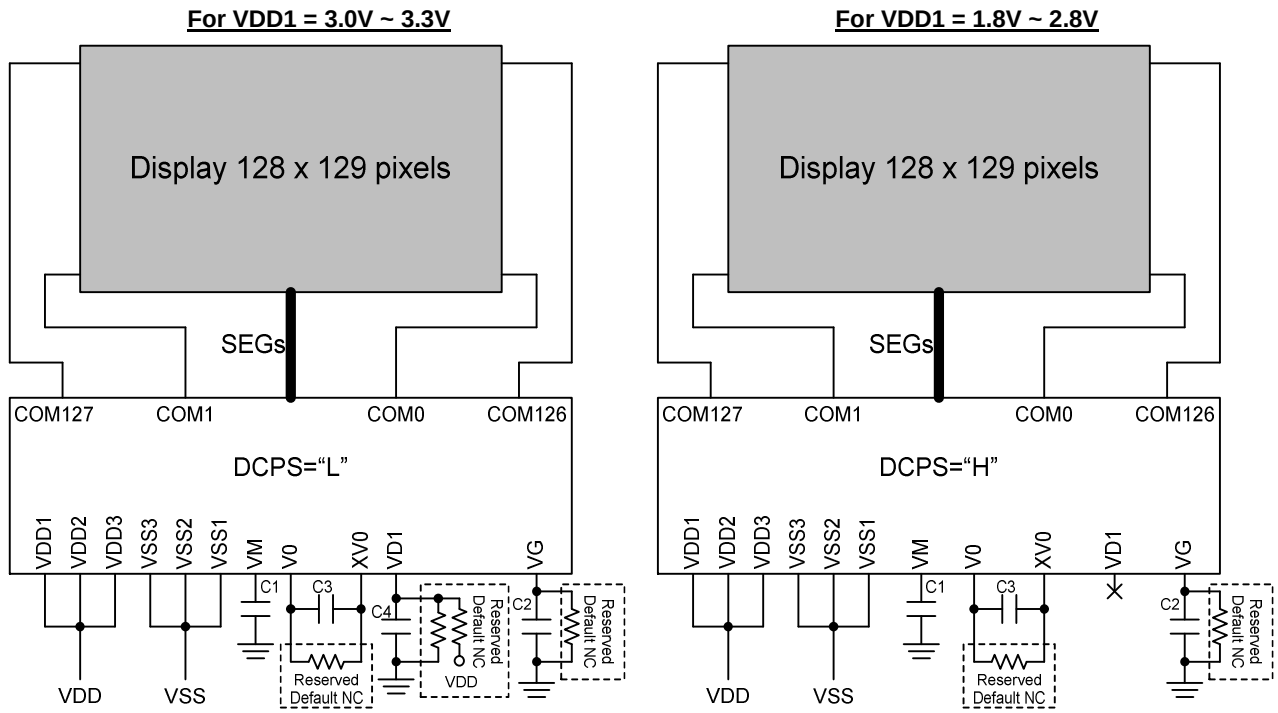


Fig. 37 External Components

Note:

1. The resistors are reserved only. Please reserve the space for them on FPC (or system).
2. The capacitors in these 2 cases are not same. C4 is not used if VDD1 is 1.8V ~ 2.8V.

Recommend Value: (for typical 1.6" LCD panel)

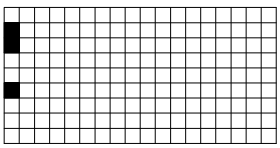
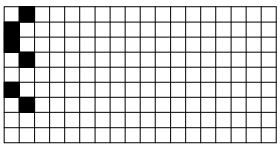
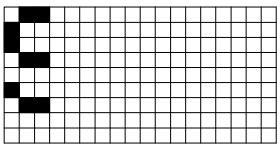
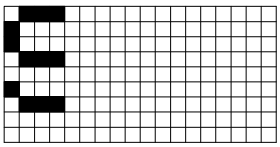
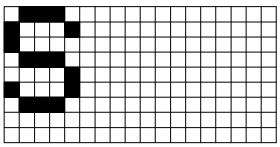
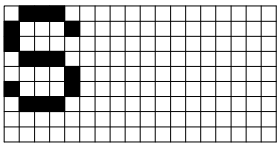
- C1~C3: 1uF ~ 4.7uF
- C4: 0.1uF ~ 1uF

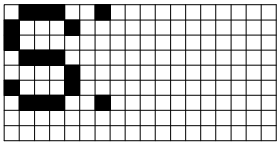
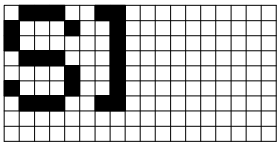
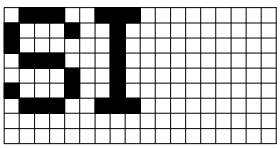
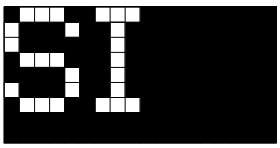
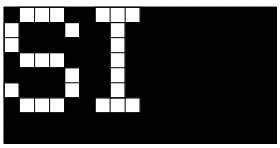
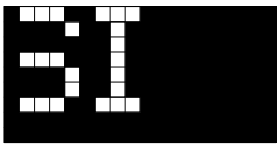
Components selection notes:

- Higher capacitor values are recommended for ripple reduction.
- In order to avoid the characteristic differences of the LCD panel. The capacitor values should be verified according to the display performance on LCD panel.
- If the display panel is larger (> 2"), higher capacitor (C1~C3) values are recommended.
- If the display panel is smaller (< 1"), lower capacitor (C1~C3) values can be used.
- The resistor is reserved for discharge in the worse case, when VDD suddenly drops to 0.

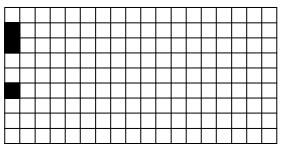
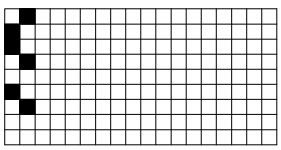
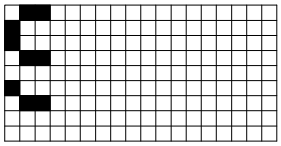
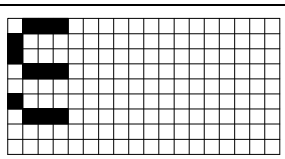
15. APPLICATION PROGRAM EXAMPLE

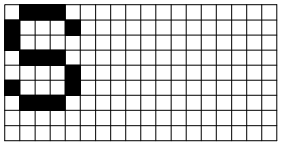
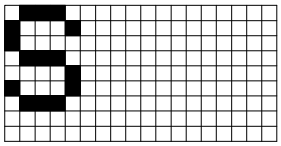
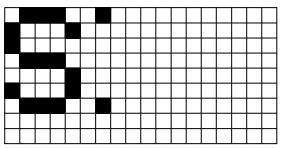
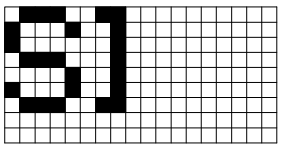
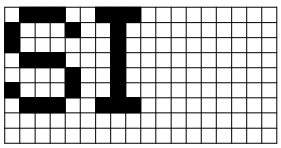
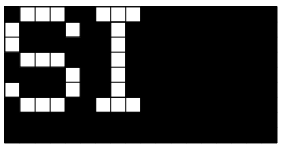
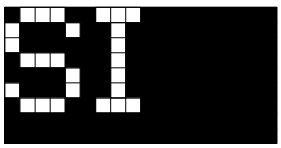
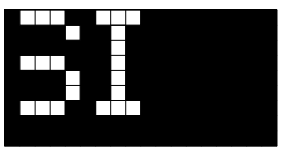
Programming example for displaying data with ST7571:

Step	Bus Status									LCD Display	Operation Description
1	A0 0 0	DB7 0 0	DB6 0 0	DB5 1 0	DB4 1 0	DB3 1 1	DB2 0 0	DB1 0 x’	DB0 0 0		Mode Set: FR[3:0]=0000; BE[1:0]=10
2	A0 0	DB7 1	DB6 0	DB5 1	DB4 0	DB3 1	DB2 0	DB1 1	DB0 1		OSC ON
3.a	A0 0	DB7 0	DB6 0	DB5 1	DB4 0	DB3 0	DB2 R2	DB1 R1	DB0 R0		Set Ra/Rb (R[2:0])
3.b	A0 0 0	DB7 1 x’	DB6 0 x’	DB5 0 EV5	DB4 0 EV4	DB3 0 EV3	DB2 0 EV2	DB1 0 EV1	DB0 1 EV0		Set contrast (EV[5:0])
3.c	A0 0	DB7 0	DB6 1	DB5 0	DB4 1	DB3 0	DB2 B2	DB1 B1	DB0 B0		Set Bias (B[2:0])
4.a	A0 0	DB7 0	DB6 0	DB5 1	DB4 0	DB3 1	DB2 1	DB1 1	DB0 1		Set Power Control Booster=ON, Regulator=ON, Follower=ON
4.b	A0 0	DB7 1	DB6 0	DB5 1	DB4 0	DB3 1	DB2 1	DB1 1	DB0 1		Display Control Display ON
5	A0 1 1	DB7 0 0	DB6 0 0	DB5 1 1	DB4 0 0	DB3 0 0	DB2 1 1	DB1 1 1	DB0 0 0		Write Data X, Y are default 0 after reset. Skip setting X & Y here.
6	A0 1 1	DB7 0 0	DB6 1 1	DB5 0 0	DB4 0 0	DB3 1 1	DB2 0 0	DB1 0 0	DB0 1 1		Write Data
7	A0 1 1	DB7 0 0	DB6 1 1	DB5 0 0	DB4 0 0	DB3 1 1	DB2 0 0	DB1 0 0	DB0 1 1		Write Data
8	A0 1 1	DB7 0 0	DB6 1 1	DB5 0 0	DB4 0 0	DB3 1 1	DB2 0 0	DB1 0 0	DB0 1 1		Write Data
9	A0 1 1	DB7 0 0	DB6 0 0	DB5 1 1	DB4 1 1	DB3 0 0	DB2 0 0	DB1 1 1	DB0 0 0		Write Data
10	A0 1 1	DB7 0 0	DB6 0 0	DB5 0 0	DB4 0 0	DB3 0 0	DB2 0 0	DB1 0 0	DB0 0 0		Write Data

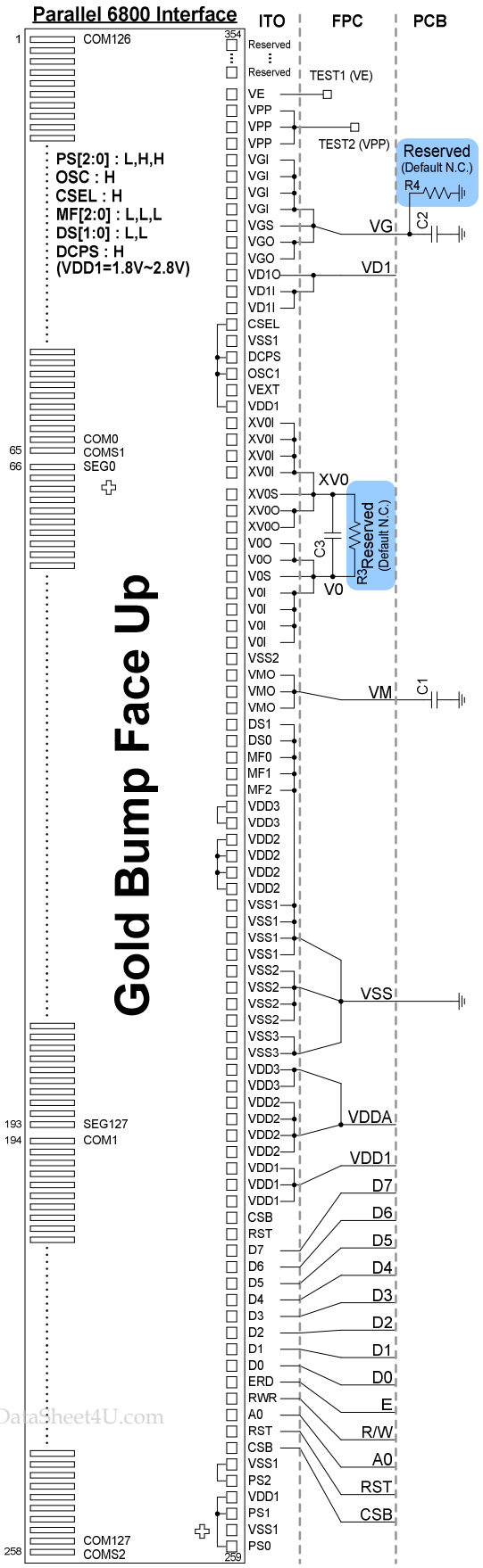
Step	Bus Status									LCD Display	Operation Description
11	A0 1 1	DB7 0 0	DB6 1 1	DB5 0 0	DB4 0 0	DB3 0 0	DB2 0 0	DB1 0 0	DB0 1 1		Write Data
12	A0 1 1	DB7 0 0	DB6 1 1	DB5 1 1	DB4 1 1	DB3 1 1	DB2 1 1	DB1 1 1	DB0 1 1		Write Data
13	A0 1 1	DB7 0 0	DB6 1 1	DB5 0 0	DB4 0 0	DB3 0 0	DB2 0 0	DB1 0 0	DB0 1 1		Write Data
14	A0 0	DB7 1	DB6 0	DB5 1	DB4 0	DB3 0	DB2 1	DB1 1	DB0 1		Display Control: Set Reverse display mode (REV=1)
15	A0 0 0	DB7 0 0	DB6 0 0	DB5 0 0	DB4 1 0	DB3 0 0	DB2 0 0	DB1 0 0	DB0 0 0		Set Column Address Set address to “00000000” X[7:0]=0x00 (X0 default is 0)
16	A0 1 1	DB7 0 0	DB6 0 0	DB5 0 0	DB4 0 0	DB3 0 0	DB2 0 0	DB1 0 0	DB0 0 0		Write Data

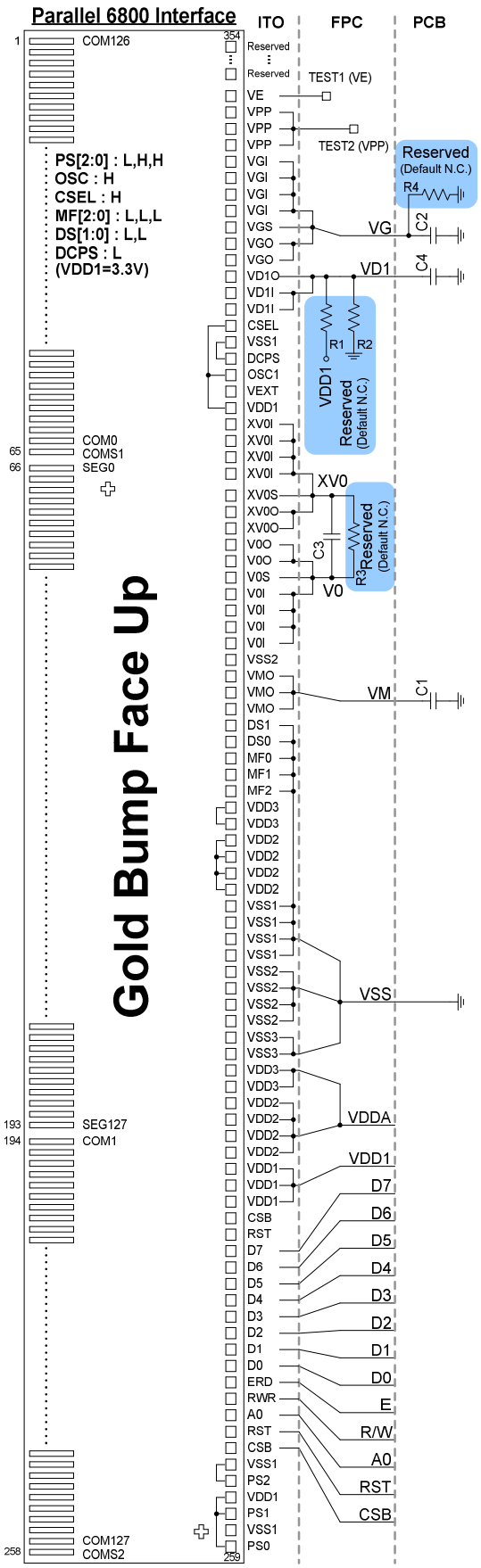
Programming example for displaying data with ST7571 (for I²C Interface):

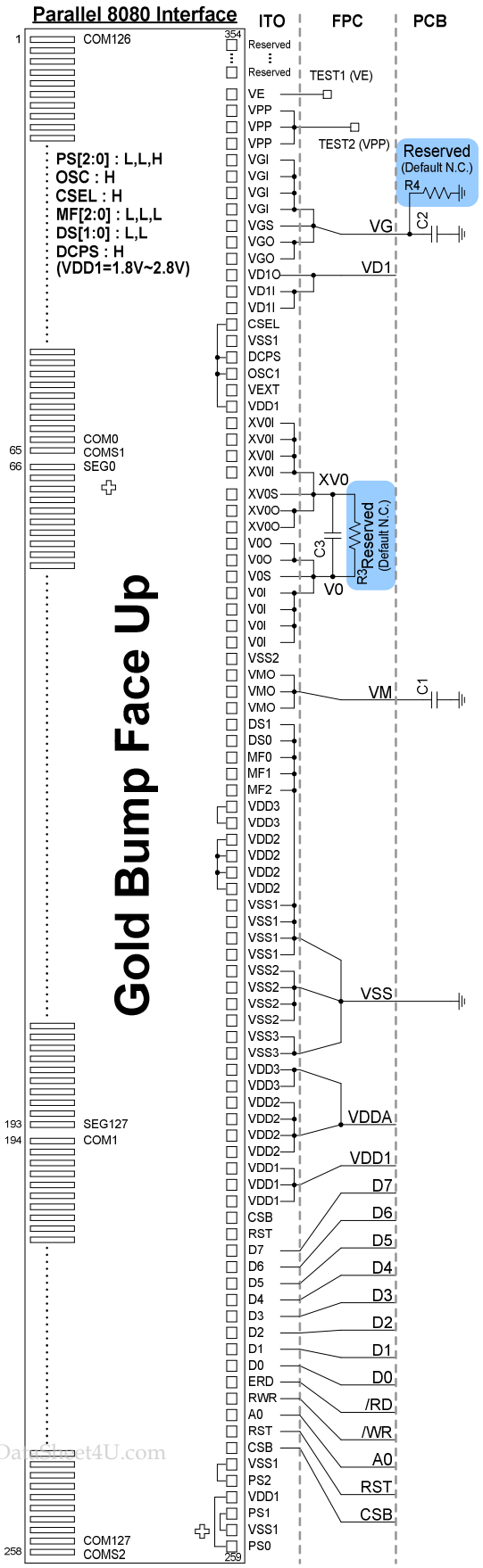
Step	Bus Status								LCD Display	Operation Description
1	I²C Interface Start									
2	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		Slave address for write
3	DB7 0	DB6 0	DB5 0	DB4 0	DB3 0	DB2 0	DB1 0	DB0 0		Set Control Byte Co=0; A0=0
4	DB7 0 0	DB6 0 0	DB5 1 0	DB4 1 0	DB3 1 1	DB2 0 0	DB1 0 x'	DB0 0 0		Mode Set: FR[3:0]=0000; BE[1:0]=10
5	DB7 1	DB6 0	DB5 1	DB4 0	DB3 1	DB2 0	DB1 1	DB0 1		OSC ON
6.a	DB7 0	DB6 0	DB5 1	DB4 0	DB3 0	DB2 R2	DB1 R1	DB0 R0		Set Ra/Rb (R[2:0])
6.b	DB7 1 x'	DB6 0 x'	DB5 0 EV5	DB4 0 EV4	DB3 0 EV3	DB2 0 EV2	DB1 0 EV1	DB0 1 EV0		Set contrast (EV[5:0])
6.c	DB7 0	DB6 1	DB5 0	DB4 1	DB3 0	DB2 B2	DB1 B1	DB0 B0		Set Bias (B[2:0])
7.a	DB7 0	DB6 0	DB5 1	DB4 0	DB3 1	DB2 1	DB1 1	DB0 1		Set Power Control Booster=ON, Regulator=ON, Follower=ON
7.b	DB7 1	DB6 0	DB5 1	DB4 0	DB3 1	DB2 1	DB1 1	DB0 1		Display Control Display ON
8	I²C Interface Start									Re-start
9	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		Slave address for write
10	DB7 0	DB6 1	DB5 0	DB4 0	DB3 0	DB2 0	DB1 0	DB0 0		Set Control Byte Co=0; A0=1
11	DB7 0 0	DB6 0 0	DB5 1 1	DB4 0 0	DB3 0 0	DB2 1 1	DB1 1 1	DB0 0 0		Write Data X, Y are default 0 after reset. Skip setting X & Y here.
12	DB7 0 0	DB6 1 1	DB5 0 0	DB4 0 0	DB3 1 1	DB2 0 0	DB1 0 0	DB0 1 1		Write Data
13	DB7 0 0	DB6 1 1	DB5 0 0	DB4 0 0	DB3 1 1	DB2 0 0	DB1 0 0	DB0 1 1		Write Data
14	DB7 0 0	DB6 1 1	DB5 0 0	DB4 0 0	DB3 1 1	DB2 0 0	DB1 0 0	DB0 1 1		Write Data

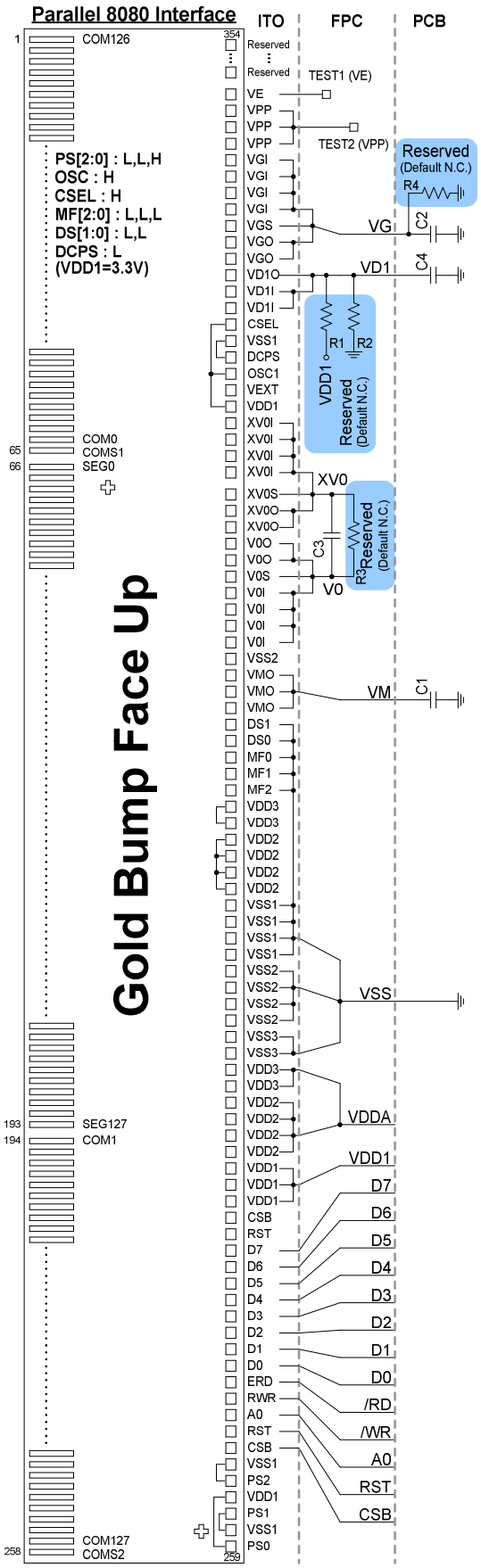
Step	Bus Status								LCD Display	Operation Description
15	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		Write Data
	0	0	1	1	0	0	1	0		
	0	0	1	1	0	0	1	0		
16	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		Write Data
	0	0	0	0	0	0	0	0		
	0	0	0	0	0	0	0	0		
17	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		Write Data
	0	1	0	0	0	0	0	1		
	0	1	0	0	0	0	0	1		
18	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		Write Data
	0	1	1	1	1	1	1	1		
	0	1	1	1	1	1	1	1		
19	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		Write Data
	0	1	0	0	0	0	0	1		
	0	1	0	0	0	0	0	1		
20	I^2C Interface Start									Re-start
21	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		Slave address for write
22	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		Set Control Byte Co=1; A0=0
	1	0	0	0	0	0	0	0		
23	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		Display Control: Set Reverse display mode (REV=1)
	1	0	1	0	0	1	1	1		
24	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		Set Control Byte Co=1; A0=0
	1	0	0	0	0	0	0	0		
25	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		Set Column Address Set address to “00000000” X[7:0]=0x00 (X0 default is 0)
	0	0	0	1	0	0	0	0		
	0	0	0	0	0	0	0	0		
26	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		Set Control Byte Co=1; A0=1
	1	1	0	0	0	0	0	0		
27	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		Write Data
	0	0	0	0	0	0	0	0		
	0	0	0	0	0	0	0	0		
28	I^2C Interface Stop									STOP I^2C transmission

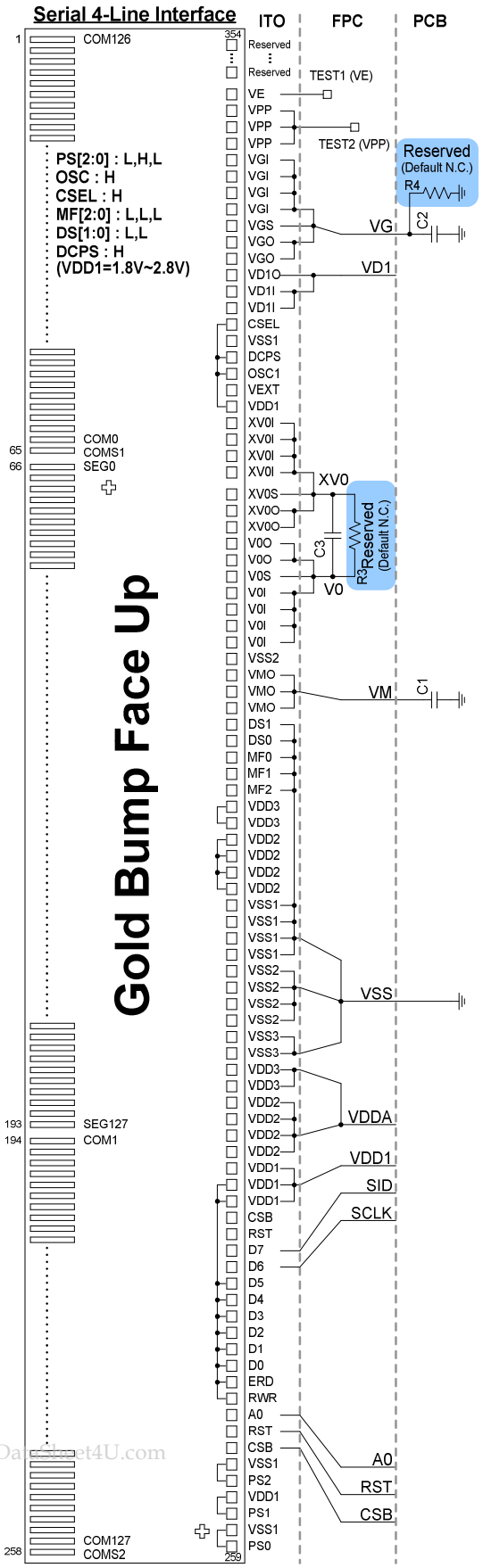
16. APPLICATION NOTES

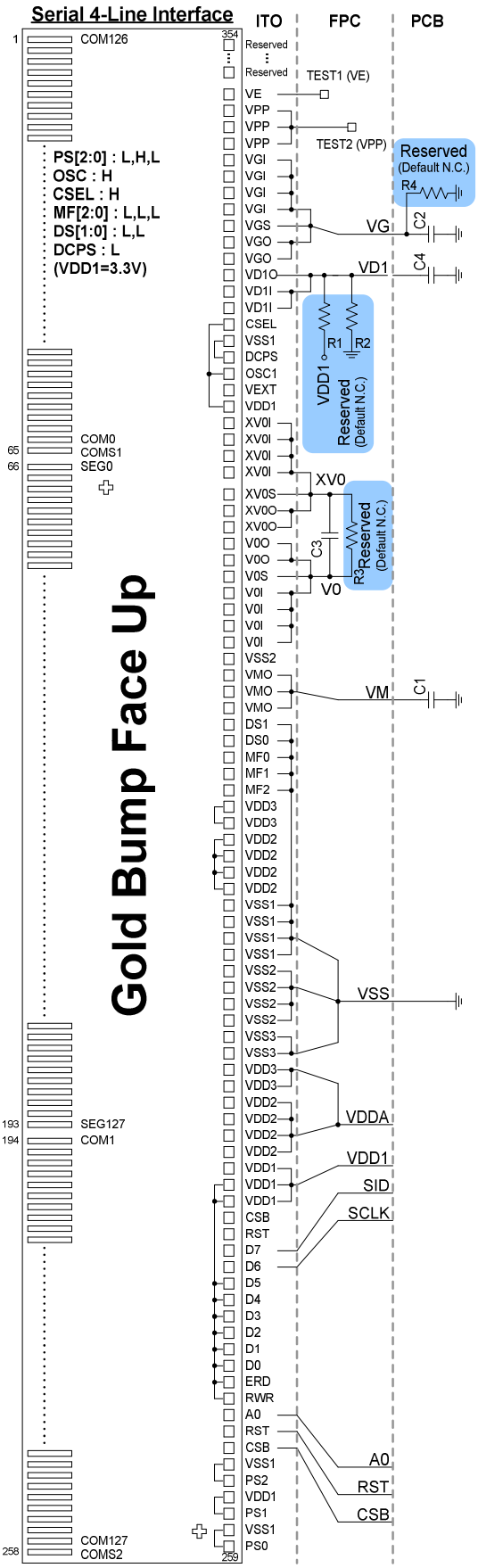


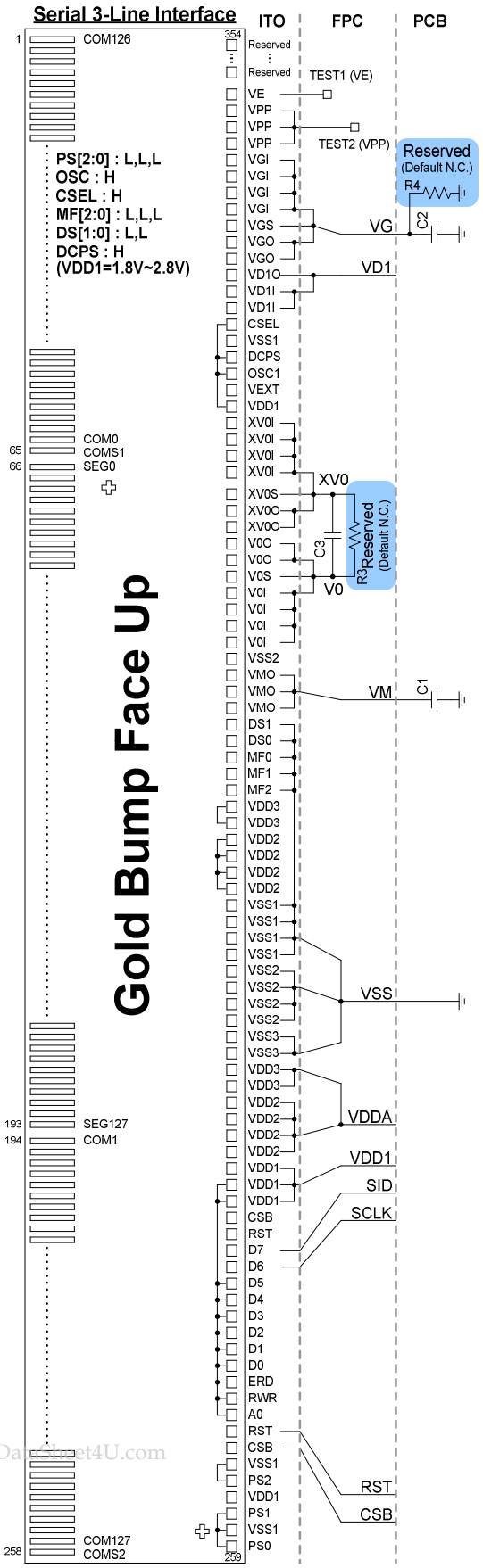


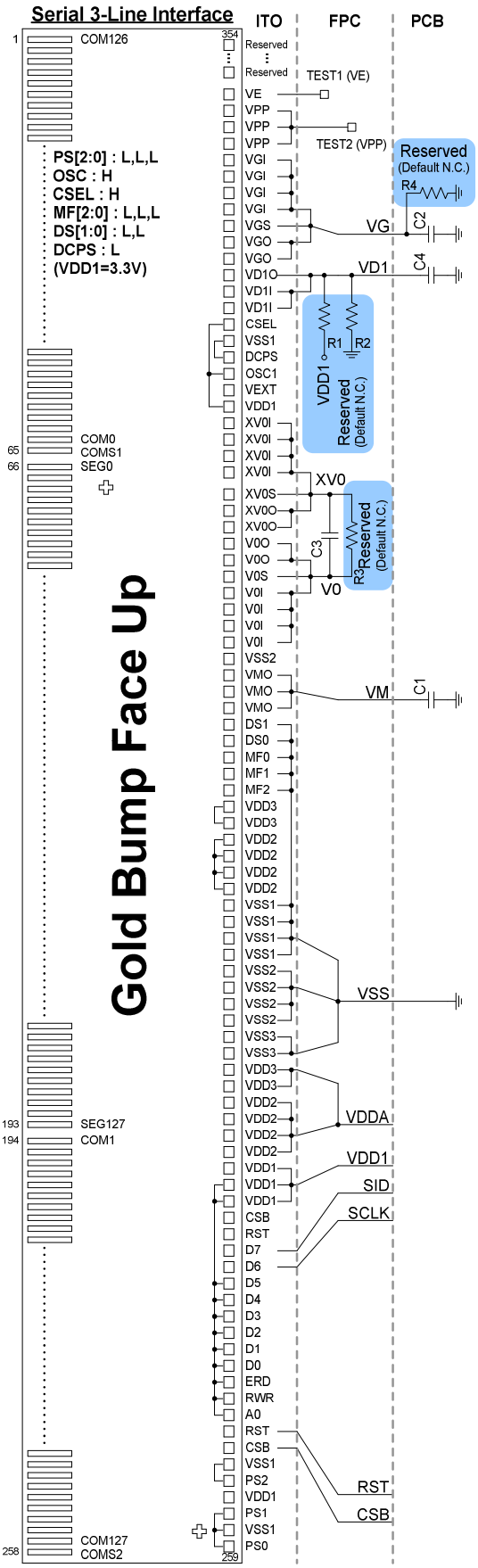


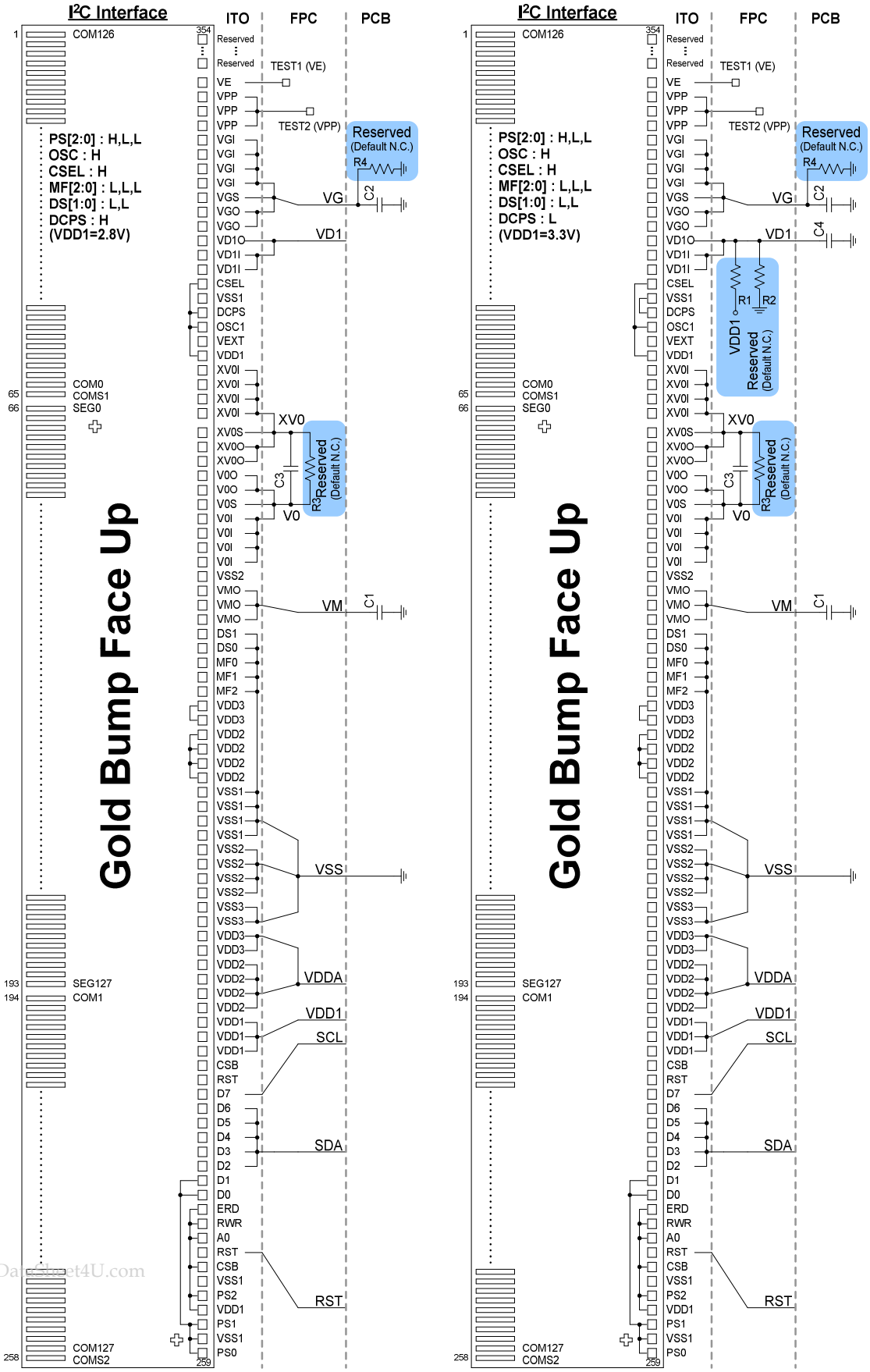












ST7571 Specification Revision History		
Version	**Date**	**Description**
1.0	2008/01/29	1. Official Release.
1.1	2008/04/02	1. Remove CSL=L setting. 2. Modify Application note 3. Add Initial code 4. Modify ITO layout reference 5. Modify 9.1.14 entire display
1.2	2008/08/08	1. Re-arrange sections for document format issue. 2. Remove one of the Power OFF flow (not easy control by customer). 3. Update recommend N-Line setting as 12-line (0x0A). 4. Rewrite some description for easy understanding and grammar issue. 5. Fix wrong Limiting Values. 6. Rewrite DC Characteristics section. Separate Internal Power Application Note for detailed description. 7. Modify Recommend LCD Vop Setting: use same bias for easy use.
1.3	2008/12/19	1. Modify limiting voltage values. 2. Modify 8080/6800 system cycle time.
1.4	2009/03/13	1. Remove reversion history before Ver. 1.0. 2. Redraw broken figures. 3. Rewrite Section 7.5 RESET CIRCUITS for easy understanding. 4. Rewrite descriptions for easy understanding. 5. Update Power ON Sequence information. 6. Add 0x8C & 0x90 to “Set_EE_Register” at Software Function Program. 7. Fix COM pad naming in figures. 8. Update external components information. 9. Match the instruction name with the instruction description.
1.4a	2009/03/16	1. Modify drawing: RST waveform at 10.1 Power ON Sequence Section (Case 2). 2. Fix typing mistakes.
1.4b	2009/05/13	1. Redraw IC outline (Page 2) and use only one view direction for IC and PAD. 2. Fix typing mistakes and rewrite descriptions for easy understanding. 3. Add ITO limitation of I^2C interface signal SDA (Page 14). 4. Fix naming issue on Page 17, 22, 35. Column Address should be X[7:0] (not Y[7:0]). 5. The default value of FR[3:0] after reset is missing in previous version. 6. Rearrange the operation flow information into one section: “Section 10. OPERATION FLOW” (Page 48). 7. Rename section “10. COMMAND DESCRIPTION” to be “10. OPERATION FLOW.” 8. Add note of I^2C: “VDD1 higher than 2.6V”. 9. Add notes to Section 14. EXTERNAL COMPONENTS. Modify the value to be a range. 10. Fix Section 15. APPLICATION PROGRAM EXAMPLE mistakes. 11. Update detailed settings into Section 16. APPLICATION NOTES: Different circuit for different VDD1 level (C4 is not used if VDD1 is 1.8V or 2.8V). Reserve 2 more resistors.

ST7571 Specification Revision History		
1.5	2009/6/25	1. Fix typing mistakes. 2. Add axis into Section 3. PAD ARRANGEMENT (COG). 3. Modify referential codes: use 8-bit format, keep delay time same as description. 4. Mark no operation instructions in initial code (Page 50). 5. Add Test Instructions into instruction table. 6. Reserve external components for special case. 7. Define the VDD2 voltage range: 2.7V ~ 3.3V (cover 2.6V ~ 3.4V).
1.5a	2009/7/21	1. Add description of Extension Command Sets.