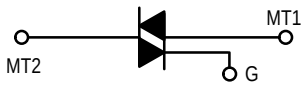
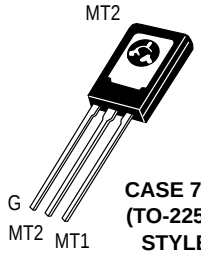
Advance Information

Sensitive Gate Triacs
Silicon Bidirectional Thyristors

MAC6071A,B*
MAC6073A,B*
MAC6075A,B*
***Motorola preferred devices**

TRIACs
4 AMPERES RMS
200 thru 600 VOLTS





CASE 77-08
(TO-225AA)
STYLE 5

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Sensitive Gate Triggering (A and B versions) Uniquely Compatible for Direct Coupling to TTL, HTL, CMOS and Operational Amplifier Integrated Circuit Logic Functions
- Gate Triggering 4 Mode — MAC6071A,B, MAC6073A,B, MAC6075A,B
- Blocking Voltages to 600 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Peak Repetitive Off-State Voltage(1) (Gate Open, T_J = 25 to 110°C)	MAC6071A,B MAC6073A,B MAC6075A,B	V_{DRM}	 200 400 600	Volts
On-State Current RMS (T_C = 85°C)		$I_{T(RMS)}$	4	Amps
Peak Surge Current (One Full cycle, 60 Hz, T_J = –40 to +110°C)		I_{TSM}	30	Amps
Circuit Fusing Considerations (t = 8.3 ms)		I^2t	3.7	A^2s
Peak Gate Power		P_{GM}	10	Watts
Average Gate Power		$P_{G(AV)}$	0.5	Watt
Peak Gate Voltage		V_{GM}	5	Volts
Operating Junction Temperature Range		T_J	–40 to +110	°C
Storage Temperature Range		T_{stg}	–40 to +150	°C
Mounting Torque (6-32 Screw)(2)		—	8	in. lb.

1. V_{DRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.
2. Torque rating applies with use of compression washer (B52200F006). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Main terminal 2 and heatsink contact pad are common.
   For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +200°C, for 10 seconds. Consult factory for lead bending options.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preferred devices are Motorola recommended choices for future use and best overall value.

MOTOROLA

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current	I_{DRM}				
(V_D = Rated V_{DRM}, gate open) (T_J = 25°C)		—	—	10	μA
(T_J = 110°C)		—	—	2.0	mA
On-State Voltage (Either Direction)	V_{TM}	—	1.3	2.0	Volts
(I_{TM} = 6 A Peak)					
Peak Gate Trigger Voltage (Continuous dc)	V_{GT}				Volts
(T_J = –40°C) (Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms)					
MT2(+), G(+); MT2(–), G(–)		0.5	0.8	1.9	
MT2(+), G(–); MT2(–), G(+)		0.5	0.8	1.9	
(T_J = 110°C)					
MT2(+), G(+); MT2(–), G(–)		0.2	0.4	0.9	
MT2(+), G(–); MT2(–), G(+)		0.2	0.4	0.9	
(T_J = 25°C)					
MT2(+), G(+); MT2(–), G(–)		0.4	0.7	1.4	
MT2(+), G(–); MT2(–), G(+)		0.4	0.7	1.4	
Holding Current (Either Direction)	I_H				mA
(T_J = –40°C) (Main Terminal Voltage = 12 Vdc, Gate Open)					
(Initiating Current = 150 mA)		0.4	2.0	10	
(T_J = 25°C)		0.2	1.0	5.0	
Latching Current (V_D = 6 V)	I_L				mA
MT2(+), G(+) (I_G = 8 mA) T_J = 25°C		—	2.0	10	
MT2(+), G(–) (I_G = 8 mA)		—	5.0	20	
MT2(–), G(–) (I_G = 8 mA)		—	1.0	10	
MT2(–), G(+) (I_G = 15 mA)		—	2.0	10	
Gate Trigger Current (Continuous dc)	I_{GT}				mA
(V_D = 12 Vdc, R_L = 100 Ohms)					
MAC6071A, MAC6073A, MAC6075A					
MT2(+), G(+) T_J = 25°C		0.4	2.0	5.0	
MT2(+), G(–)		0.4	3.0	5.0	
MT2(–), G(–)		0.4	3.0	5.0	
MT2(–), G(+)		0.8	4.5	10	
MT2(+), G(+) T_J = –40°C		0.8	3.5	10	
MT2(+), G(–)		0.8	4.5	10	
MT2(–), G(–)		0.8	5.0	10	
MT2(–), G(+)		1.6	10	20	

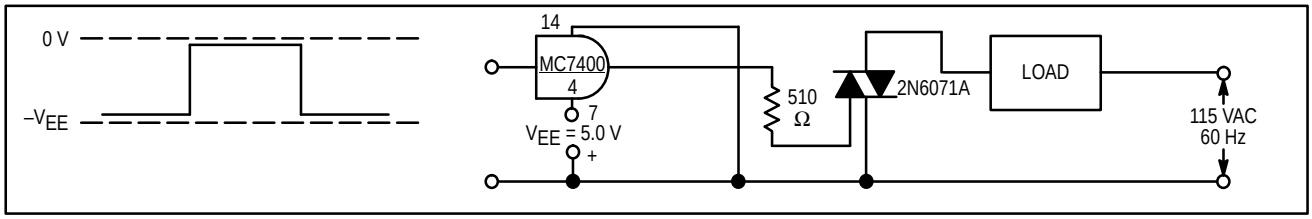
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

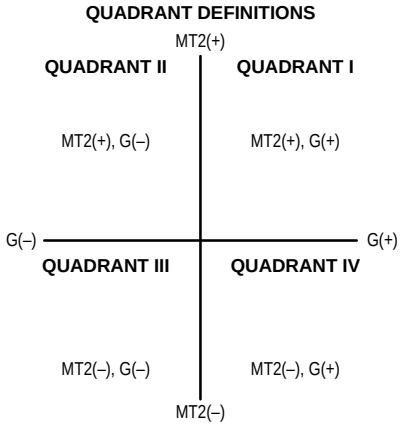
Characteristic		Symbol	Min	Typ	Max	Unit
Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, R_L = 100 Ohms) MAC6071B, MAC6073B, MAC6075B		I_{GT}				mA
MT2(+), G(+)	T_J = 25°C		0.4	1.5	3.0	
MT2(+), G(–)			0.4	2.5	3.0	
MT2(–), G(–)			0.4	2.5	3.0	
MT2(–), G(+)			0.8	3.5	5.0	
MT2(+), G(+)	T_J = –40°C		0.8	3.0	8.0	
MT2(+), G(–)			0.8	4.0	8.0	
MT2(–), G(–)			0.8	4.5	8.0	
MT2(–), G(+)			1.6	7.5	15	
Turn-On Time (Either Direction) (I_{TM} = 14 Adc, I_{GT} = 100 mAdc)		t_{gt}	—	1.5	—	μs

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Critical Rate of Rise of Off–State Voltage (V_D = 200 V, I_{TM} = 1.4 A, Commutating dv/dt = 0.5 Vμ/sec, Gate Open, T_J = 110°C, f = 250 Hz, Snubber: C_S = 0.1 μF, R_S = 56 Ω, see Figure 16)	(di/dt)c	—	2.2	—	A/ms
Critical Rate of Rise of Off–State Voltage (V_D = Rate V_{DRM}, Exponential Waveform, R_{GK} = OPEN, T_J = 110°C)	dv/dt	—	7.0	—	V/μs

SAMPLE APPLICATION:
TTL-SENSITIVE GATE 4 AMPERE TRIAC
TRIGGERS IN MODES II AND III





NOTES: For detail Digital Interfacing and Silicon Bilateral Switch (SBS) trigger application information, see the Motorola's Thyristor Data Book (DL137/D, Revision 6).

1. Interfacing Digital Circuits to Thyristor Controlled AC Loads, page 1.6–25.
2. Silicon Bilateral Switch (SBS) Applications, page 1.6–41.

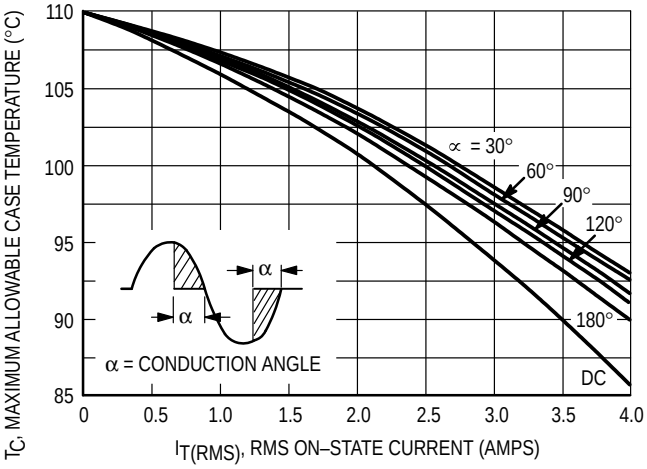


Figure 1. RMS Current Derating

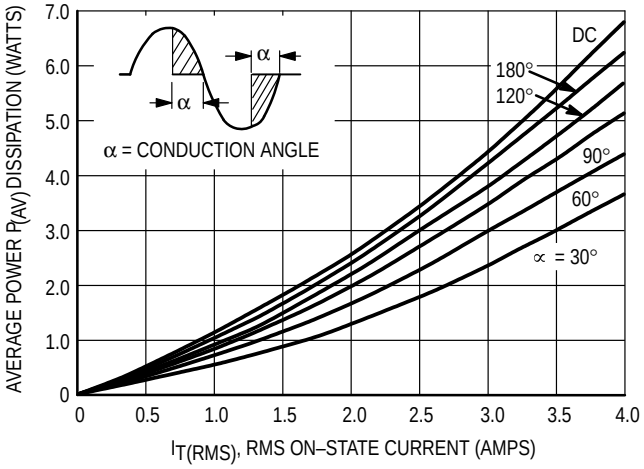


Figure 2. Maximum On–State Power Dissipation

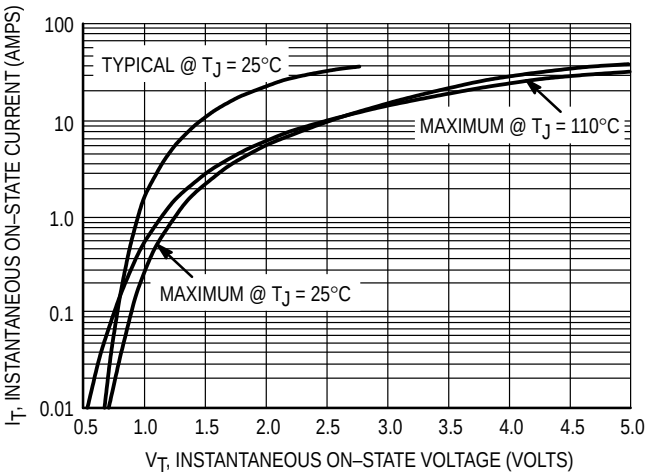


Figure 3. On–State Characteristics

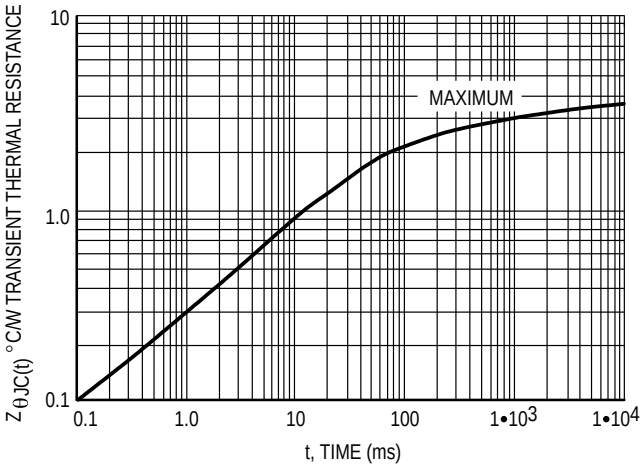


Figure 4. Transient Thermal Response

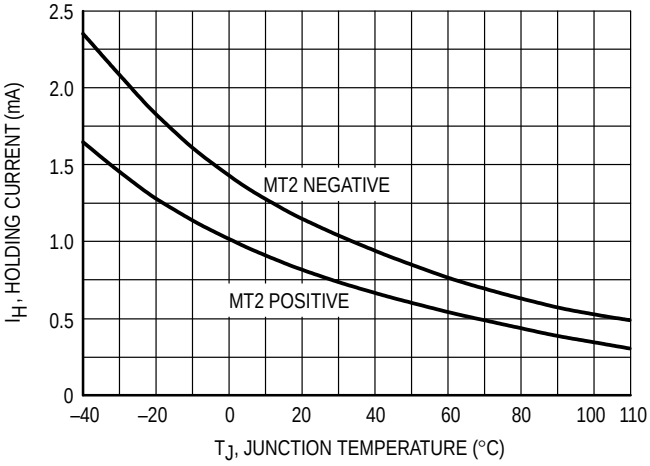


Figure 5. Typical Holding Current versus Junction Temperature

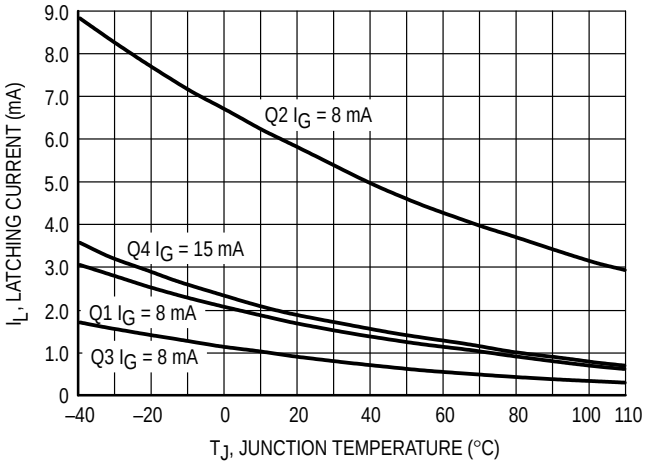


Figure 6. Typical Latching Current versus Junction Temperature (MAC6075B)

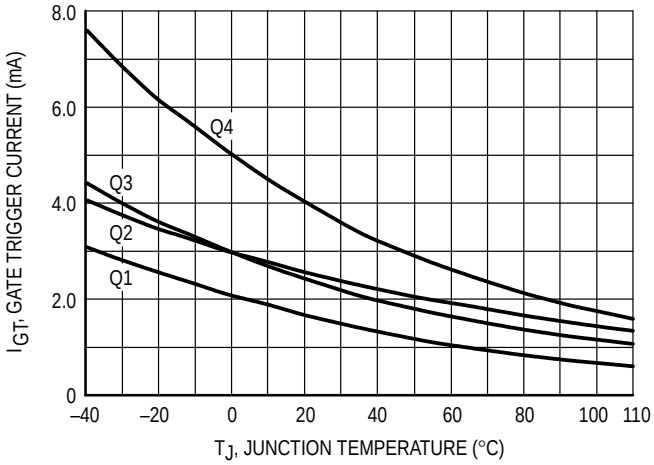


Figure 7. Typical Gate Trigger Current versus Junction Temperature

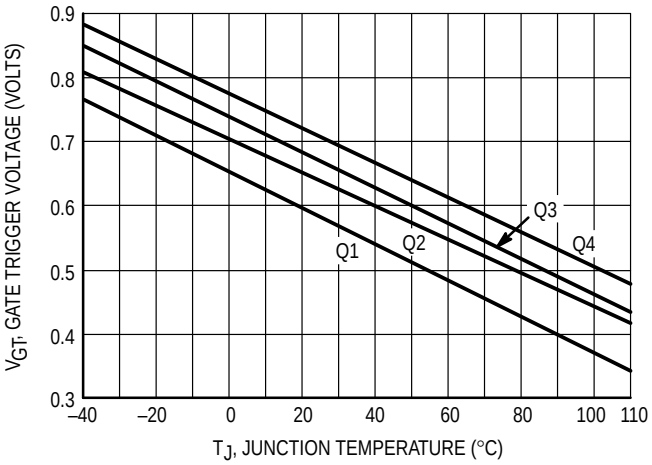


Figure 8. Typical Gate Trigger Voltage versus Junction Temperature

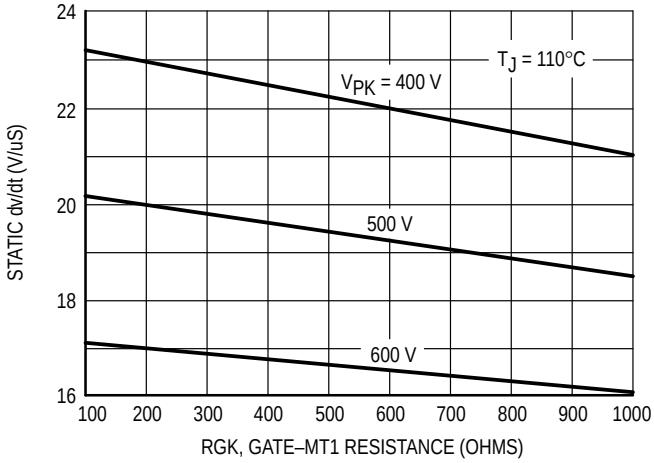


Figure 9. Typical Exponential Static dv/dt versus Gate–MT1 Resistance, MT2(+)

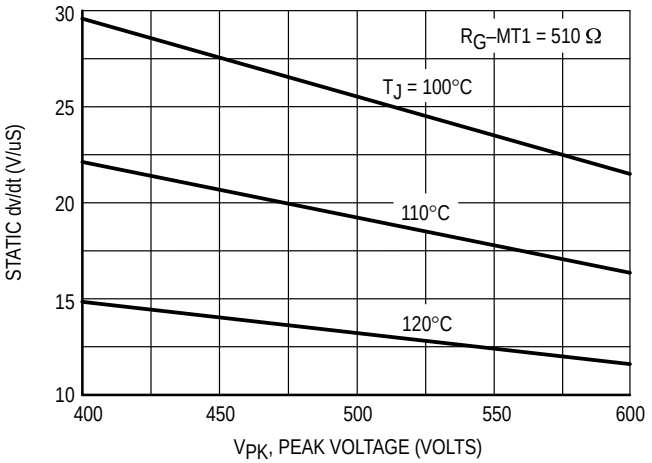


Figure 10. Typical Exponential Static dv/dt versus Peak Voltage, MT2(+)

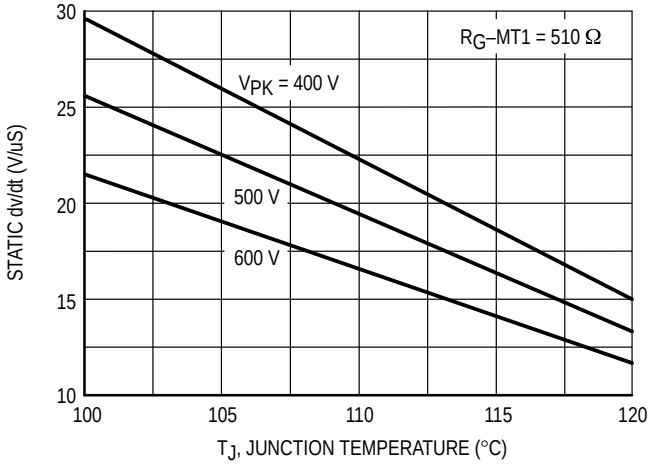


Figure 11. Typical Exponential Static dv/dt versus Junction Temperature, MT2(+)

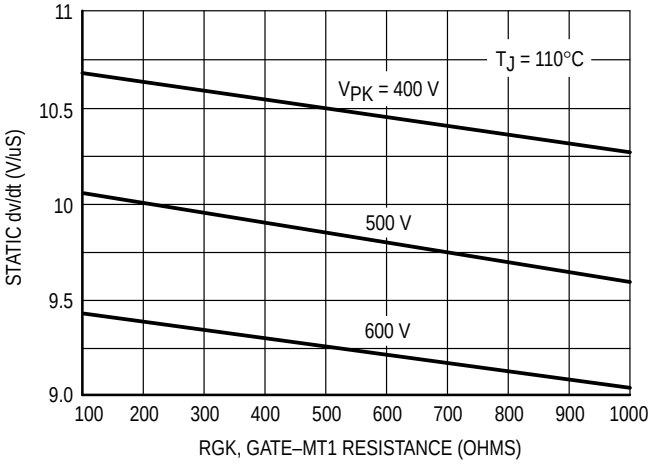


Figure 12. Typical Exponential Static dv/dt versus Gate–MT1 Resistance, MT2(–)

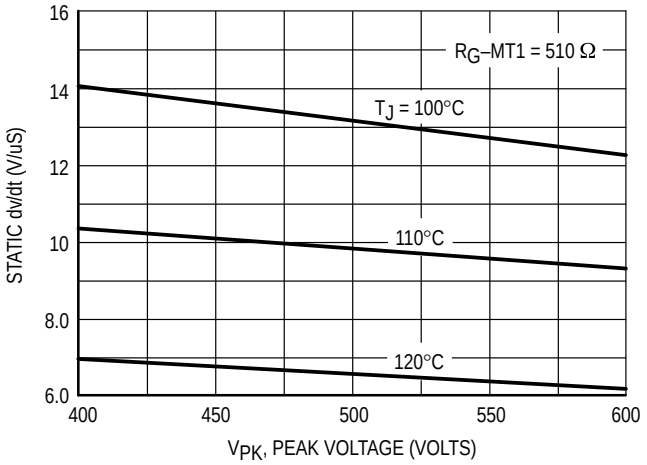


Figure 13. Typical Exponential Static dv/dt versus Peak Voltage, MT2(–)

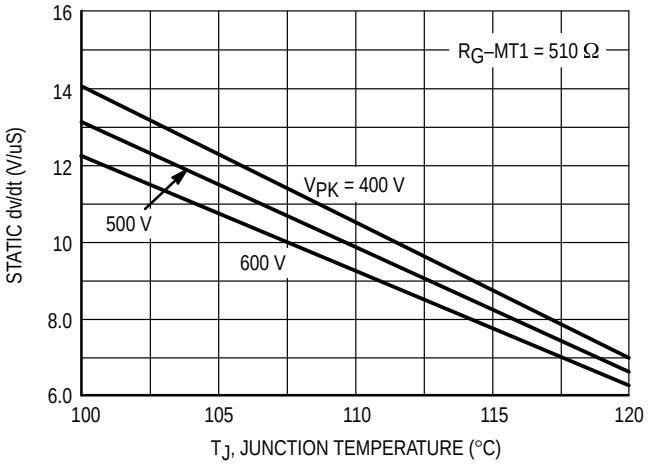


Figure 14. Typical Exponential Static dv/dt versus Junction Temperature, MT2(–)

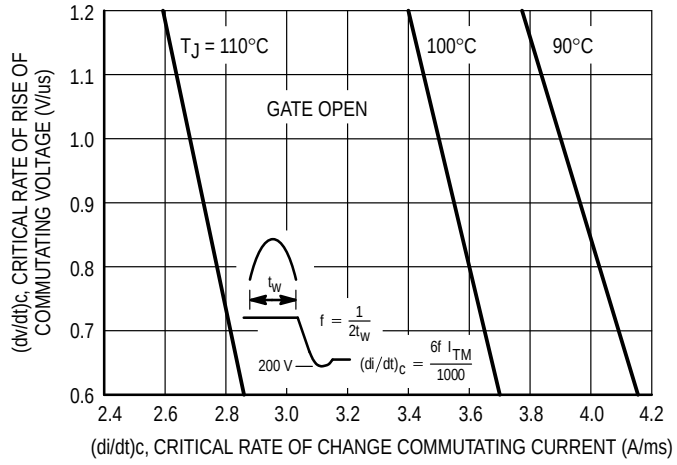
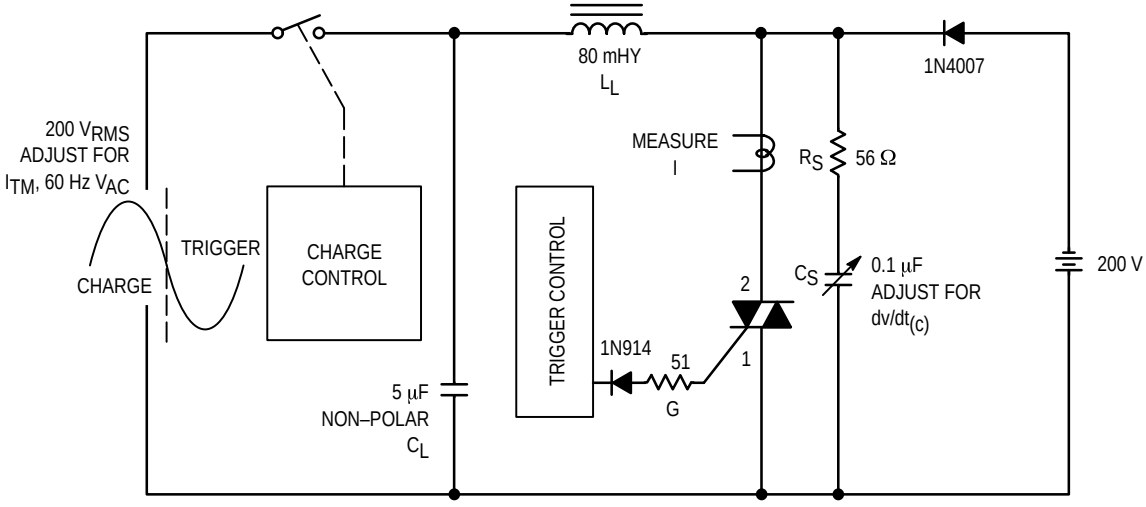


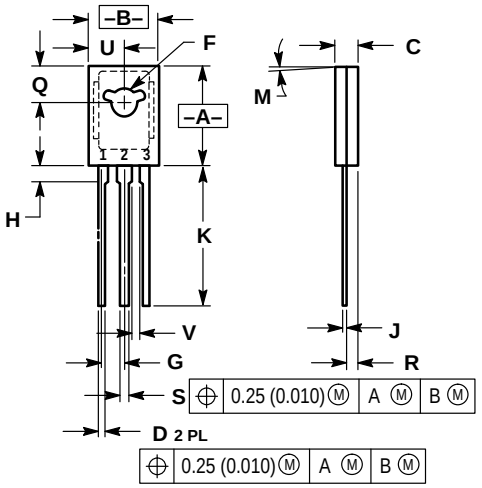
Figure 15. Critical Rate of Rise of Commutating Voltage



NOTE: Component values are for verification of rated $(dv/dt)_c$. See AN1048 for additional information.

Figure 16. Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Voltage

PACKAGE DIMENSIONS



STYLE 5:
PIN 1. MT 1
2. MT 2
3. GATE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.425	0.435	10.80	11.04
B	0.295	0.305	7.50	7.74
C	0.095	0.105	2.42	2.66
D	0.020	0.026	0.51	0.66
F	0.115	0.130	2.93	3.30
G	0.094 BSC		2.39 BSC	
H	0.050	0.095	1.27	2.41
J	0.015	0.025	0.39	0.63
K	0.575	0.655	14.61	16.63
M	5° TYP		5° TYP	
Q	0.148	0.158	3.76	4.01
R	0.045	0.055	1.15	1.39
S	0.025	0.035	0.64	0.88
U	0.145	0.155	3.69	3.93
V	0.040	—	1.02	—

CASE 77–08
(TO–225AA)

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