

SOT-223 Triac Silicon Bidirectional Thyristors

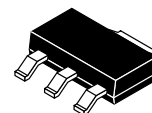
Designed for use in solid state relays, MPU interface, TTL logic and other light industrial or consumer applications. Supplied in surface mount package for use in automated manufacturing.

- Sensitive Gate Trigger Current in Four Trigger Modes
- Blocking Voltage to 600 Volts
- Glass Passivated Surface for Reliability and Uniformity
- Surface Mount Package
- Devices Supplied on 1 K Reel

MAC08BT1 Series *

*Motorola preferred devices

TRIAC
0.8 AMPERE RMS
200 thru 600 Volts



CASE 318E-04
(SOT-223)
STYLE 11

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Blocking Voltage ⁽¹⁾ (1/2 Sine Wave, Gate Open, T _J = 25 to 110°C)	V _{DRM}	200 400 600	Volts
On-State Current RMS (T _C = 80°C)	I _{T(RMS)}	0.8	Amps
Peak Non-repetitive Surge Current (One Full Cycle, 60 Hz, T _C = 25°C)	I _{TSM}	10	Amps
Circuit Fusing Considerations (t = 8.3 ms)	I ² t	0.4	A ² s
Peak Gate Power (t < 2.0 μs)	P _{GM}	5.0	Watts
Average Gate Power (T _C = 80°C, t = 8.3 ms)	P _{G(AV)}	0.1	Watts
Operating Junction Temperature Range	T _J	-40 to +110	°C
Storage Temperature Range	T _{stg}	-40 to +150	°C
Maximum Device Temperature for Soldering Purposes (for 5 Seconds Maximum)	T _L	260	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient PCB Mounted per Figure 1	R _{θJA}	156	°C/W
Thermal Resistance, Junction to Tab Measured on Anode Tab Adjacent to Epoxy	R _{θJT}	25	°C/W

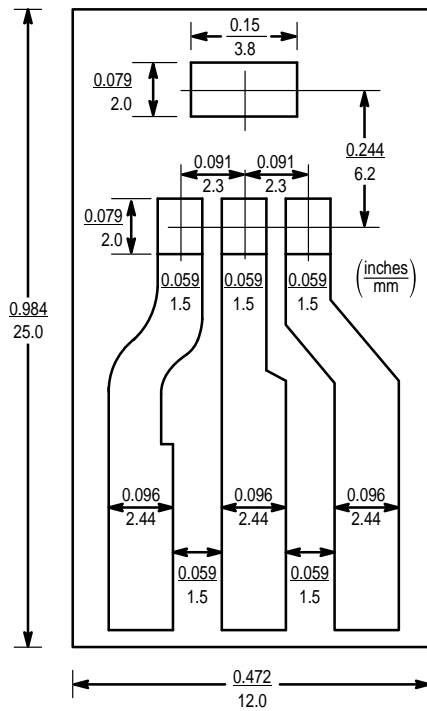
1. V_{DRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Repetitive Blocking Current ($V_D = \text{Rated } V_{DRM}$ Gate Open) $T_J = 25^\circ\text{C}$ $T_J = 110^\circ\text{C}$	I_{DRM}	— —	— —	10 200	μA μA
Maximum On-State Voltage (Either Direction) ($I_T = 1.1 \text{ A Peak}$, $T_A = 25^\circ\text{C}$)	V_{TM}	—	—	1.9	Volts
Gate Trigger Current (Continuous dc) All Quadrants ($V_D = 7.0 \text{ Vdc}$, $R_L = 100 \Omega$)	I_{GT}	—	—	10	mA
Holding Current (Either Direction) ($V_D = 7.0 \text{ Vdc}$, Gate Open, Initiating Current = 20 mA, Gate Open)	I_H	—	—	5.0	mA
Gate Trigger Voltage (Continuous dc) All Quadrants ($V_D = 7.0 \text{ Vdc}$, $R_L = 100 \Omega$)	V_{GT}	—	—	2.0	Volts
Critical Rate of Rise of Commutation Voltage ($f = 250 \text{ Hz}$, $I_{TM} = 1.0 \text{ A}$, Commutating $di/dt = 1.5 \text{ A/ms}$ On-State Current Duration = 2.0 ms, $V_{DRM} = 200 \text{ V}$, Gate Unenergized, $T_C = 110^\circ\text{C}$, Gate Source Resistance = 150Ω , See Figure 10)	dv/dt_C	1.5	—	—	$\text{V}/\mu\text{s}$
Critical Rate-of-Rise of Off State Voltage ($V_{pk} = \text{Rated } V_{DRM}$, $T_C = 110^\circ\text{C}$, Gate Open, Exponential Method)	dv/dt	10	—	—	$\text{V}/\mu\text{s}$



BOARD MOUNTED VERTICALLY IN CINCH 8840 EDGE CONNECTOR.
BOARD THICKNESS = 65 MIL., FOIL THICKNESS = 2.5 MIL.
MATERIAL: G10 FIBERGLASS BASE EPOXY

Figure 1. PCB for Thermal Impedance and Power Testing of SOT-223

MAC08BT1 Series

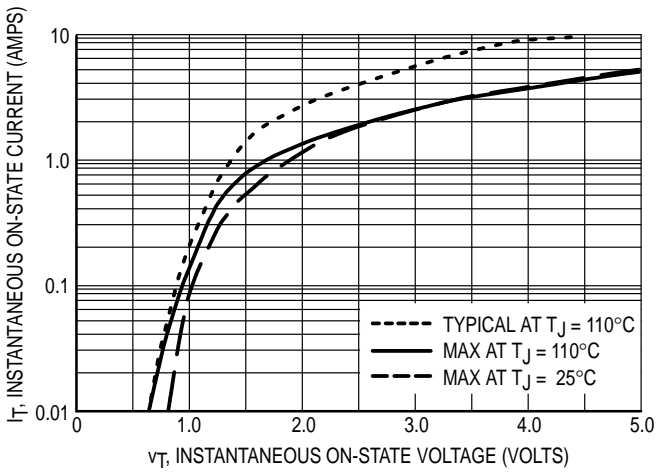


Figure 2. On-State Characteristics

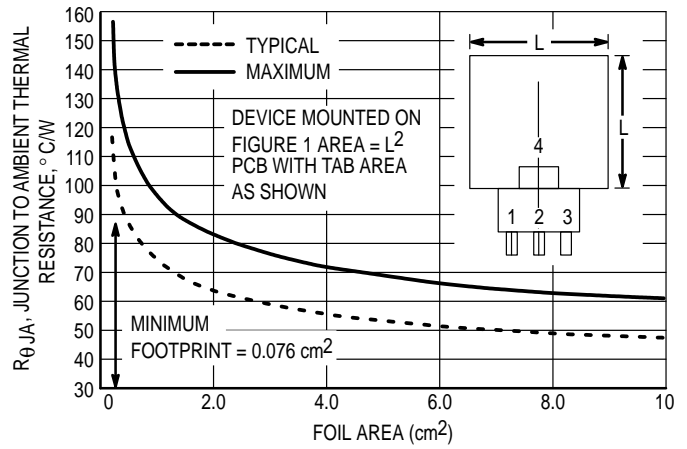


Figure 3. Junction to Ambient Thermal Resistance versus Copper Tab Area

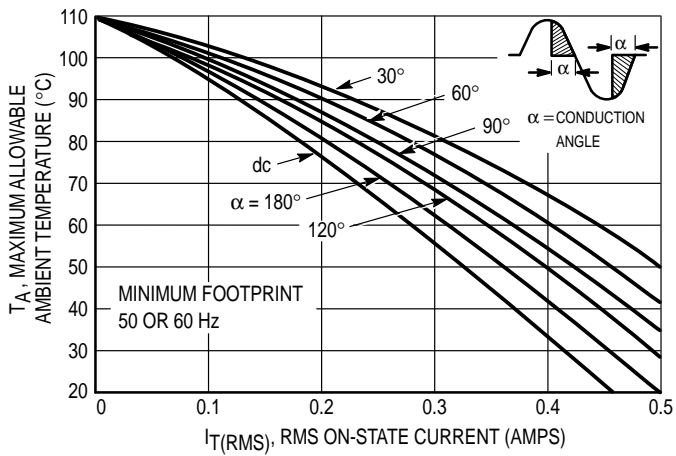


Figure 4. Current Derating, Minimum Pad Size Reference: Ambient Temperature

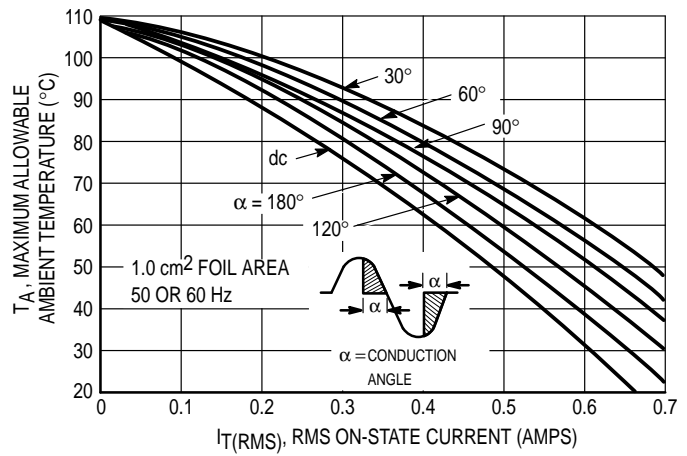


Figure 5. Current Derating, 1.0 cm Square Pad Reference: Ambient Temperature

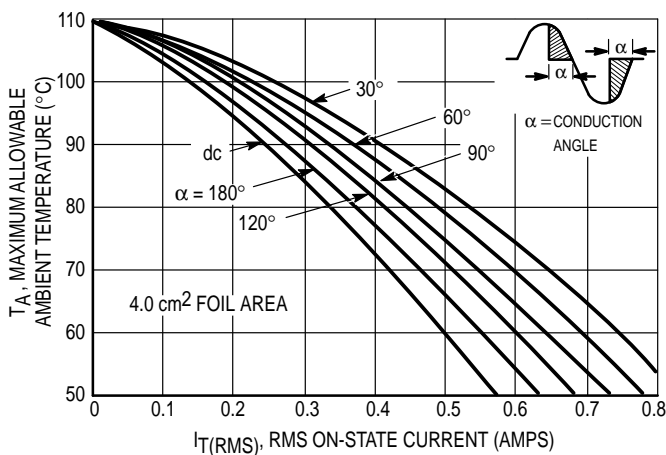


Figure 6. Current Derating, 2.0 cm Square Pad Reference: Ambient Temperature

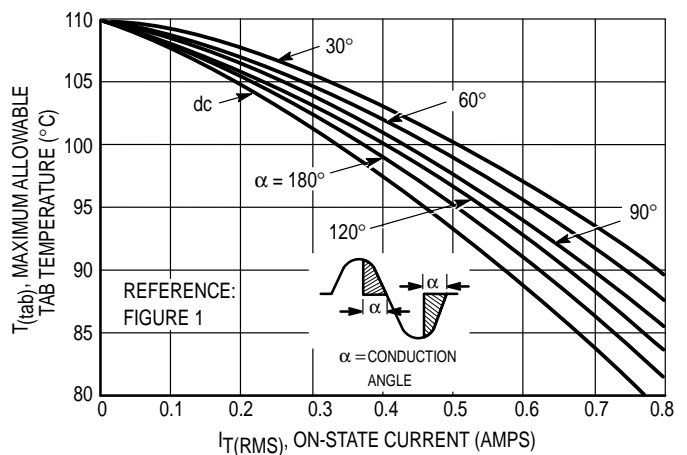


Figure 7. Current Derating Reference: MT2 Tab

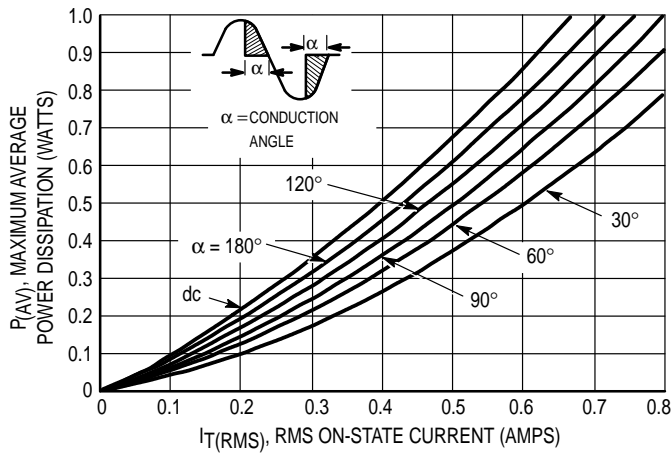


Figure 8. Power Dissipation

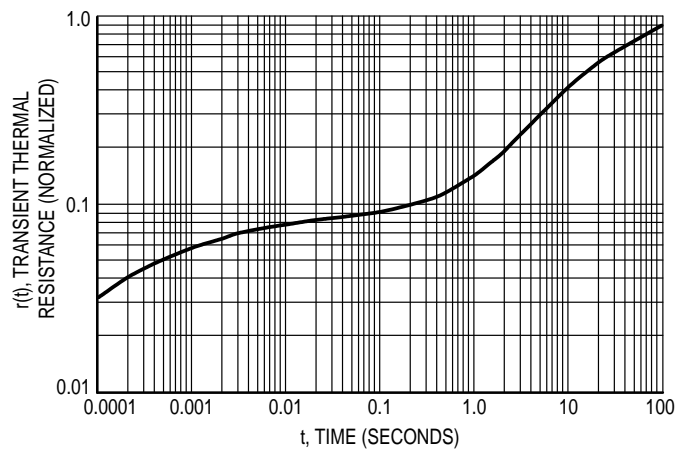
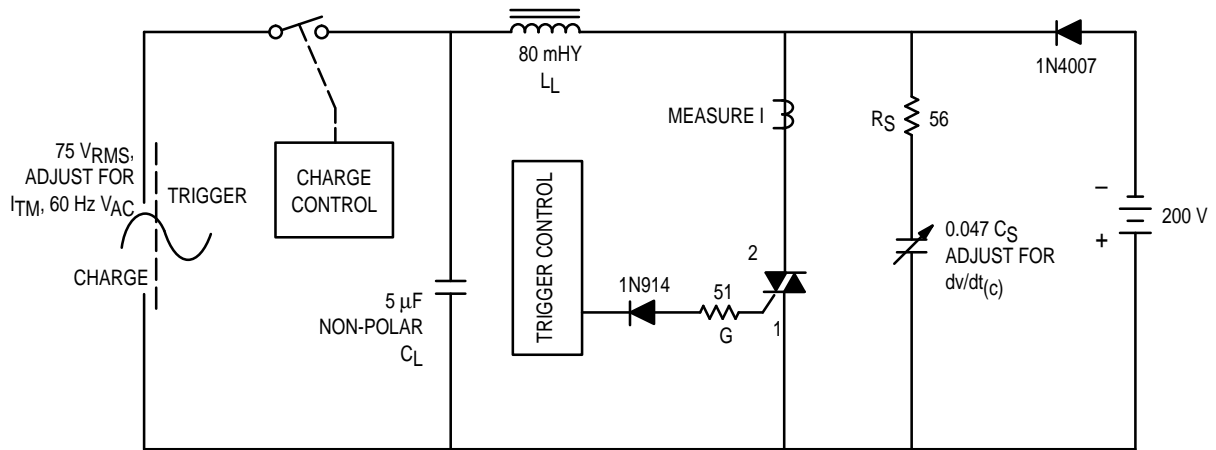


Figure 9. Thermal Response, Device Mounted on Figure 1 Printed Circuit Board



Component values are for verification of rated $(dv/dt)_c$. See AN1048 for additional information.

Figure 10. Simplified Q_1 $(dv/dt)_c$ Test Circuit

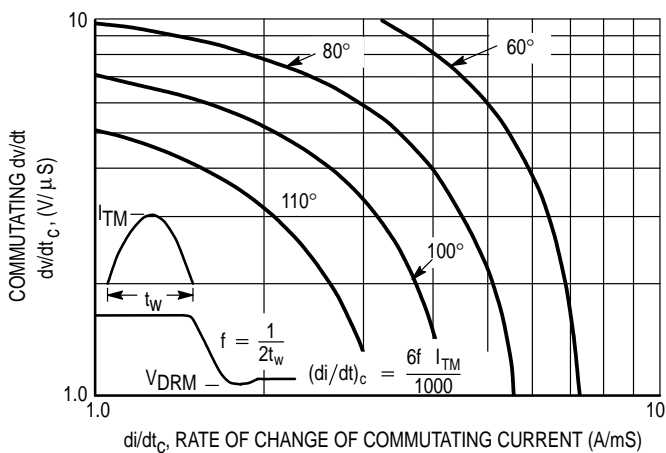


Figure 11. Typical Commutating dv/dt versus Current Crossing Rate and Junction Temperature

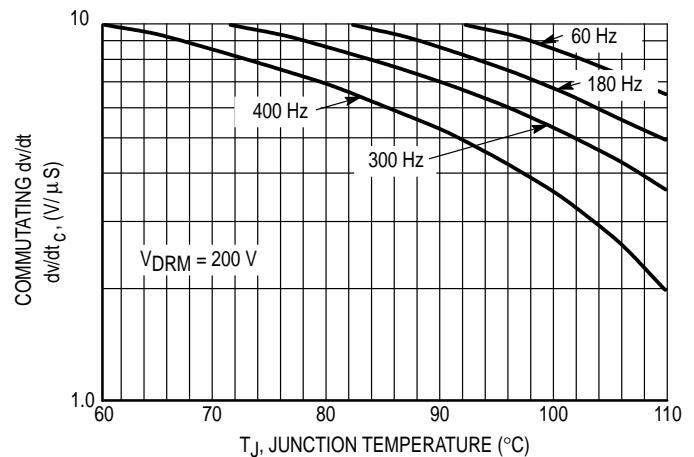


Figure 12. Typical Commutating dv/dt versus Junction Temperature at 0.8 Amps RMS

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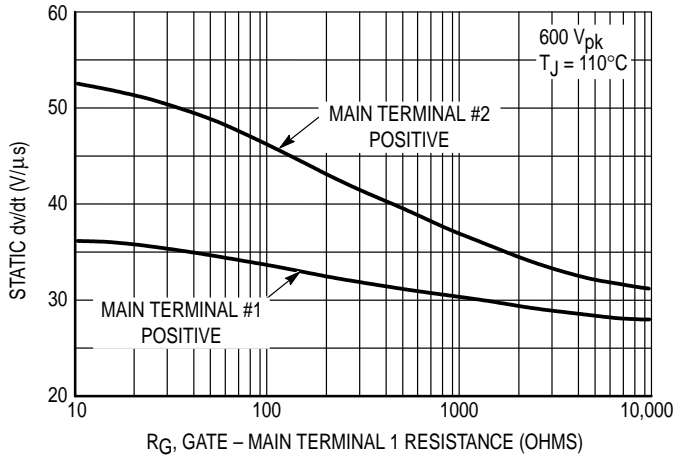


Figure 13. Exponential Static dv/dt versus Gate - Main Terminal 1 Resistance

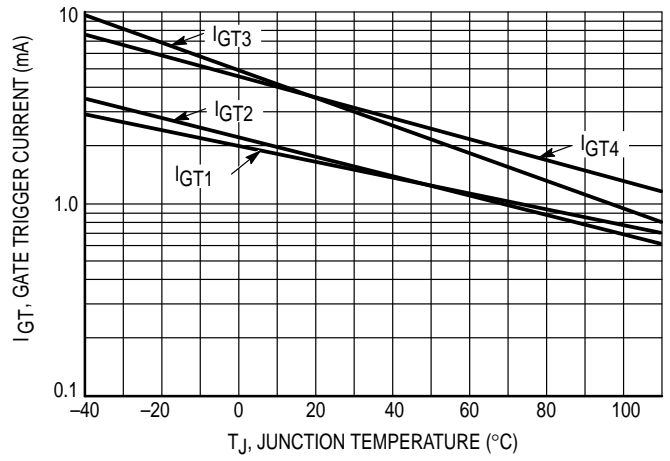


Figure 14. Typical Gate Trigger Current Variation

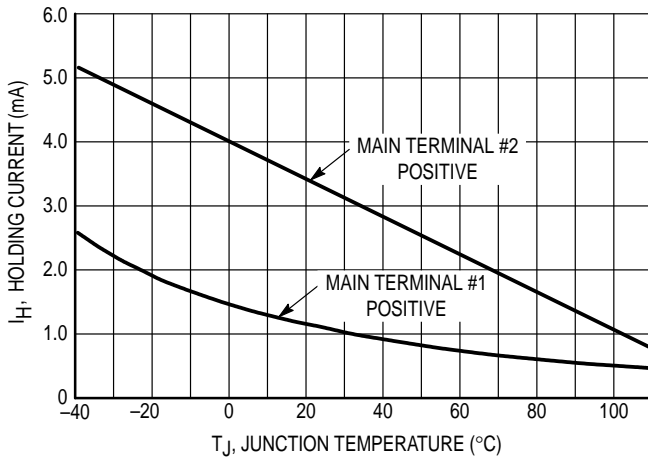


Figure 15. Typical Holding Current Variation

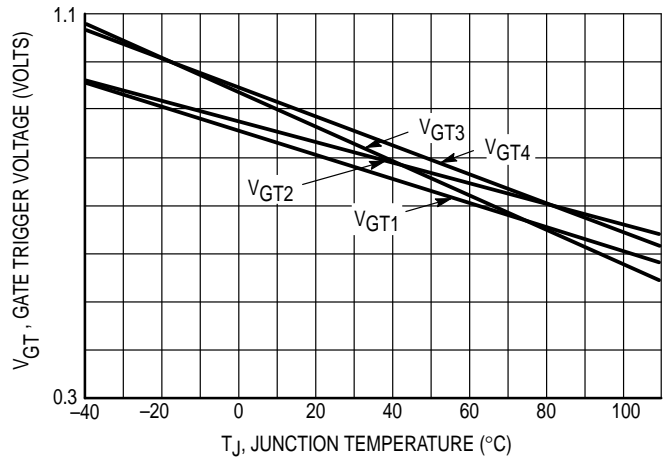


Figure 16. Gate Trigger Voltage Variation