

## High-Speed, Low $r_{ON}$ , SPST Analog Switch (1-Bit Bus Switch)

### FEATURES

- SC-70 5-Lead Package
- 5- $\Omega$  Switch Connection Between Two Ports
- Minimal Propagation Delay Through The Switch
- Low  $I_{CC}$
- Zero Bounce In Flow-Through Mode
- Control Inputs Compatible with TTL Level

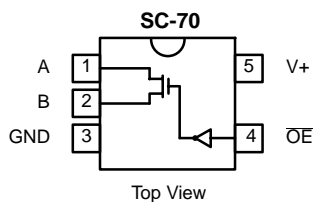
### DESCRIPTION

The DG2301 is a high-speed, 1-bit, low power, TTL-compatible bus switch. Using sub-micron CMOS technology, DG2301 achieves low on-resistance and negligible propagation delay.

The DG2301 consist of a bi-directional input/output pins A and

B. When the output enable ( $\overline{OE}$ ) is low, the input/output pins are connected. When the  $\overline{OE}$  is high, the switch is open and a high-impedance state exists between input/output pins A and B.

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Device Marking: E4

**TRUTH TABLE**

$\overline{OE}$	B	Function
L	A	Connect
H	HiZ State	Disconnect

**ORDERING INFORMATION**

Temp Range	Package	Part Number
-40 to 85°C	SC70-5	DG2301DL



**ABSOLUTE MAXIMUM RATINGS**

Reference to GND

V+	.....	-0.3 to +6 V
OE, A, B <sup>a</sup>	.....	-0.3 to (V+ + 0.3 V)
Continuous Current (Any terminal)	.....	± 50 mA
Peak Current (Pulsed at 1 ms, 10% duty cycle)	.....	± 200 mA
Storage Temperature (D Suffix)	.....	-65 to 150°C

Power Dissipation (Packages)<sup>b</sup>

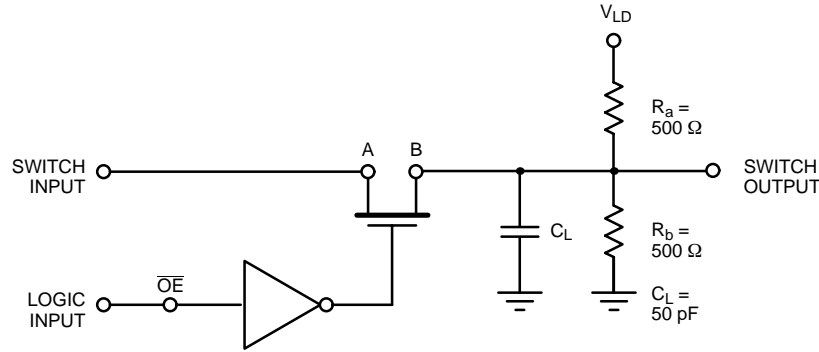
6-Pin SC70 <sup>c</sup>	.....	250 mW
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- Notes:
- Signals on A, or B or OE exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
  - All leads welded or soldered to PC Board.
  - Derate 3.1 mW/°C above 70°C

SPECIFICATIONS (V+ = 5.0 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 4.0 V to 5.5 V, V <sub>OE</sub> = 0.8 or 2.0 V <sup>e</sup>	Temp <sup>a</sup>	Limits -40 to 85°C			Unit
				Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
<b>DC Characteristics</b>							
On-Resistance	r <sub>ON</sub>	V+ = 4.5 V, V <sub>A</sub> = 0 V, I <sub>B</sub> = 64 mA	Full			7	Ω
		V+ = 4.5 V, V <sub>A</sub> = 0 V, I <sub>B</sub> = 30 mA	Full			7	
		V+ = 4.5 V, V <sub>A</sub> = 2.4 V, I <sub>B</sub> = 15 mA	Full			15	
		V+ = 4.0 V, V <sub>A</sub> = 2.4 V, I <sub>B</sub> = 15 mA	Full			20	
Switch Off Leakage Current	I <sub>(off)</sub>	V+ = 5.5 V, V <sub>A</sub> = 1 V/4.5 V, V <sub>B</sub> = 4.5 V/1 V	Full	-10		10	μA
Switch-On Leakage Current	I <sub>(on)</sub>	V+ = 5.5 V, V <sub>A</sub> = V <sub>B</sub> = 1 V/4.5 V	Full	-10		10	
Input High Voltage	V <sub>IH</sub>		Full	2.0			V
Input Low Voltage	V <sub>IL</sub>		Full			0.8	
Input Current	I <sub>IL</sub> or I <sub>IH</sub>	V <sub>OE</sub> = 0 or V+	Full	-1		1	μA
<b>Dynamic Characteristics</b>							
Prop Delay Bus-to-Bus <sup>f</sup>	t <sub>PHL</sub>	V <sub>LD</sub> = Open (Figure 1 and 2)	Full			1	ns
	t <sub>PLH</sub>		Full			1	
Output Enable Time <sup>d</sup>	t <sub>PZL</sub>	V <sub>LD</sub> = 7 V, V+ = 4.5 V to 5.5 V (Figure 1 and 2)	Full			3.9	
		V <sub>LD</sub> = 7 V, V+ = 4.0 V (Figure 1 and 2)	Full			4.5	
	t <sub>PZH</sub>	V <sub>LD</sub> = Open, V+ = 4.5 V to 5.5 V (Figure 1 and 2)	Full			3.7	
		V <sub>LD</sub> = Open, V+ = 4.0 V (Figure 1 and 2)	Full			4.5	
Output Disable Time <sup>d</sup>	t <sub>PLZ</sub>	V <sub>LD</sub> = 7 V, V+ = 4.5 V to 5.5 V (Figure 1 and 2)	Full			4.0	
		V <sub>LD</sub> = 7 V, V+ = 4.0 V (Figure 1 and 2)	Full			4.2	
	t <sub>PHZ</sub>	V <sub>LD</sub> = Open, V+ = 4.5 V to 5.5 V (Figure 1 and 2)	Full			1.0	
		V <sub>LD</sub> = Open, V+ = 4.0 V (Figure 1 and 2)	Full			1.0	
Input Capacitance	C <sub>in</sub>		Room			3.5	pF
Channel-Off Capacitance <sup>d</sup>	C <sub>(off)</sub>	V <sub>OE</sub> = 0 or V+, f = 1 MHz	Room			5	
Channel-On Capacitance <sup>d</sup>	C <sub>ON</sub>		Room			11	
<b>Power Supply</b>							
Power Supply Range	V+			4.0		5.5	V
Power Supply Current	I+	V <sub>OE</sub> = 0 or V+			0.01	1.0	μA

- Notes:
- Room = 25°C, Full = as determined by the operating suffix.
  - The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
  - Typical values are for design aid only, not guaranteed nor subject to production testing.
  - Guarantee by design, nor subjected to production test.
  - V<sub>IN</sub> = input voltage to perform proper function.
  - Guaranteed by design and not production tested. The bus switch propagation delay is a function of the RC time constant contributed by the on-resistance and the specified load capacitance with an ideal voltage source (zero output impedance) driving the switch.

**AC LOADING AND WAVEFORMS**



Input driven by 50- $\Omega$  source terminated in 50  $\Omega$   
 $C_L$  includes load and stray capacitance  
 Input PRR = 1.0 MHz,  $t_W = 50 \text{ ns}$

Figure 1. AC Test Circuit

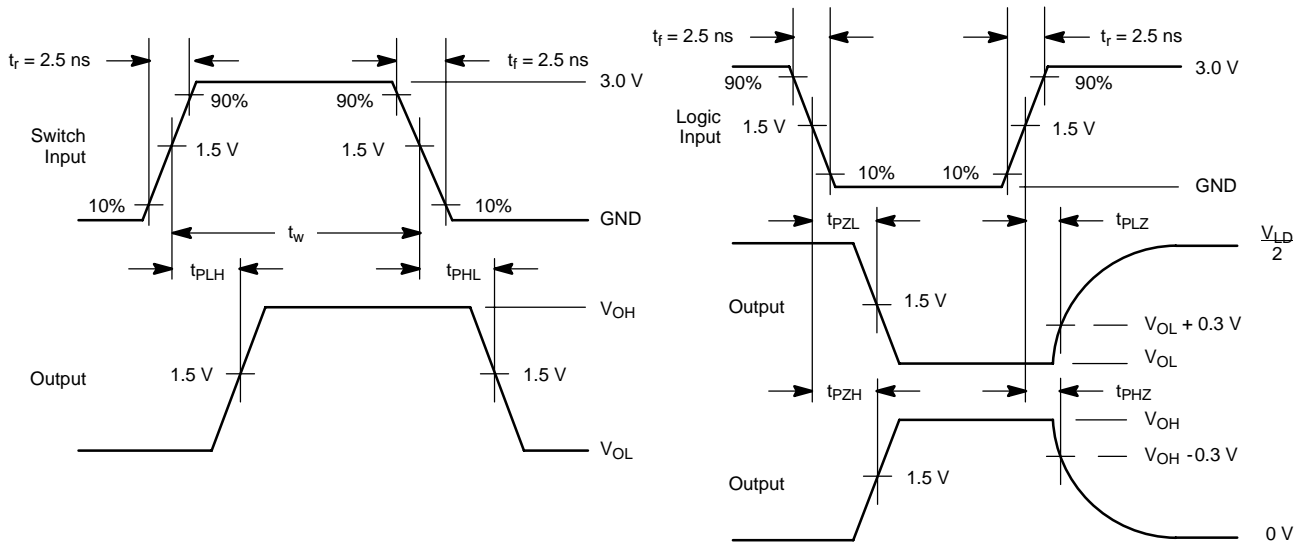
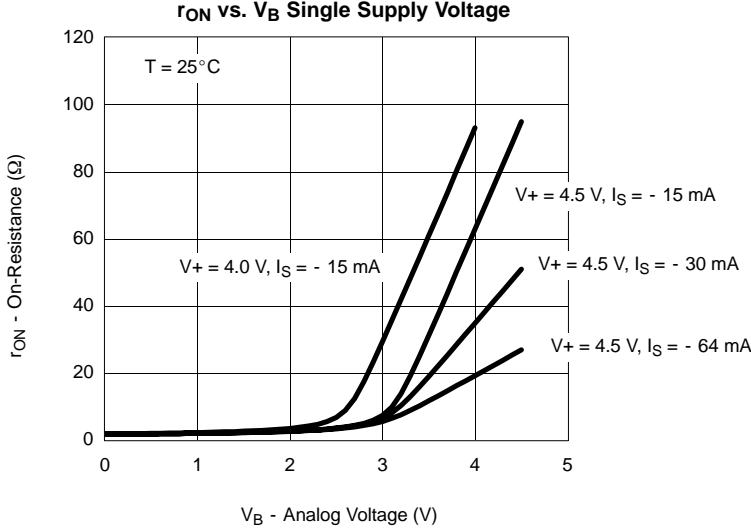


Figure 2. AC Waveforms



**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**



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