



# Quad SPST CMOS Analog Switch with Latches

## FEATURES

- Accepts 150-ns Write Pulse Width
- 5-V On-Chip Regulator
- Latches Are Transparent with  $\overline{WR}$  Low
- Low On-Resistance: 60  $\Omega$

## BENEFITS

- Compatible with Most  $\mu$ P Buses
- Allows Wide Power Supply Tolerance Without Affecting TTL Compatibility
- Reduced Power Consumption
- Allows Flexibility of Design

## APPLICATIONS

- $\mu$ P Based Systems
- Automatic Test Equipment
- Communication Systems
- Data Acquisition Systems
- Medical Instrumentation
- Factory Automation

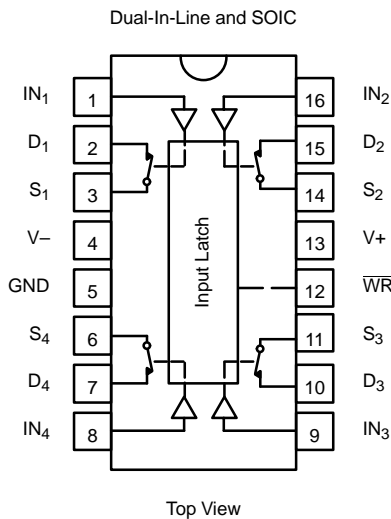
## DESCRIPTION

The DG221B is a monolithic quad single-pole, single-throw analog switch designed for precision switching applications in communication, instrumentation and process control systems. Featuring independent onboard latches and a common  $\overline{WR}$  pin, each DG221B can be memory mapped, and addressed as a single data byte for simultaneous switching.

The DG221B combines low power and low on-resistance (60  $\Omega$  typical) while handling continuous currents up to 20 mA. An epitaxial layer prevents latchup.

The device features true bidirectional performance in the on condition.

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Four Latchable SPST Switches per Package

TRUTH TABLE		
$IN_x$	$\overline{WR}$	Switch
0	0	ON
1	0	OFF
X		Control data latched-in, switches on or off as selected by last $IN_x$
X	1	Maintains previous state

Logic "0"  $\leq$  0.8 V  
Logic "1"  $\geq$  2.4 V

ORDERING INFORMATION		
Temp Range	Package	Part Number
-40°C to 85°C	16-Pin Plastic DIP	DG221BDJ
	16-Pin Narrow SOIC	DG221BDY

**ABSOLUTE MAXIMUM RATINGS**

Voltages Referenced to V-	
V+ .....	34 V
GND .....	25 V
Digital Inputs <sup>a</sup> , V <sub>S</sub> , V <sub>D</sub> .....	(V-) -2 V to (V+) +2 V or 20 mA, whichever occurs first
Continuous Current (Any Terminal) .....	30 mA
Continuous Current, S or D .....	20 mA
Peak Current, S or D (Pulsed 1 ms, 10% duty cycle) .....	70 mA

Storage Temperature: (DJ and DY Suffix) .....	-65 to 125°C
Power Dissipation (Package) <sup>b</sup>	
16-Pin Plastic DIP <sup>c</sup> .....	470 mW
16-Pin SOIC <sup>d</sup> .....	600 mW

- Notes:
- a. Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
  - b. All leads welded or soldered to PC Board.
  - c. Derate 6.5 mW/°C above 25°C
  - d. Derate 7.7 mW/°C above 75°C

**SCHEMATIC DIAGRAM (TYPICAL CHANNEL)**

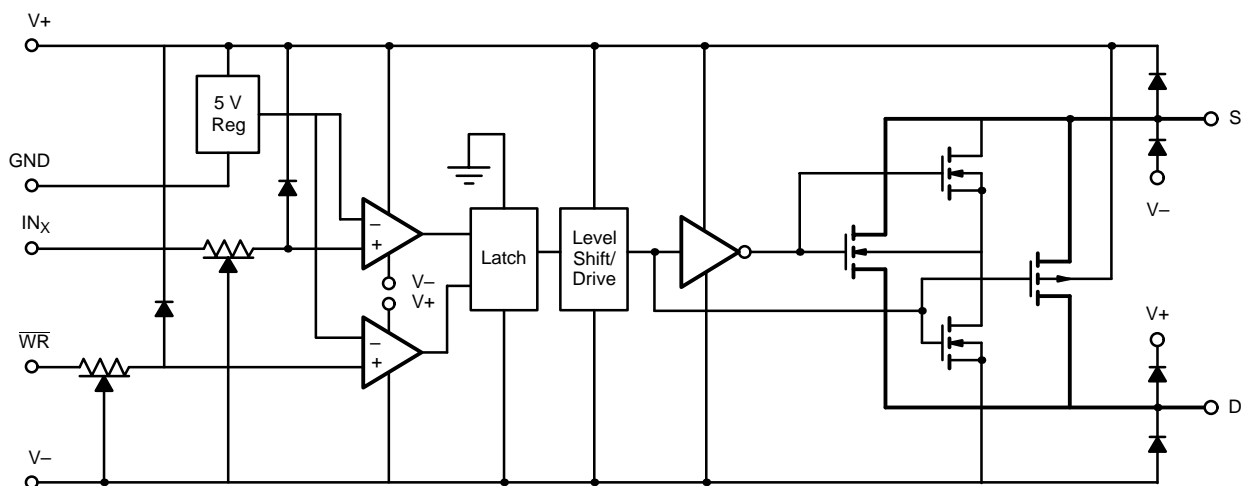


FIGURE 1.

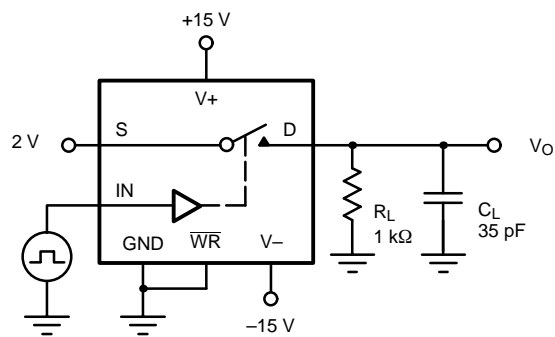


SPECIFICATIONS <sup>a</sup>							
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $V_{IN} = 2.4\text{ V}, 0.8^f\text{ V}, \overline{WR} = 0$	Temp <sup>b</sup>	Limits -40 to 85°C			Unit
				Min <sup>d</sup>	Typ <sup>c</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full	-15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	$I_S = -10\text{ mA}, V_D = \pm 10\text{ V}$	Room Full		60	90 135	$\Omega$
Source Off Leakage Current	$I_{S(off)}$	$V_S = \pm 14\text{ V}, V_D = \mp 14\text{ V}$	Room Full	-5 -100	$\pm 0.01$	5 100	nA
Drain Off Leakage Current	$I_{D(off)}$		Room Full	-5 -100	$\pm 0.02$	5 100	
Drain On Leakage Current	$I_{D(on)}$	$V_S = V_D = \pm 14\text{ V}$	Room Full	-5 -200	$\pm 0.01$	5 200	
<b>Digital Control</b>							
Input Current	$I_{INL}, I_{INH}$	$V_{IN} = 0\text{ V or } 2.4\text{ V}$	Room Full	-1 -10	-0.0004	1 10	$\mu\text{A}$
<b>Dynamic Characteristics</b>							
Turn-On Time	$t_{ON}$	See Figure 2	Room			550	ns
Turn-Off Time	$t_{OFF}$		Room			340	
Turn-On Time Write	$t_{ON}, \overline{WR}$	See Figure 3	Room			550	
Turn-Off Time Write	$t_{OFF}, \overline{WR}$		Room			340	
Write Pulse Width	$t_W$	See Figure 4	Room	150	120		
Input Setup Time	$t_S$		Room	180	130		
Input Hold Time	$t_H$		Room	20	18		
Charge Injection	Q	$C_L = 1000\text{ pF}$ $V_{GEN} = 0\text{ V}, R_{GEN} = 0\ \Omega$	Room		20		pC
Source-Off Capacitance	$C_{S(off)}$	$f = 1\text{ MHz}, V_S, V_D = 0\text{ V}$	Room		8		pF
Drain-Off Capacitance	$C_{D(off)}$		Room		9		
Channel-On Capacitance	$C_{D(on)}$		Room		29		
Off Isolation	OIRR	$V_S = 1\text{ V}_{p-p}, f = 100\text{ kHz}$ $C_L = 15\text{ pF}, R_L = 1\text{ k}\Omega$	Room		70		dB
Interchannel Crosstalk	$X_{TALK}$		Room		90		
<b>Power Supplies</b>							
Positive Supply Current	I+	All Channels On or Off $V_{IN} = 0\text{ V or } 2.4\text{ V}$	Full		0.8	1.5	mA
Negative Supply Current	I-		Room	-1	-0.4		

Notes:

- Refer to PROCESS OPTION FLOWCHART.
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.

TEST CIRCUITS



$C_L$  (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

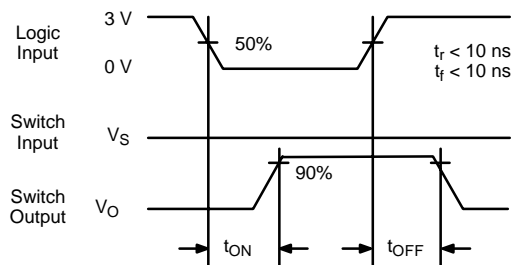
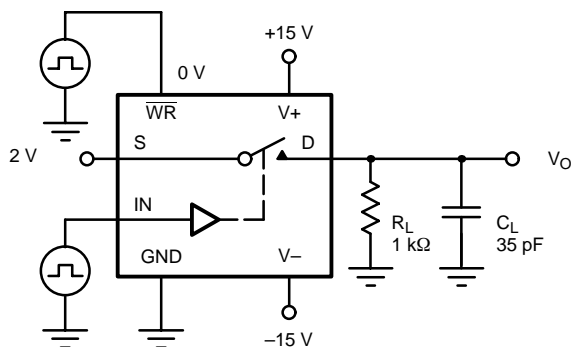


FIGURE 2. Switching Time



$C_L$  (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

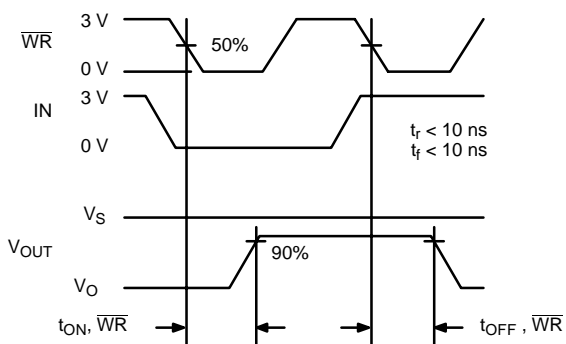
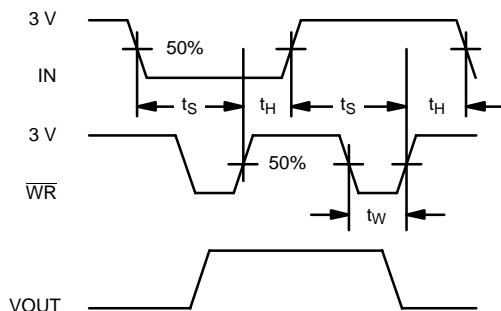


FIGURE 3.  $\overline{WR}$  Switching Time

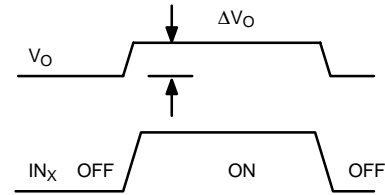
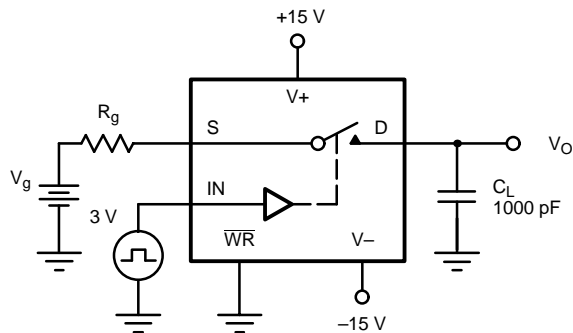


$t_H$  = Hold Time  
 $t_S$  = Setup Time  
 $t_W$  =  $\overline{WR}$  Pulse Width

The latches are level sensitive. When  $\overline{WR}$  is held low the latches are transparent and the switches respond to the digital inputs. The digital inputs are latched on the rising edge of  $\overline{WR}$ .

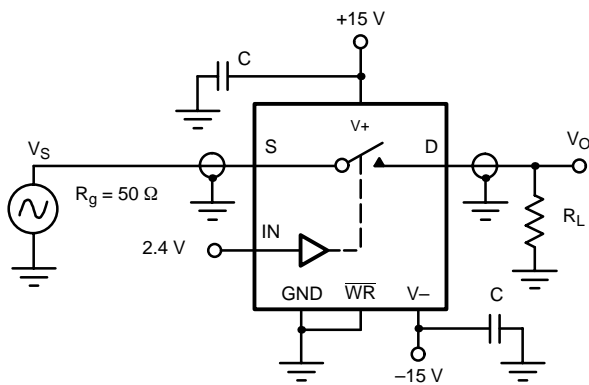
FIGURE 4.  $\overline{WR}$  Setup Conditions

TEST CIRCUITS



$\Delta V_O$  = measured voltage error due to charge injection  
The charge injection in coulombs is  $Q = C_L \times \Delta V_O$

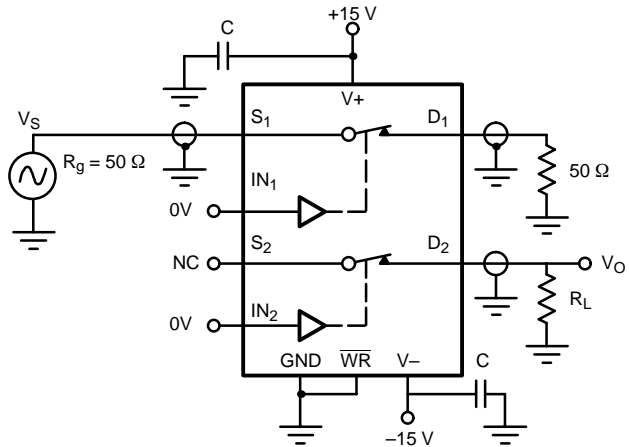
FIGURE 5. Charge Injection



$$\text{Off Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

C = RF bypass

FIGURE 6. Off Isolation



$$X_{\text{TALK}} \text{ Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

C = RF bypass

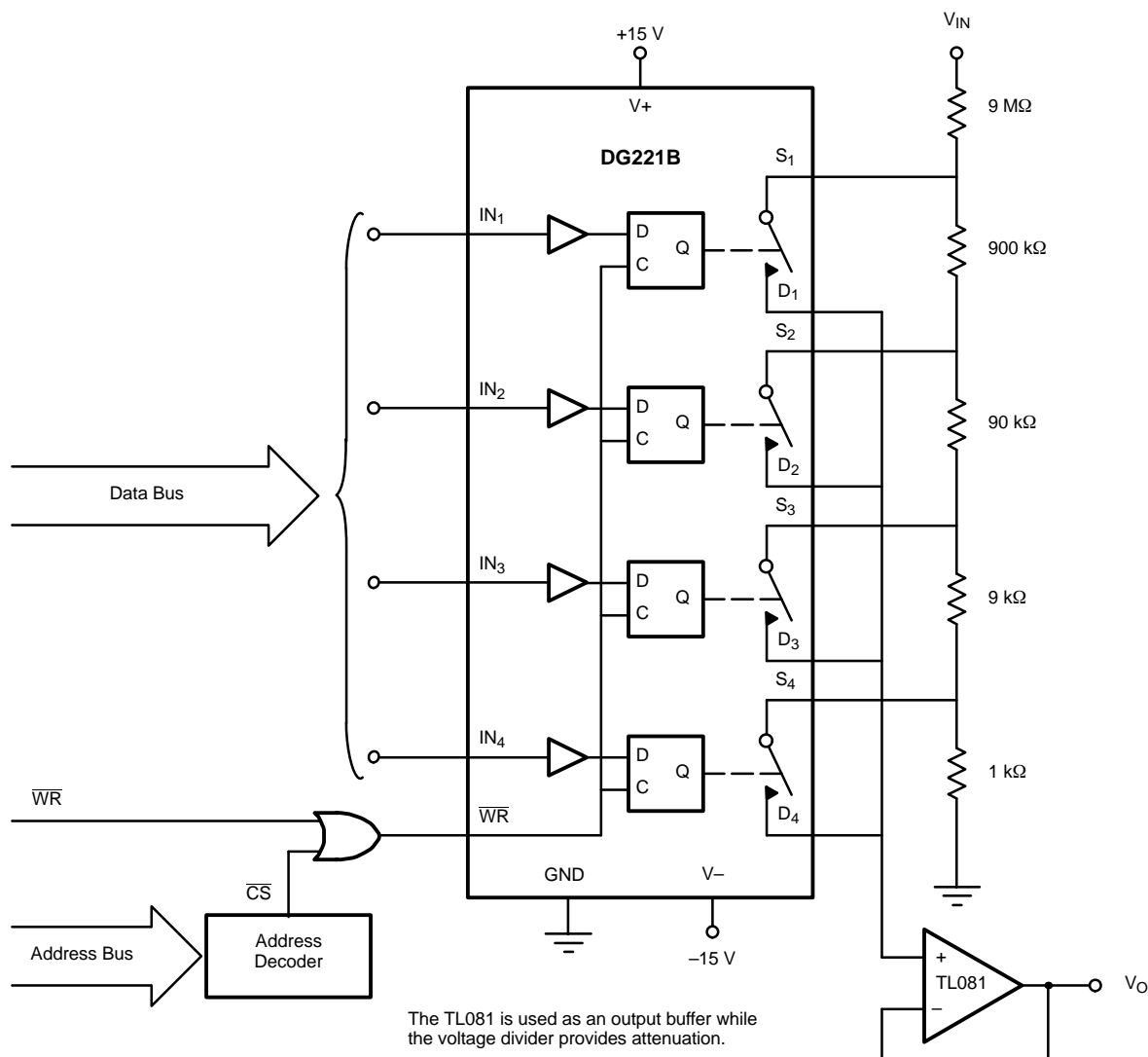
FIGURE 7. Channel-to-Channel Crosstalk

APPLICATION HINTS <sup>a</sup>					
V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	GND (V)	WR (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH(min)</sub> /V <sub>INL(max)</sub> (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
15	-15	0	2.4/0.8	2.4/0.8	-15 to 15
10	-10	0	2.4/0.8	2.4/0.8	-10 to 10
10	-5	0	2.4/0.8	2.4/0.8	-5 to 10

Notes:

a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**APPLICATIONS**



**FIGURE 8.** μP-Controlled Analog Signal Attenuator

TRUTH TABLE					
IN <sub>1</sub>	IN <sub>2</sub>	IN <sub>3</sub>	IN <sub>4</sub>	WR <sup>A</sup>	ON SWITCH
0	0	0	0	0	All
1	1	1	1	0	None
0	1	1	1	0	1
1	0	1	1	0	2
1	1	0	1	0	3
1	1	1	0	0	4

OUTPUT ATTENUATION FOR FIGURE 8					
WR	IN <sub>1</sub>	IN <sub>2</sub>	IN <sub>3</sub>	IN <sub>4</sub>	Gain
0	0	1	1	1	0.1
0	1	0	1	1	0.01
0	1	1	0	1	0.001
0	1	1	1	0	0.0001

Notes:

a. WR may be held at "0" for temporary operation similar to DG201A/DG201B. With WR at "0" SW<sub>1</sub> will remain on as long as IN<sub>1</sub> is held at "0".