

**CMOS Quad SPST Analog Switch**

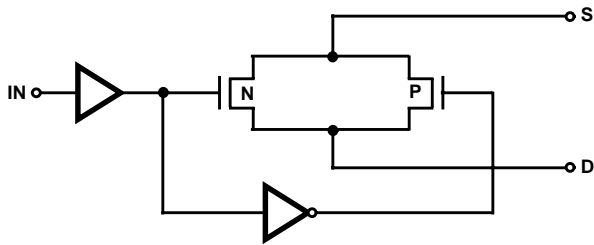
The DG201 solid state analog switch is designed using an improved, high voltage CMOS monolithic technology. It provides ease-of-use and performance advantages not previously available from solid state switches. Destructive latch-up of solid state analog gates have been eliminated by Intersil's CMOS technology.

The DG201 is completely specification and pinout compatible with the industry standard devices.

**Ordering Information**

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG201CJ	0 to 70	16 Ld PDIP	E16.3

**Functional Diagram**



DG201 SWITCH CELL

TRUTH TABLE

LOGIC	DG201
0	ON
1	OFF

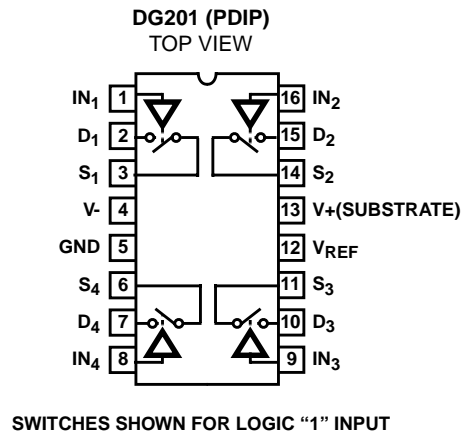
**Features**

- Switches Greater than 28V<sub>P-P</sub> Signals with ±15V Supplies
- Break-Before-Make Switching
  - t<sub>OFF</sub> .....250ns
  - t<sub>ON</sub> .....700ns
- TTL, DTL, CMOS, PMOS Compatible
- Non-Latching with Supply Turn-Off
- Complete Monolithic Construction
- Industry Standard (DG201)

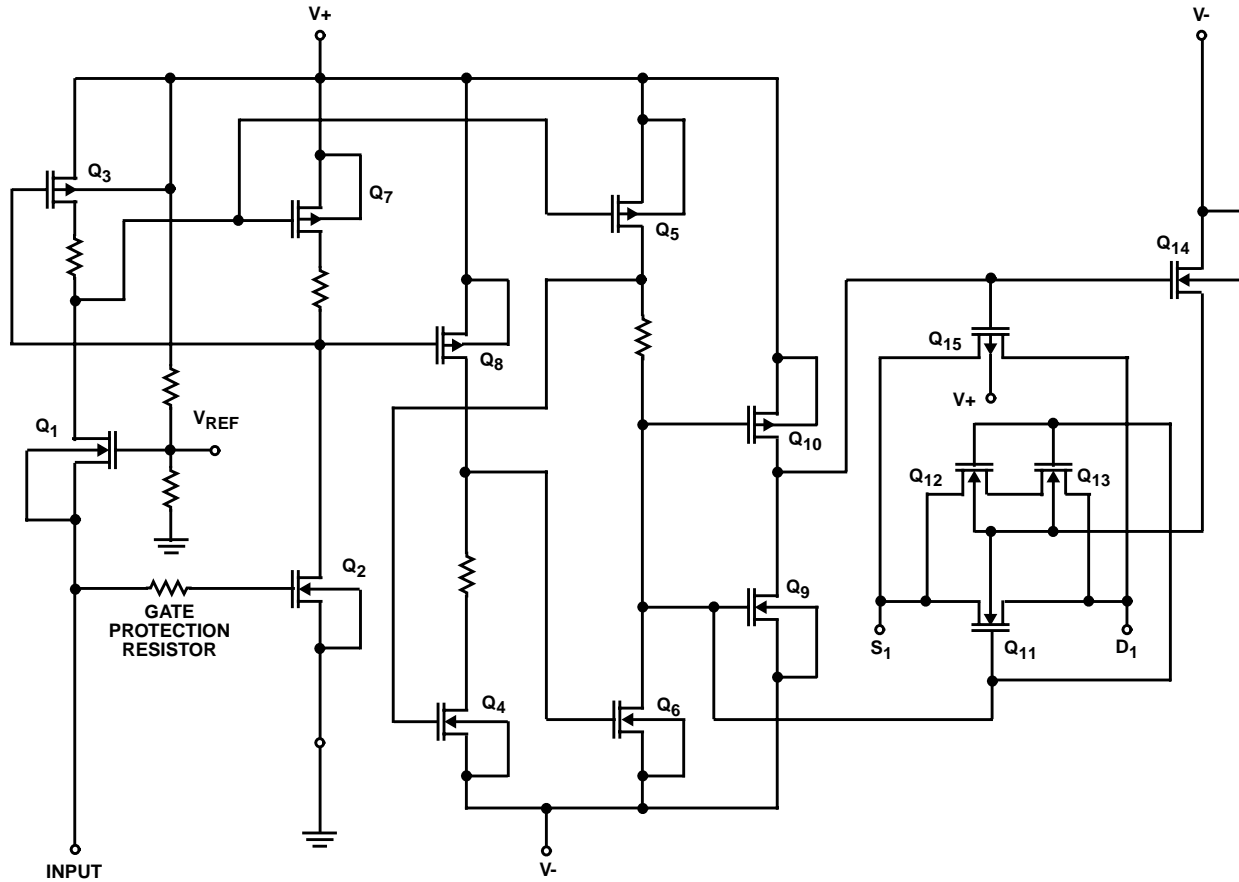
**Applications**

- Data Acquisition
- Sample and Hold Circuits
- Operational Amplifier Gain Switching Networks

**Pinout**



**Functional Diagram** ( $1/4$  DG201)



**Pin Descriptions**

PIN	SYMBOL	DESCRIPTION
1	IN <sub>1</sub>	Logic Control for Switch 1
2	D <sub>1</sub>	Drain (Output) Terminal for Switch 1
3	S <sub>1</sub>	Source (Input) Terminal for Switch 1
4	V-	Negative Power Supply Terminal
5	GND	Ground Terminal (Logic Common)
6	S <sub>4</sub>	Source (Input) Terminal for Switch 4
7	D <sub>4</sub>	Drain (Output) Terminal for Switch 4
8	IN <sub>4</sub>	Logic Control for Switch 4
9	IN <sub>3</sub>	Logic Control for Switch 3
10	D <sub>3</sub>	Drain (Output) Terminal for Switch 3
11	S <sub>3</sub>	Source (Input) Terminal for Switch 3
12	V <sub>REF</sub>	Logic Reference Voltage
13	V+	Positive Power Supply Terminal (Substrate)
14	S <sub>2</sub>	Source (Input) Terminal for Switch 2
15	D <sub>2</sub>	Drain (Output) Terminal for Switch 2
16	IN <sub>2</sub>	Logic Control for Switch 2

**Absolute Maximum Ratings**

V+ to V-	36V
V+ to V <sub>D</sub>	30V
V <sub>D</sub> to V-	30V
V <sub>D</sub> to V <sub>S</sub>	28V
V <sub>REF</sub> to V-	33V
V <sub>REF</sub> to V <sub>IN</sub>	30V
V <sub>REF</sub> to GND	20V
V <sub>IN</sub> to GND	20V
Current (Any Terminal)	30mA

**Thermal Information**

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)
PDIP Package	90	N/A
Maximum Junction Temperature		
Plastic Package	150°C	
Maximum Storage Temperature Range	-65°C to 150°C	
Maximum Lead Temperature (Soldering 10s)	300°C	

**Operating Conditions**

Temperature Range	
“C” Suffix	0°C to 70°C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

**Electrical Specifications**  $T_A = 25^\circ\text{C}$ , V+ = +15V, V- = -15V

PARAMETER	TEST CONDITIONS	“C” SUFFIX			UNITS
		0°C	(NOTE 2) 25°C	70°C	
<b>DYNAMIC CHARACTERISTICS</b>					
Turn-ON Time (Note 3), t <sub>ON</sub>	R <sub>L</sub> = 1k $\Omega$ , V <sub>ANALOG</sub> = -10V to +10V (Figure 1)	-	1.0	-	$\mu\text{s}$
Turn-OFF Time (Note 3), t <sub>OFF</sub>	R <sub>L</sub> = 1k $\Omega$ , V <sub>ANALOG</sub> = -10V to +10V (Figure 1)	-	0.5	-	$\mu\text{s}$
Charge Injection, Q	Figure 2	-	20 (Typ)	-	mV
Off Isolation Rejection Ratio, OIRR	f = 1MHz, R <sub>L</sub> = 100 $\Omega$ , C <sub>L</sub> $\leq$ 5pF, (Figure 3)	-	50 (Typ)	-	dB
Crosstalk (Channel-to-Channel), CCRR	One Channel Off	-	-50 (Typ)	-	dB
<b>DIGITAL INPUT CHARACTERISTICS</b>					
Input Logic Current, I <sub>IN(ON)</sub>	V <sub>IN</sub> = 0.8V (Note 3)	$\pm 1$	$\pm 1$	$\pm 10$	$\mu\text{A}$
Input Logic Current, I <sub>IN(OFF)</sub>	V <sub>IN</sub> = 2.4V (Note 3)	$\pm 1$	$\pm 1$	$\pm 10$	$\mu\text{A}$
<b>ANALOG SWITCH CHARACTERISTICS</b>					
Analog Signal Range, V <sub>ANALOG</sub>		-	$\pm 15$ (Typ)	-	V
Drain-Source ON Resistance, r <sub>DS(ON)</sub>	I <sub>S</sub> = 10mA, V <sub>ANALOG</sub> = $\pm 10\text{V}$	100	100	125	$\Omega$
Channel-to-Channel r <sub>DS(ON)</sub> Match, r <sub>DS(ON)</sub>		-	30 (Typ)	-	$\Omega$
Drain OFF Leakage Current, I <sub>D(OFF)</sub>	V <sub>ANALOG</sub> = -14V to +14V	-	$\pm 5$	100	nA
Source OFF Leakage Current, I <sub>S(OFF)</sub>	V <sub>ANALOG</sub> = -14V to +14V	-	$\pm 5$	100	nA
Channel ON Leakage Current, I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>D</sub> = V <sub>S</sub> = -14V to +14V	-	$\pm 5$	200	nA
<b>POWER SUPPLY CHARACTERISTICS</b>					
Supply Current, I+ Positive	V <sub>IN</sub> = 0V or V <sub>IN</sub> = 5V	2000	1000	2000	$\mu\text{A}$
Supply Current, I- Negative		2000	1000	2000	$\mu\text{A}$

NOTES:

2. Typical values are for design aid only, not guaranteed and not subject to production testing.
3. All channels are turned off by high “1” logic inputs and all channels are turned on by low “0” inputs; however 0.8V to 2.4V describes the minimum range for switching properly. Peak input current required for transition is typically -120 $\mu\text{A}$ .

**Test Circuits**

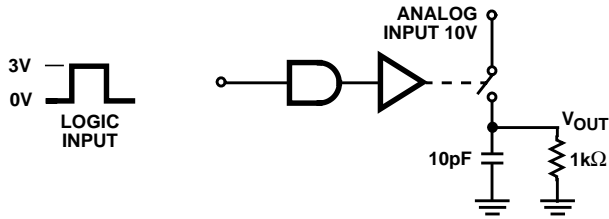


FIGURE 1.  $t_{ON}$  AND  $t_{OFF}$  TEST CIRCUIT

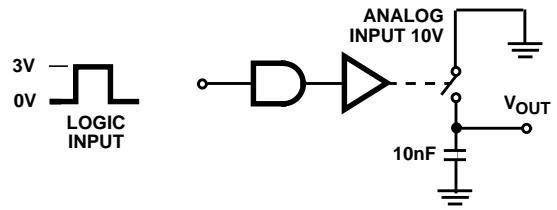


FIGURE 2. CHARGE INJECTION TEST CIRCUIT

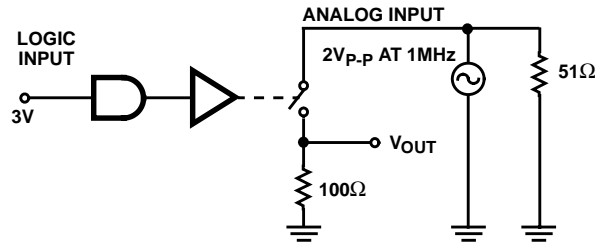


FIGURE 3. OFF ISOLATION TEST CIRCUIT

**Typical Applications**

**Using the  $V_{REF}$  Terminal**

The DG201 has an internal voltage divider setting the TTL threshold on the input control lines for  $V+$  equal to +15V. The schematic shown in Figure 4 with nominal resistor values, gives approximately 2.4V on the  $V_{REF}$  pin. As the TTL input signal goes from +0.8V to +2.4V,  $Q_1$  and  $Q_2$  switch states to turn the switch ON and OFF. If the power supply voltage is less than +15V, then a resistor ( $R_{EXT}$ ) must be added between  $V+$  and the  $V_{REF}$  pin, to restore +2.4V at  $V_{REF}$ . The table shows the value of this resistor for various supply voltages, to maintain TTL compatibility. If CMOS logic levels with a +5V supply are being used, the threshold shifts are less critical, but a separate column of suitable values is given in the table. For logic swings of -5V to +5V, no resistor is needed.

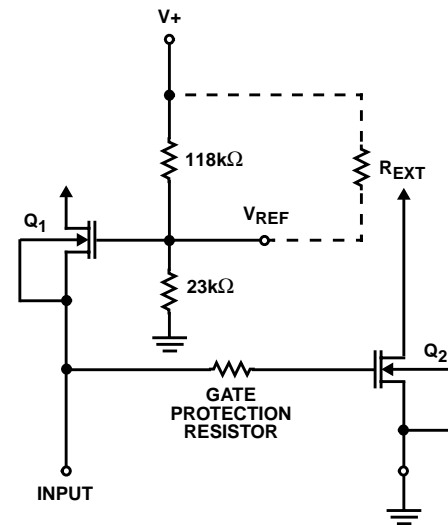


FIGURE 4.

In general, the "low" logic level should be <0.8V to prevent  $Q_1$  and  $Q_2$  from both being ON together (this will cause incorrect switch function).

TABLE 1.

$V+$ SUPPLY (V)	$R_{EXT}$ FOR TTL LEVELS (kΩ)	$R_{EXT}$ FOR CMOS LEVELS (kΩ)
+15	-	-
+12	420	-
+10	190	-
+9	136	136
+8	98	98
+7	70	70

Typical Performance Curves

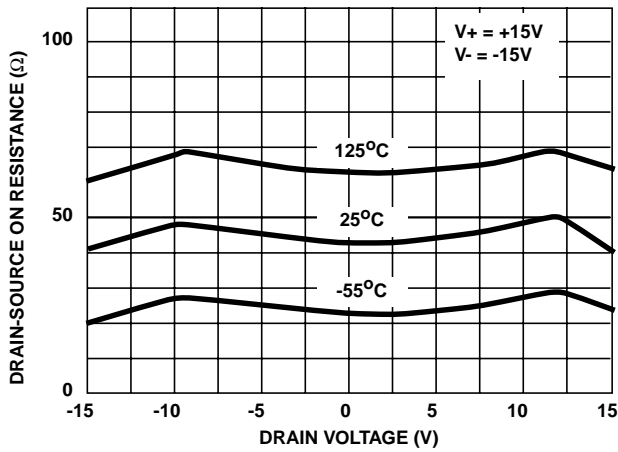


FIGURE 5.  $r_{DS(ON)}$  vs  $V_D$  AND TEMPERATURE

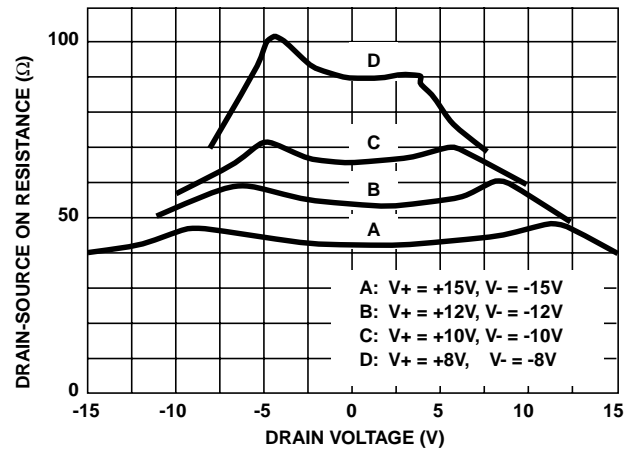


FIGURE 6.  $r_{DS(ON)}$  vs  $V_D$  AND POWER SUPPLY VOLTAGE

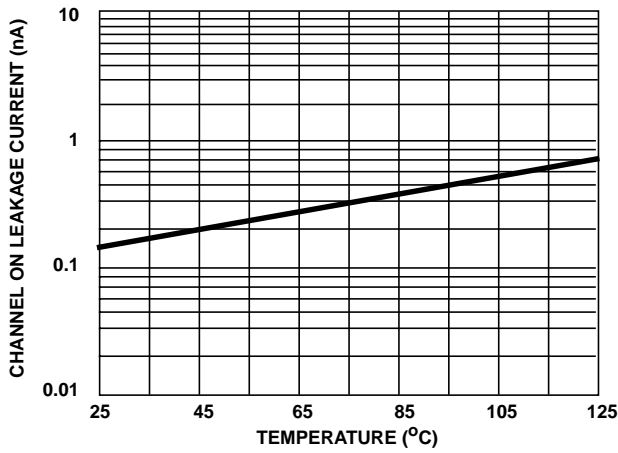


FIGURE 7.  $I_{D(ON)}$  vs TEMPERATURE

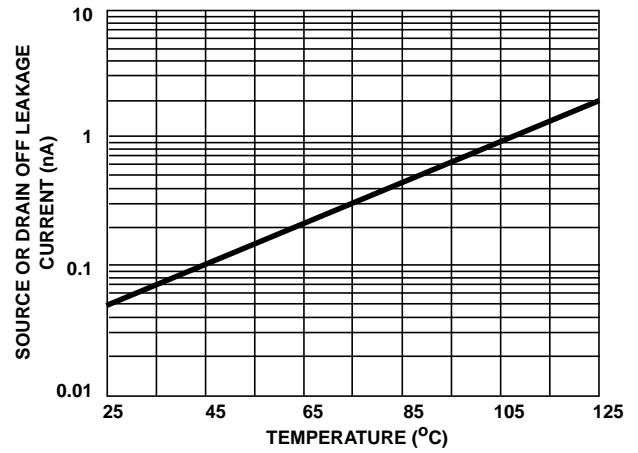


FIGURE 8.  $I_{S(OFF)}$  OR  $I_{D(OFF)}$  vs TEMPERATURE

**Die Characteristics**

**DIE DIMENSIONS:**

94 mils x 101 mils x 14 mils

**METALLIZATION:**

Type: Al  
Thickness: 10kÅ

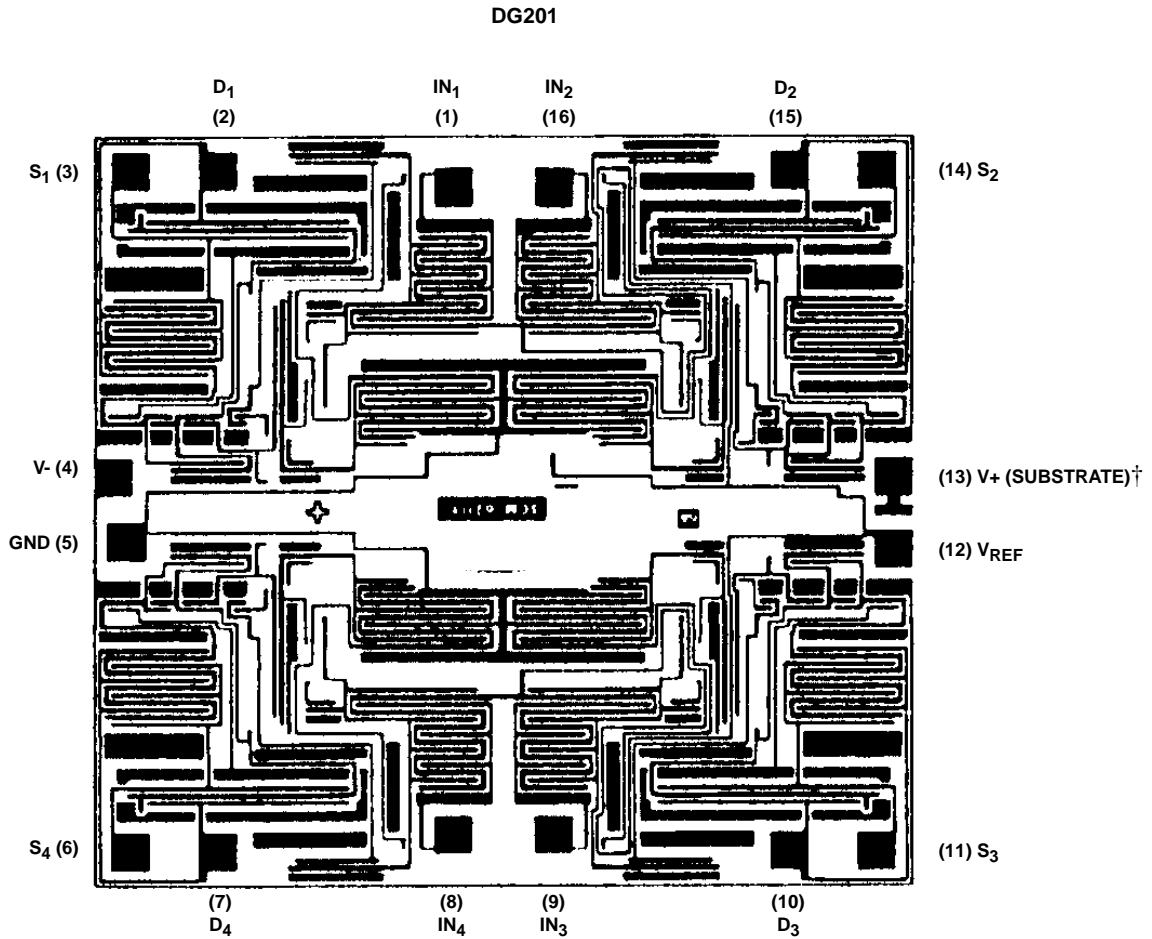
**PASSIVATION:**

Type: SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub>  
SiO<sub>2</sub> Thickness: 7kÅ  
Si<sub>3</sub>N<sub>4</sub> Thickness: 8kÅ

**WORST CASE CURRENT DENSITY:**

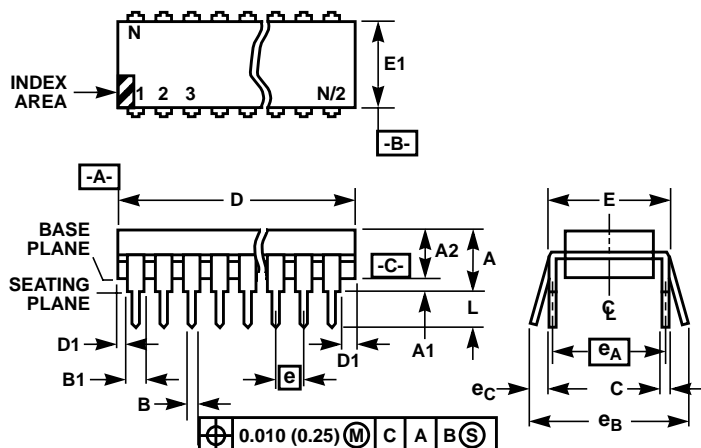
1 x 10<sup>5</sup> A/cm<sup>2</sup>

**Metallization Mask Layout**



† BACKSIDE OF CHIP IS V+

**Dual-In-Line Plastic Packages (PDIP)**



**NOTES:**

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and  $e_A$  are measured with the leads constrained to be perpendicular to datum  $-C-$ .
7.  $e_B$  and  $e_C$  are measured at the lead tips with the leads unconstrained.  $e_C$  must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

**E16.3 (JEDEC MS-001-BB ISSUE D)  
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
$e_A$	0.300 BSC		7.62 BSC		6
$e_B$	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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