FAIRCHILD SEMICONDUCTOR™

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74F825
8-Bit D-Type Flip-Flop

General Description

The 74F825 is an 8-bit buffered register. It has Clock Enable and Clear features which are ideal for parity bus interfacing in high performance microprogramming systems. Also included in the 74F825 are multiple enables that allow multi-user control of the interface.

Features

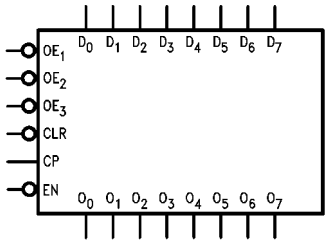
- 3-STATE output
- Clock enable and clear
- Multiple output enables

Ordering Code:

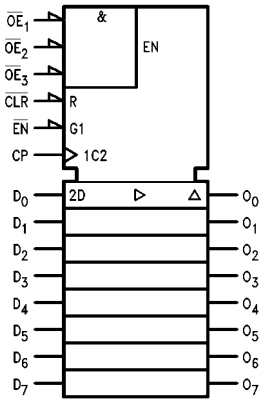
Order Number	Package Number	Package Description
74F825SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F825SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

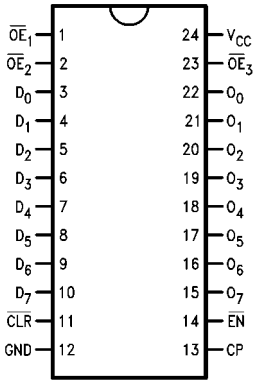
Logic Symbols



IEEE/IEC



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0–D_7	Data Inputs	1.0/1.0	20 µA/–0.6 mA
O_0–O_7	3-STATE Data Outputs	150/40 (33.3)	–3 mA/24 mA (20 mA)
$\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$	Output Enable Input	1.0/1.0	20 µA/–0.6 mA
$\overline{EN}$	Clock Enable	1.0/1.0	20 µA/–0.6 mA
$\overline{CLR}$	Clear	1.0/1.0	20 µA/–0.6 mA
CP	Clock Input	1.0/2.0	20 µA/–1.2 mA

Functional Description

The 74F825 consists of eight D-type edge-triggered flip-flops. This device has 3-STATE true outputs and is organized in broadside pinning. In addition to the clock and output enable pins, the buffered clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH CP transition. With the $\overline{OE}$ LOW the contents of the flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. The 74F825 has Clear ($\overline{CLR}$) and Clock Enable ($\overline{EN}$) pins.

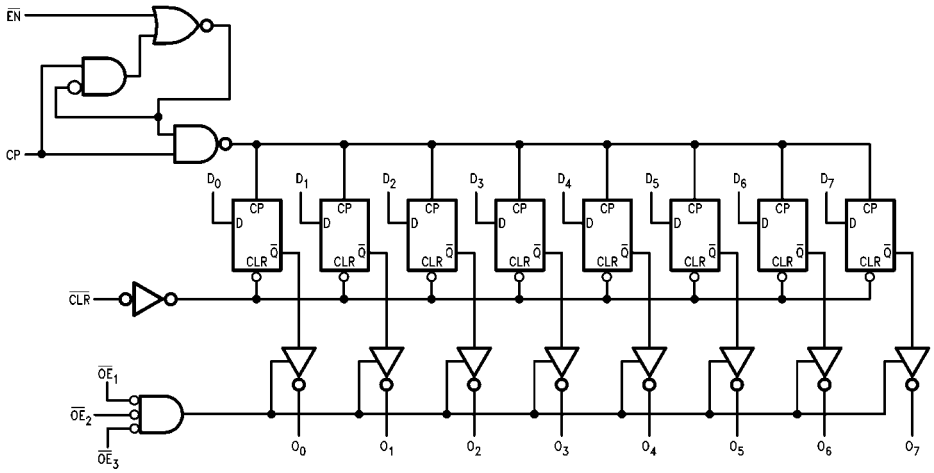
When the $\overline{CLR}$ is LOW and the $\overline{OE}$ is LOW the outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the flip-flops. When $\overline{EN}$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the $\overline{EN}$ is HIGH the outputs do not change state, regardless of the data or clock input transitions.

Function Table

Inputs					Internal	Output	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	D	$\overline{Q}$	O	
H	H	L	H	X	NC	Z	Hold
H	H	L	L	X	NC	Z	Hold
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	L	X	X	X	H	Z	Clear
L	L	X	X	X	H	L	Clear
H	H	L	↗	L	H	Z	Load
H	H	L	↗	H	L	Z	Load
L	H	L	↗	L	H	L	Data Available
L	H	L	↗	H	L	H	Data Available
L	H	L	H	X	NC	NC	No Change in Data
L	H	L	L	X	NC	NC	No Change in Data

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
Z = High Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		10% V_{CC}	2.4					I_{OH} = −3 mA
		5% V_{CC}	2.7					I_{OH} = −1 mA
		5% V_{CC}	2.7					I_{OH} = −3 mA
V_{OL}	Output LOW Voltage	10% V_{CC}			0.5	V	Min	I_{OL} = 24 mA
I_{IH}	Input HIGH Current				5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				7.0	µA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current				50	µA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current				−50	µA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{ZZ}	Buss Drainage Test				500	µA	0.0V	V_{OUT} = 5.25V
I_{CCZ}	Power Supply Current			75	90	mA	Max	V_O = HIGH Z

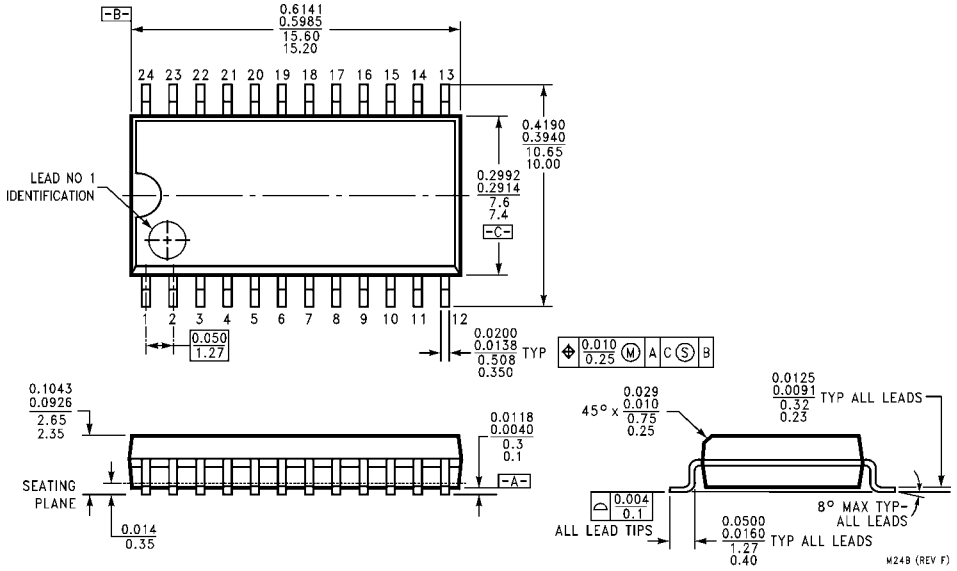
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	100	160		60		70		MHz
t_{PLH}	Propagation Delay	2.0	6.5	9.5	2.0	10.5	2.0	10.5	ns
t_{PHL}	CP to O_n	2.0	6.6	9.5	2.0	10.5	2.0	10.5	
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	4.0	7.4	12.0	4.0	13.0	4.0	13.0	ns
t_{PZH}	Output Enable Time	2.0	6.5	10.5	2.0	13.0	2.0	11.5	ns
t_{PZL}	$\overline{OE}$ to O_n	2.0	6.6	10.5	2.0	13.0	2.0	11.5	
t_{PHZ}	Output Disable TIme	1.5	3.5	7.0	1.0	7.5	1.5	7.5	
t_{PLZ}	$\overline{OE}$ to O_n	1.5	3.3	7.0	1.0	7.5	1.5	7.5	

AC Operating Requirements

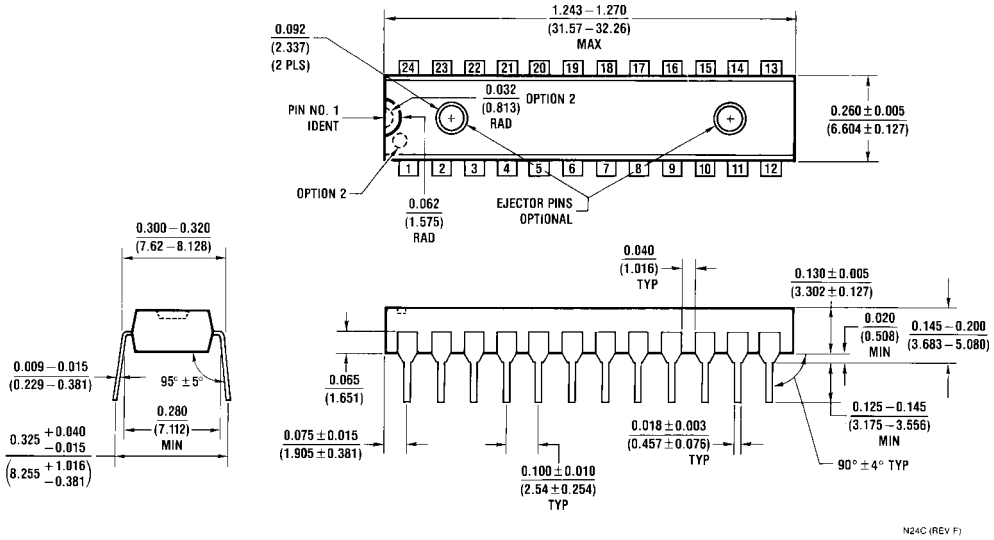
Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$		$T_A = -55°C$ to $+125°C$, $V_{CC} = +5.0V$		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$		Units
		Min	Max	Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW	2.5		4.0		3.0		ns
$t_S(L)$	D_n to CP	2.5		4.0		3.0		
$t_H(H)$	Hold Time, HIGH or LOW	2.5		2.5		2.5		
$t_H(L)$	D_n to CP	2.5		2.5		2.5		
$t_S(H)$	Setup Time, HIGH or LOW	4.5		5.0		5.0		ns
$t_S(L)$	$\overline{EN}$ to CP	2.5		3.0		3.0		
$t_H(H)$	Hold Time, HIGH or LOW	2.0		3.0		1.0		
$t_H(L)$	$\overline{EN}$ to CP	0		2.0		0		
$t_W(H)$	CP Pulse Width	5.0		6.0		6.0		ns
$t_W(L)$	HIGH or LOW	5.0		6.0		6.0		
$t_W(L)$	$\overline{CLR}$ Pulse Width, LOW	5.0		5.0		5.0		ns
t_{REC}	$\overline{CLR}$ Recovery Time	5.0		5.0		5.0		ns

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide
Package Number N24C

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