

74F673A 16-Bit Serial-In, Serial/Parallel-Out Shift Register

General Description

The 74F673A contains a 16-bit serial-in, serial-out shift register and a 16-bit Parallel-Out storage register. A single pin serves either as an input for serial entry or as a 3-STATE serial output. In the Serial-Out mode, the data recirculates in the shift register. By means of a separate clock, the contents of the shift register are transferred to the storage register for parallel outputting. The contents of the storage register can also be parallel loaded back into the shift register. A HIGH signal on the Chip Select input prevents both shifting and parallel transfer. The storage register may be cleared via STMR.

Features

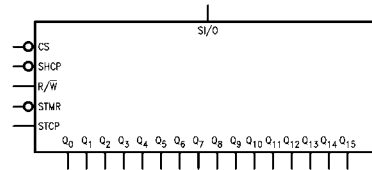
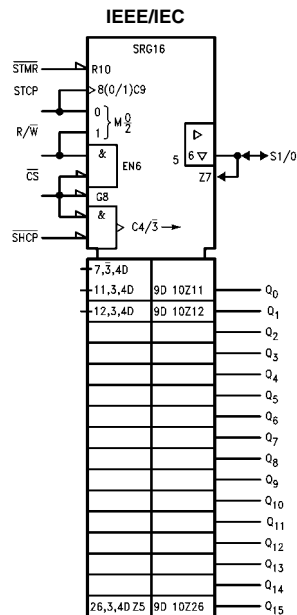
- Serial-to-parallel converter
- 16-bit serial I/O shift register
- 16-bit parallel-out storage register
- Recirculating serial shifting
- Recirculating parallel transfer
- Common serial data I/O pin
- Slim 24 lead package

Ordering Code:

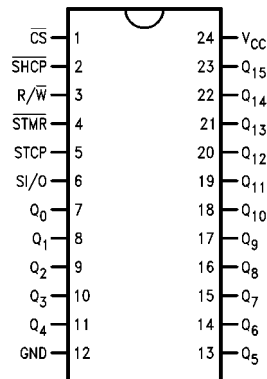
| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| 74F673ASC | M24B | 24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide |
| 74F673APC | N24A | 24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600 Wide |
| 74F673ASPC | N24C | 24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

| Pin Names | Description | U.L. HIGH/LOW | Input I_{IH}/I_{IL} Output I_{OH}/I_{OL} |
|-------------------|---|------------------|---|
| \overline{CS} | Chip Select Input (Active LOW) | 1.0/1.0 | 20 μ A/-0.6 mA |
| \overline{SHCP} | Shift Clock Pulse Input (Active Falling Edge) | 1.0/1.0 | 20 μ A/-0.6 mA |
| \overline{STMR} | Store Master Reset Input (Active LOW) | 1.0/1.0 | 20 μ A/-0.6 mA |
| STCP | Store Clock Pulse Input | 1.0/1.0 | 20 μ A/-0.6 mA |
| R/ \overline{W} | Read/Write Input | 1.0/1.0 | 20 μ A/-0.6 mA |
| SI/O | Serial Data Input or 3-STATE Serial Output | 3.5/1.0 | 70 μ A/-0.6 mA -3 mA/24 mA |
| Q_0 - Q_{15} | Parallel Data Outputs | 50/33.3 | -1 mA/20 mA |

Functional Description

The 16-bit shift register operates in one of four modes, as indicated in the Shift Register Operations Table. A HIGH signal on the Chip Select (\overline{CS}) input prevents clocking and forces the Serial Input/Output (SI/O) 3-STATE buffer into the high impedance state. During serial shift-out operations, the SI/O buffer is active (i.e., enabled) and the output data is also recirculated back into the shift register. When

parallel loading the shift register from the storage register, serial shifting is inhibited.

The storage register has an asynchronous master reset (\overline{STMR}) input that overrides all other inputs and forces the Q_0 - Q_{15} outputs LOW. The storage register is in the Hold mode when either \overline{CS} or the Read/Write (R/ \overline{W}) input is HIGH. With \overline{CS} and R/ \overline{W} both LOW, the storage register is parallel loaded from the shift register.

Shift Register Operations Table

| Control Inputs | | | | SI/O Status | Operating Mode |
|-----------------|-------------------|-------------------|------|----------------|-------------------------------------|
| \overline{CS} | R/ \overline{W} | \overline{SHCP} | STCP | | |
| H | X | X | X | High Z | Hold |
| L | L | | X | Data In | Serial Load |
| L | H | \sim | L | Data Out | Serial Output with Recirculation |
| L | H | \sim | H | Active | Parallel Load; No Shifting |

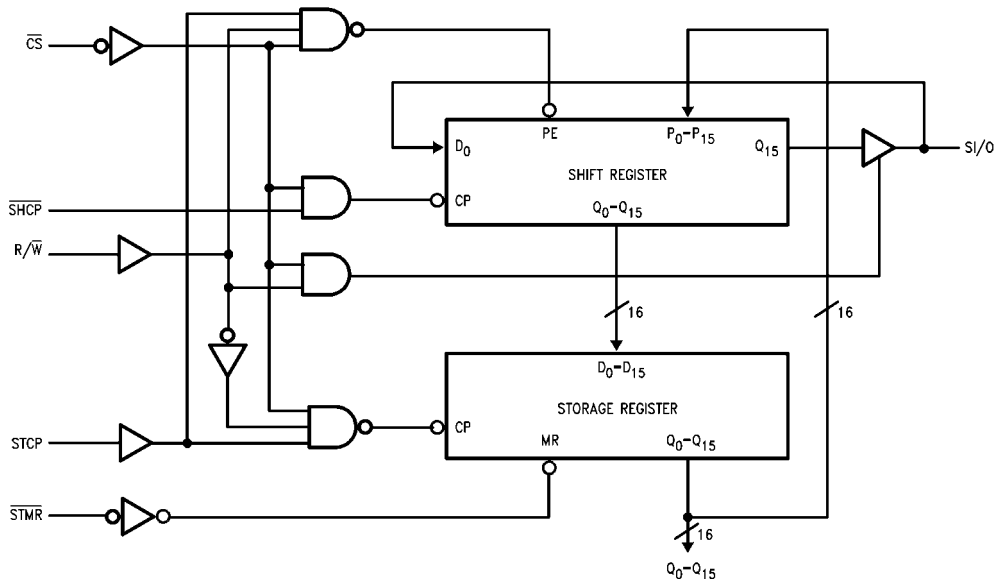
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
 \sim = HIGH-to-LOW Transition

Storage Register Operations Table

| Control Inputs | | | | Operating Mode |
|-------------------|-----------------|-------------------|--------|--------------------|
| \overline{STMR} | \overline{CS} | R/ \overline{W} | STCP | |
| L | X | X | X | Reset; Outputs LOW |
| H | H | X | X | Hold |
| H | X | H | X | Hold |
| H | L | L | \sim | Parallel Load |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
 \sim = LOW-to-HIGH Transition

Block Diagram



Absolute Maximum Ratings (Note 1)

| | |
|--|--------------------------------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature under Bias | -55°C to +125°C |
| Junction Temperature under Bias | -55°C to +150°C |
| V _{CC} Pin Potential to Ground Pin | -0.5V to +7.0V |
| Input Voltage (Note 2) | -0.5V to +7.0V |
| Input Current (Note 2) | -30 mA to +5.0 mA |
| Voltage Applied to Output in HIGH State (with V _{CC} = 0V) | |
| Standard Output | -0.5V to V _{CC} |
| 3-STATE Output | -0.5V to +5.5V |
| Current Applied to Output in LOW State (Max) | twice the rated I _{OL} (mA) |

Recommended Operating Conditions

| | |
|------------------------------|----------------|
| Free Air Ambient Temperature | 0°C to +70°C |
| Supply Voltage | +4.5V to +5.5V |

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

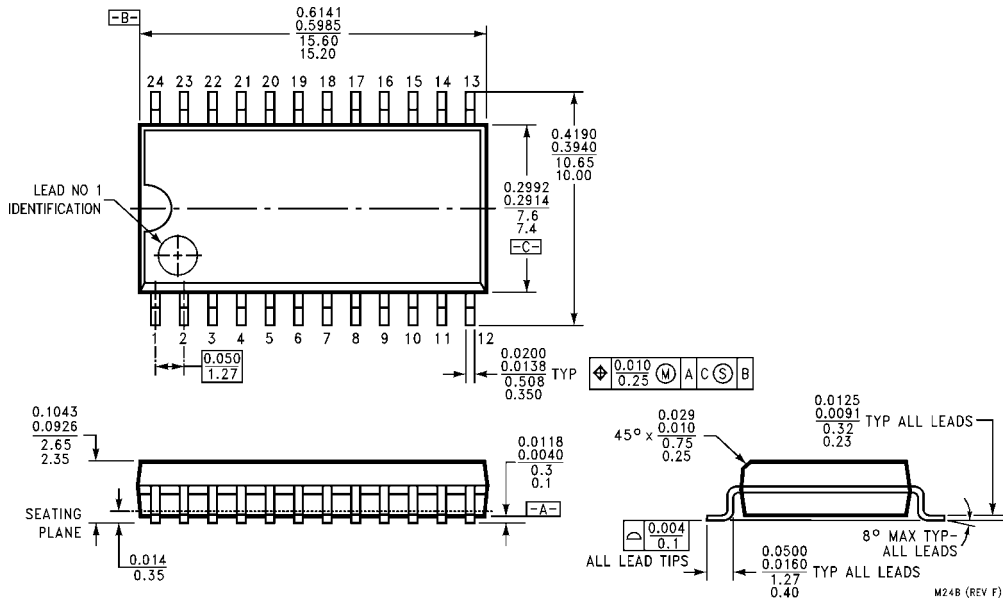
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

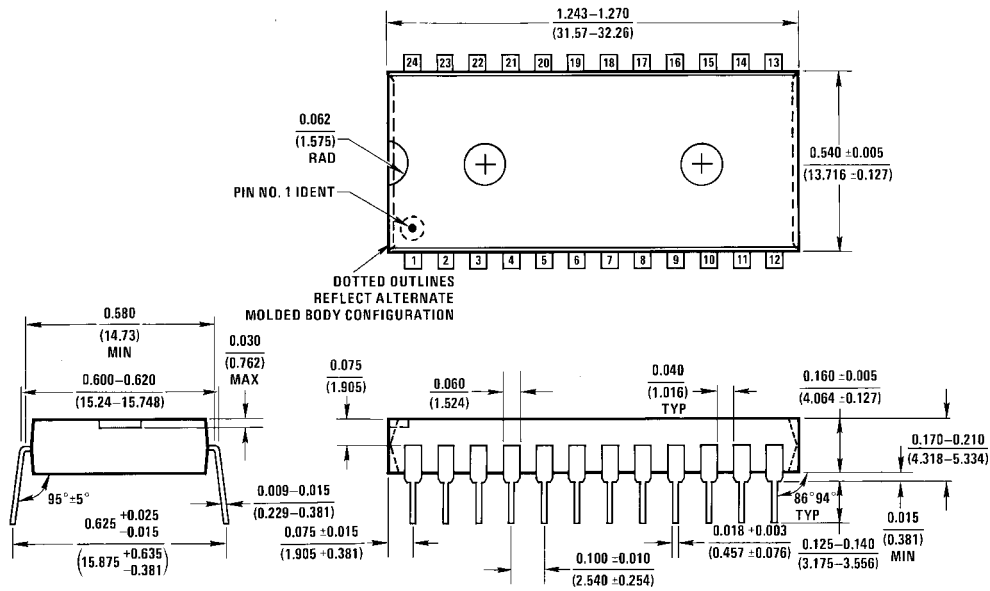
| Symbol | Parameter | Min | Typ | Max | Units | V _{CC} | Conditions |
|---------------------------------------|---|--|--------------------------|------------|-------|-----------------|--|
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | | Recognized as a HIGH Signal |
| V _{IL} | Input LOW Voltage | | | 0.8 | V | | Recognized as a LOW Signal |
| V _{CD} | Input Clamp Diode Voltage | | | -1.2 | V | Min | I _{IN} = -18 mA (Non I/O pins) |
| V _{OH} | Output HIGH Voltage | 10% V _{CC} 10% V _{CC} 5% V _{CC} 5% V _{CC} | 2.5 2.4 2.7 2.7 | | V | Min | I _{OH} = -1 mA (Q _n , SI/O) I _{OH} = -3 mA (SI/O) I _{OH} = -1 mA (Q _n , SI/O) I _{OH} = -3 mA (SI/O) |
| V _{OL} | Output LOW Voltage | 10% V _{CC} 10% V _{CC} | | 0.5 0.5 | V | Min | I _{OL} = 20 mA (Q _n) I _{OL} = 24 mA (SI/O) |
| I _{IH} | Input HIGH Current | | | 20 | μA | Max | V _{IN} = 2.7V (Non I/O pins) |
| I _{BVI} | Input HIGH Current Breakdown Test | | | 100 | μA | Max | V _{IN} = 7.0V (Non I/O pins) |
| I _{BVIT} | Input HIGH Current Breakdown Test (I/O) | | | 1.0 | mA | Max | V _{IN} = 5.5V (SI/O) |
| I _{IL} | Input LOW Current | | | -0.6 | mA | Max | V _{IN} = 0.5V |
| I _{IH} + I _{OZH} | Output Leakage Current | | | 70 | μA | Max | V _{OUT} = 2.7V (SI/O) |
| I _{IL} + I _{OZL} | Output Leakage Current | | | -650 | μA | Max | V _{OUT} = 0.5V (SI/O) |
| I _{OS} | Output Short-Circuit Current | -60 | | -150 | mA | Max | V _{OUT} = 0V |
| I _{CEX} | Output HIGH Leakage Current | | | 250 | μA | Max | V _{OUT} = V _{CC} |
| I _{ZZ} | Bus Drainage Test | | | 500 | μA | 0.0V | V _{OUT} = 5.25V |
| I _{CCH} | Power Supply Current | | 114 | 172 | mA | Max | V _O = HIGH |
| I _{CCL} | Power Supply Current | | 114 | 172 | mA | Max | V _O = LOW |

| AC Electrical Characteristics | | | | | | | |
|-------------------------------|---|---|------|--|--|-------|-------|
| Symbol | Parameter | T _A = +25°C V _{CC} = +5.0V C _L = 50 pF | | | T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF | | Units |
| | | Min | Typ | Max | Min | Max | |
| f _{MAX} | Maximum Clock Frequency | 100 | 130 | | 85 | | MHz |
| t _{PLH} | Propagation Delay | 3.0 | 8.0 | 10.5 | 2.5 | 12.0 | ns |
| t _{PHL} | STCP to Q _n | 3.0 | 10.5 | 13.5 | 2.5 | 15.0 | |
| t _{PHL} | Propagation Delay STMR to Q _n | 6.0 | 16.5 | 20.5 | 5.5 | 22.5 | ns |
| t _{PLH} | Propagation Delay | 4.0 | 6.5 | 8.5 | 3.5 | 9.5 | ns |
| t _{PHL} | SHCP to SI/O | 4.5 | 8.0 | 10.5 | 4.0 | 12.0 | |
| t _{PZH} | Output Enable Time | 5.0 | 8.5 | 11.0 | 4.0 | 12.5 | ns |
| t _{PZL} | $\overline{\text{CS}}$ to SI/O | 5.5 | 9.0 | 11.5 | 4.5 | 13.0 | |
| t _{PHZ} | Output Disable Time | 3.5 | 5.5 | 7.5 | 3.0 | 8.5 | |
| t _{PLZ} | $\overline{\text{CS}}$ to SI/O | 3.0 | 4.5 | 6.5 | 2.5 | 7.5 | |
| t _{PZH} | Output Enable Time | 4.5 | 7.5 | 9.5 | 4.0 | 10.5 | ns |
| t _{PZL} | R $\overline{\text{W}}$ to SI/O | 4.5 | 8.0 | 10.0 | 4.0 | 11.5 | |
| t _{PHZ} | Output Disable Time | 3.0 | 5.5 | 7.0 | 2.5 | 8.0 | |
| t _{PLZ} | R $\overline{\text{W}}$ to SI/O | 2.5 | 4.0 | 5.5 | 2.0 | 6.5 | |
| AC Operating Requirements | | | | | | | |
| Symbol | Parameter | T _A = +25°C V _{CC} = +5.0V | | T _A = 0°C to +70°C V _{CC} = +5.0V | | Units | |
| | | Min | Max | Min | Max | | |
| t _S (H) | Setup Time, HIGH or LOW | 3.5 | | 4.0 | | ns | |
| t _S (L) | $\overline{\text{CS}}$ or R $\overline{\text{W}}$ to STCP | 6.0 | | 7.0 | | | |
| t _H (H) | Hold Time, HIGH or LOW | 0 | | 0 | | | |
| t _H (L) | $\overline{\text{CS}}$ or R $\overline{\text{W}}$ to STCP | 0 | | 0 | | ns | |
| t _S (H) | Setup Time, HIGH or LOW | 3.0 | | 3.5 | | | |
| t _S (L) | SI/O to SHCP | 3.0 | | 3.5 | | | |
| t _H (H) | Hold Time, HIGH or LOW | 3.0 | | 3.5 | | | |
| t _H (L) | SI/O to SHCP | 3.0 | | 3.5 | | | |

Physical Dimensions inches (millimeters) unless otherwise noted

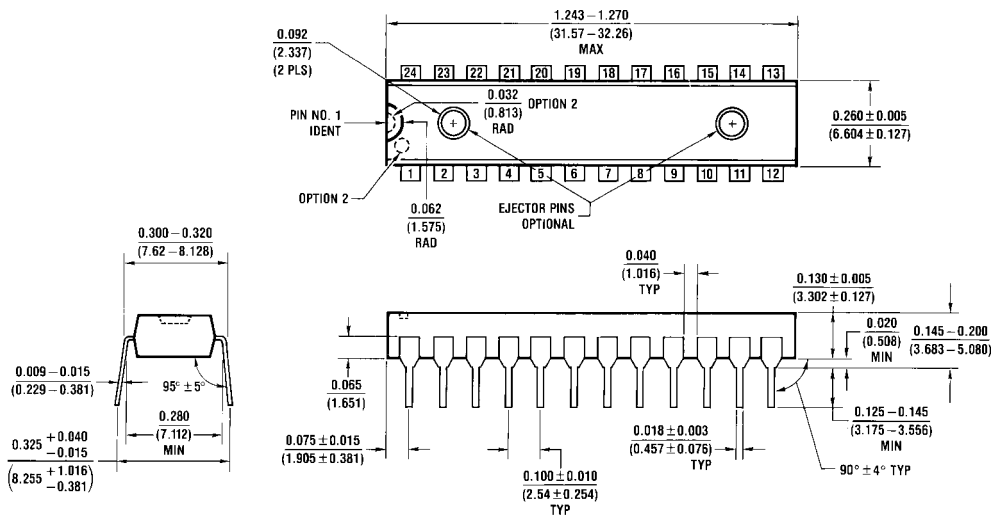


24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide Package Number M24B



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600 Wide Package Number N24A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide
Package Number N24C**

N24C (REV F)

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