

DATA SHEET

74F38

Quad 2-input NAND buffer (open collector)

Product specification

1990 Oct 04

IC15 Data Handbook

Quad 2-input NAND buffer (open collector)

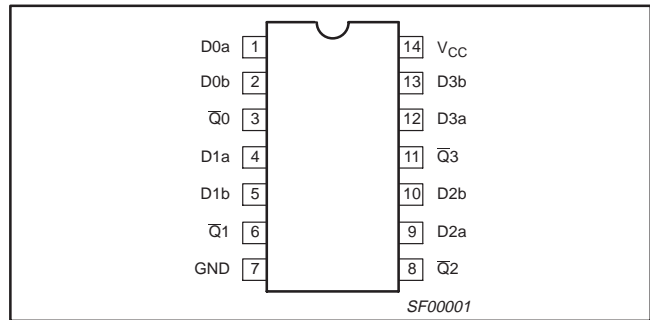
74F38

FEATURE

- Industrial temperature range available (-40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F38	7.0ns	13mA

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	INDUSTRIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$	
14-pin plastic DIP	N74F38N	I74F38N	SOT27-1
14-pin plastic SO	N74F38D	I74F38D	SOT108-1

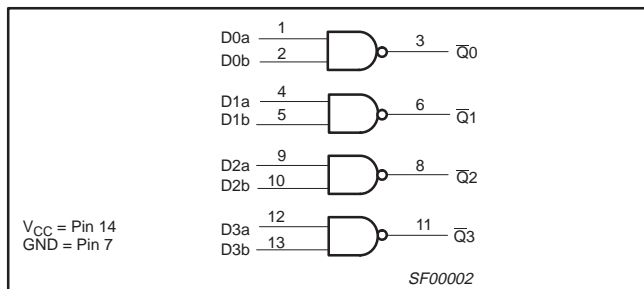
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb	Data inputs	1.0/2.0	20µA/1.2mA
\bar{Q}_n	Data output	OC/106.7	OC/64mA

NOTES:

- One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.
- OC = open collector

LOGIC DIAGRAM



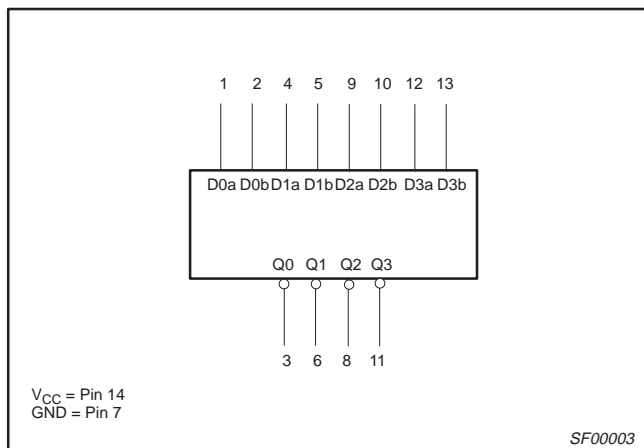
FUNCTION TABLE

INPUTS		OUTPUT
Dna	Dnb	\bar{Q}_n
L	L	H
L	H	H
H	L	H
H	H	L

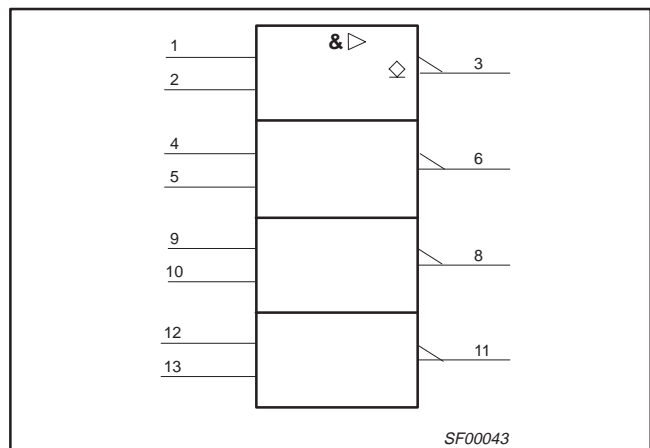
NOTES:

- H = High voltage level
- L = Low voltage level

LOGIC SYMBOL



IEC/IEEE SYMBOL



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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		128	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	-40 to +85	°C
T_{stg}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			64	mA
T_{amb}	Operating free air temperature range	Commercial range	0	+70	°C
		Industrial range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT
			MIN	TYP ²	MAX	
I_{OH}	High-level output current	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, V_{OH} = \text{MAX}$			250	μA
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$	$\pm 10\%V_{CC}$		0.55	V
		$V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$	$\pm 5\%V_{CC}$	0.42	0.55	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$		-0.73	-1.2	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$			100	μA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$			20	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$			-1.2	mA
I_{CC}	Supply current (total)	I_{CCH} $V_{CC} = \text{MAX}$	$V_{IN} = \text{GND}$	4.0	7.0	mA
		I_{CCL} $V_{CC} = \text{MAX}$	$V_{IN} = 4.5\text{V}$	22	30	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_{amb} = 25^\circ\text{C}$.

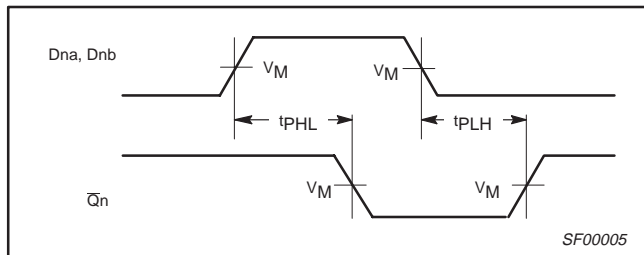
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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT	
			$V_{CC} = +5.0V$ $T_{amb} = +25^{\circ}C$ $C_L = 50pF, R_L = 500\Omega$			$V_{CC} = +5.0V \pm 10\%$ $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$ $C_L = 50pF, R_L = 500\Omega$		$V_{CC} = +5.0V \pm 10\%$ $T_{amb} = -40^{\circ}C \text{ to } +85^{\circ}C$ $C_L = 50pF, R_L = 500\Omega$		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to \bar{Q}_n	Waveform 1	7.5	10.0	12.5	7.5	13.0	7.5	14.5	ns
			1.5	3.0	5.0	1.5	5.5	1.5	6.0	

AC WAVEFORMS

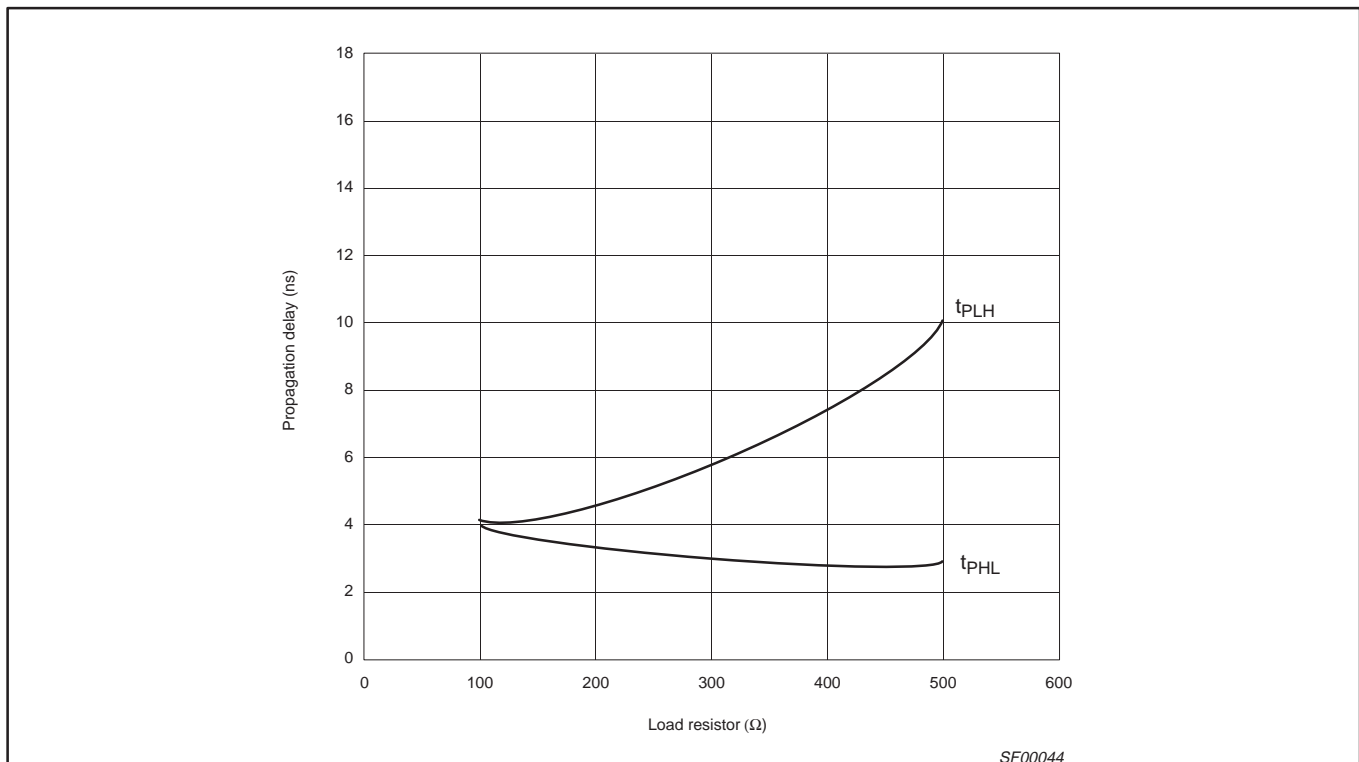


Waveform 1. Propagation delay for inverting outputs

NOTE:

For all waveforms, $V_M = 1.5V$.

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



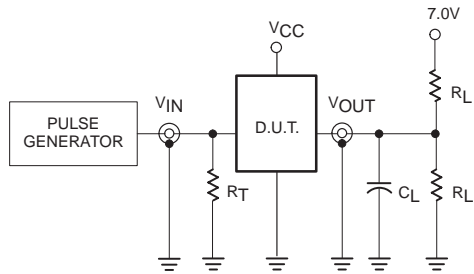
NOTE:

1 When using open collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH} . For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL} . However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL} 's of the receivers does not exceed the I_{OL} minimum specification.

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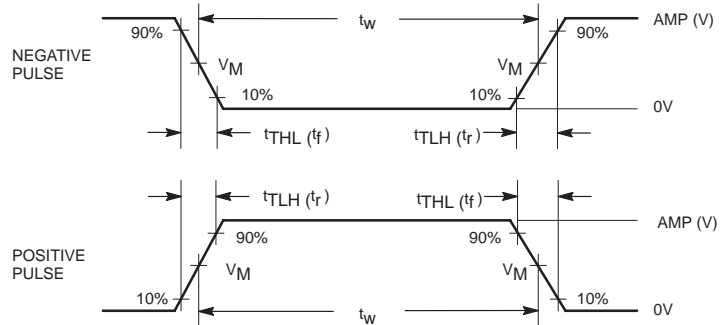
TEST CIRCUIT AND WAVEFORM



Test Circuit for Open Collector Outputs

DEFINITIONS:

- R_L = Load resistor; see AC electrical characteristics for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

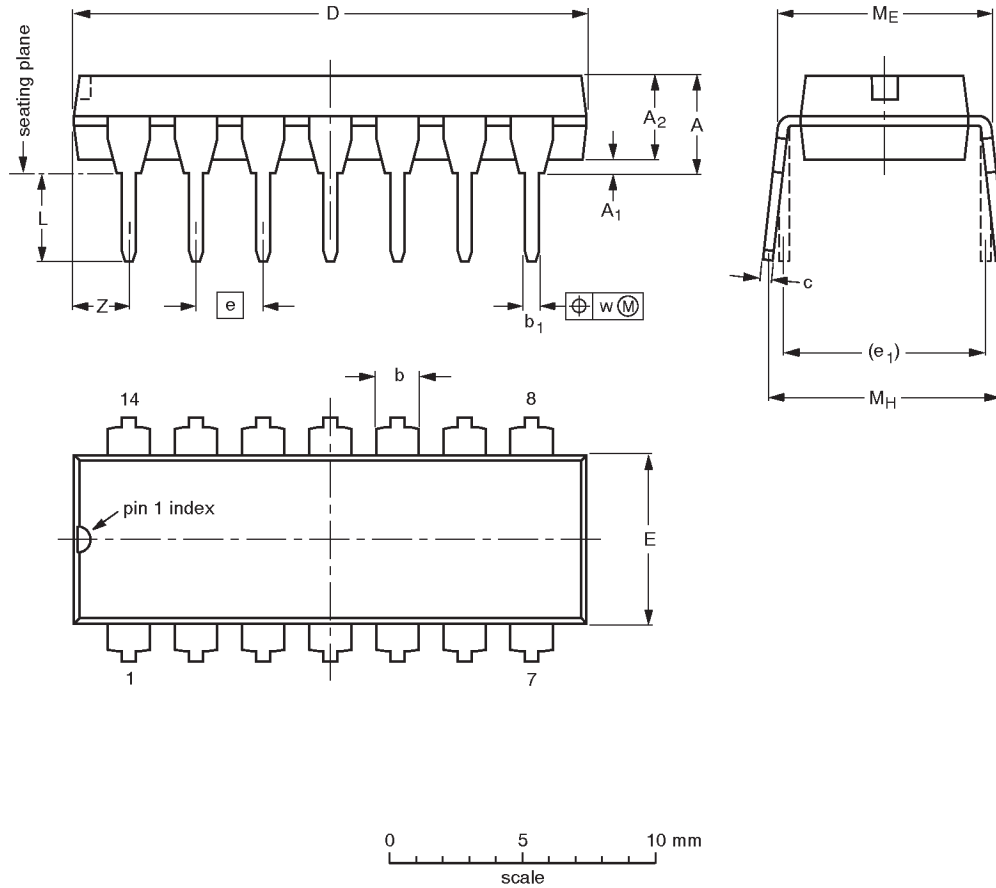
SF00027

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DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

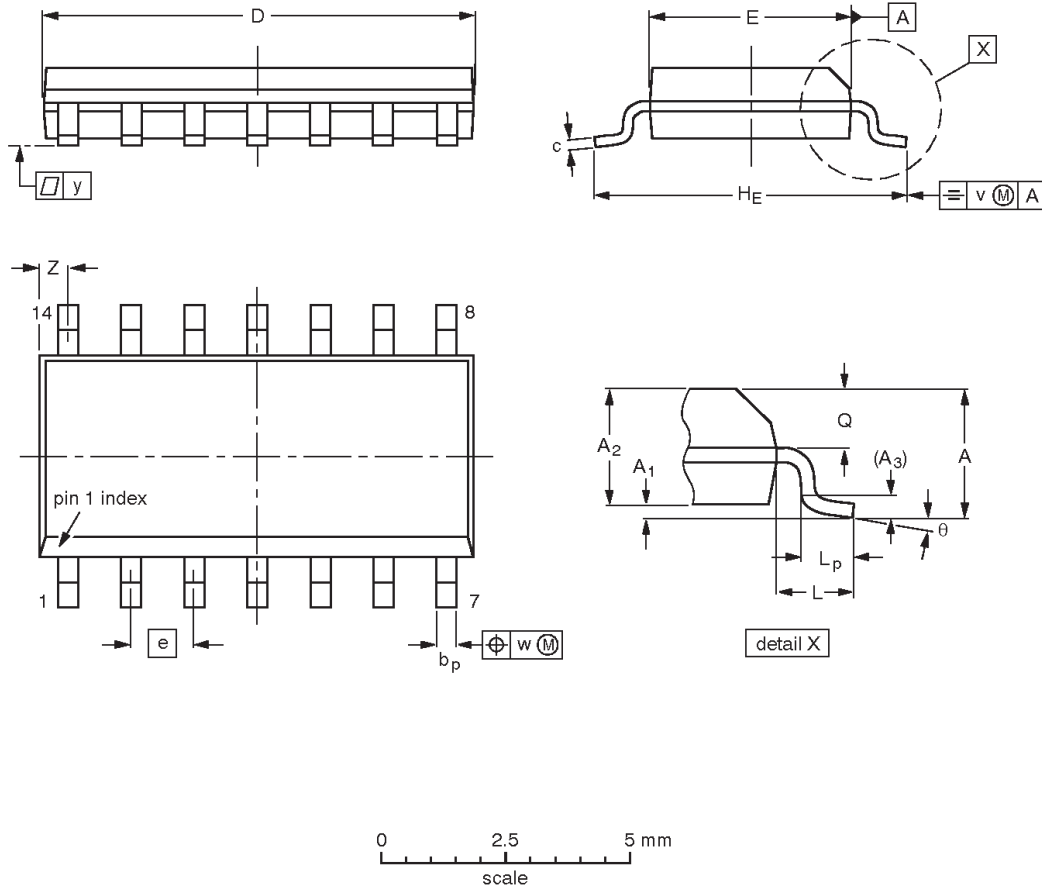
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT27-1	050G04	MO-001AA			92-11-17 95-03-11

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				95-01-29 97-05-22

Quad 2-input NAND buffer (open collector)

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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