# INTEGRATED CIRCUITS

# DATA SHEET

# **74F3037** Quad 2-input NAND $30\Omega$ driver

Product specification

1990 Feb 09

IC15 Data Handbook





74F3037

#### **FEATURES**

- 30Ω line driver
- 67mA output drive capability in the high state
- High speed
- Facilitates incident wave switching
- 3nh lead inductance each on V<sub>CC</sub> and GND when both side pins are used
- 160mA output drive capability in the low state
- Industrial temperature range available (-40°C to +85°C)

### **DESCRIPTION**

The 74F3037 is a high current line driver composed of four 2—input NAND gates. It has been designed to deal with the

transmission line effects of PC boards which appear when fast edge rates are used.

The drive capability of the 74F3037 is 67mA source and 160mA sink with a  $V_{CC}$  as low as 4.5V. This guarantees incident wave switching with  $V_{OH}$  not less than 2.0V and  $V_{OL}$  not more than 0.8mA while driving impedances as low as 30 ohms. This is applicable with any combination of outputs using continuous duty. The propagation delay of the part is minimally affected by reflections when terminated only by the TTL inputs of other devices. Performances may be improved by full or partial line termination.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT( TOTAL)
74F3037	2.0ns	16mA

# ORDERING INFORMATION

	C		
DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$	INDUSTRIAL RANGE $V_{CC} = 5V \pm 10\%,$ $T_{amb} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	PKG DWG#
16-pin plastic DIP	N74F3037N	I74F3037N	SOT38-4
16-pin plastic SOL	N74F3037D	I74F3037D	SOT162-1

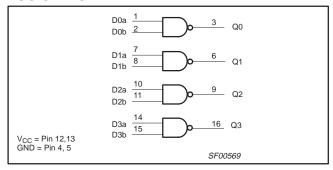
# INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb	Data inputs	1.0/1.0	20μA/0.6mA
Qn	Data output	3350/266	67mA/160mA

Note to input and output loading and fan out table

One (1.0) FAST unit load is defined as:  $20\mu A$  in the high state and 0.6mA in the low state.

### LOGIC DIAGRAM



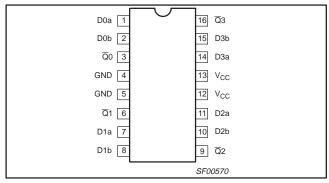
### **FUNCTION TABLE**

INP	UTS	OUTPUT
Dna	Dnb	Qn
L	L	Н
L	Н	Н
Н	L	Н
Н	Н	Ĺ

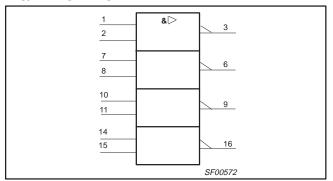
Notes to function table H = High voltage level L = Low voltage level

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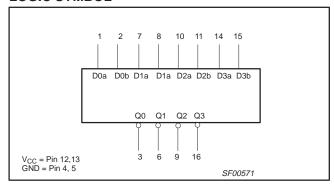
# **PIN CONFIGURATION**



# **IEC/IEEE SYMBOL**



# **LOGIC SYMBOL**



# **ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V <sub>CC</sub>	Supply voltage		-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage		-0.5 to +7.0	V
I <sub>IN</sub>	Input current		-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in high output state		$-0.5$ to $V_{CC}$	V
I <sub>OUT</sub>	Current applied to output in low output state		320	mA
T <sub>amb</sub>	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	-40 to +85	°C
T <sub>stg</sub>	Storage temperature range		-65 to +150	°C

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### RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER			LIMITS		T <sub>A</sub> =
UNIT			MIN	NOM	MAX	–40 to +85°C
V <sub>CC</sub>	Supply voltage		4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage		2.4			V
V <sub>IL</sub>	Low-level input voltage			0.8	V	
I <sub>lk</sub>	Input clamp current				-18	mA
I <sub>OH</sub>	High-level output current				-67	mA
I <sub>OL</sub>	Low-level output current				160	mA
T <sub>amb</sub>	Operating free air temperature range	Commercial range	0		+70	°C
			-40		+85	°C

# DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST LIMITS								
		CONDITIONS <sup>1</sup>									
			V <sub>CC</sub> = MIN,	$I_{OH} = -45 \text{mA}$	±10%V <sub>CC</sub>	2.5			V		
V <sub>OH</sub>	High-level output voltage		$V_{IL} = MAX,$		±5%V <sub>CC</sub>	2.7			V		
			V <sub>IH</sub> = MIN	I <sub>OH1</sub> = -67mA <sup>3</sup>	±10%V <sub>CC</sub>	2.0			V		
V <sub>OL</sub>	Low-level output voltage		V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX,	I <sub>OL</sub> = 100mA	±10%V <sub>CC</sub>		0.30	0.50	V		
			V <sub>IH</sub> = MIN	I <sub>OL1</sub> = 160mA <sup>4</sup>	±5%V <sub>CC</sub>		0.30	0.50	V		
V <sub>IK</sub>	Input clamp voltage		$V_{CC} = MIN, I_I = I_{IK}$				-0.73	-1.2	V		
I <sub>I</sub>	Input current at maximum input vol	tage	$V_{CC} = MAX, V_I = 7.0V$					100	μΑ		
I <sub>IH</sub>	High-level input current		$V_{CC} = MAX, V_I = 2.7V$	$V_{CC} = MAX, V_I = 2.7V$				20	μΑ		
I <sub>IL</sub>	Low-level input current		$V_{CC} = MAX, V_I = 0.5V$					-0.6	mA		
Io	Output current <sup>5</sup>		$V_{CC} = MAX, V_O = 2.25V$	,		-100		-200	mA		
Icc	Supply current (total)	I <sub>CCH</sub>	V <sub>CC</sub> = MAX				6.0	9.0	mA		
		I <sub>CCL</sub>					30	40	mA		

# Notes to DC electrical characteristics

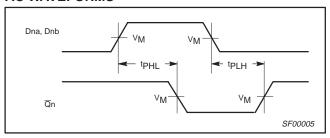
- 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- 2. All typical values are at  $V_{CC} = 5V$ ,  $T_{amb} = 25^{\circ}C$ .
- 3. I<sub>OH1</sub> is the current necessary to guarantee the low to high transition in a 30 ohm transmission line on the incident wave.
  4. I<sub>OL1</sub> is the current necessary to guarantee the high to low transition in a 30 ohm transmission line on the incident wave.
- 5. Io is tested under conditions that produce current approximately one half of the true short-circuit current (Ios).

# **AC ELECTRICAL CHARACTERISTICS**

						LII	MITS			
			Tan	<sub>nb</sub> = +25	°C	$T_{amb} = 0^{\circ}C$	c to +70°C	$T_{amb} = -40^{\circ}$	C to +85°C	1 1
SYMBOL	PARAMETER	TEST	$V_{CC} = +5.0V$		V <sub>CC</sub> = +5.	0V $\pm$ 10%	$V_{CC} = +5.0$	UNIT		
		CONDITION	C <sub>L</sub> = 50pF,		C <sub>L</sub> = 5		$C_L = 50 pF,$ $R_1 = 500 \Omega$			
			$R_L = 500\Omega$		$R_L = 500\Omega$ $R_L = 500\Omega$			$R_L = $	50075	J I
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay Dna, Dnb to Qn	Waveform 1	1.0 1.0	2.0 2.0	5.0 4.5	1.0 1.0	5.5 5.0	1.0 1.0	5.5 5.0	ns

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### **AC WAVEFORMS**

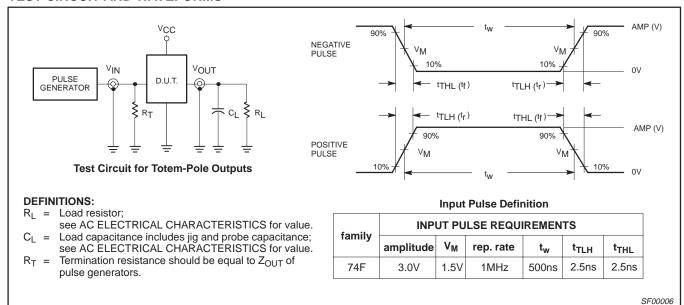


Waveform 1. Propagation delay for inverting outputs

# Note to AC waveforms

For all waveforms,  $V_M = 1.5V$ .

# **TEST CIRCUIT AND WAVEFORMS**



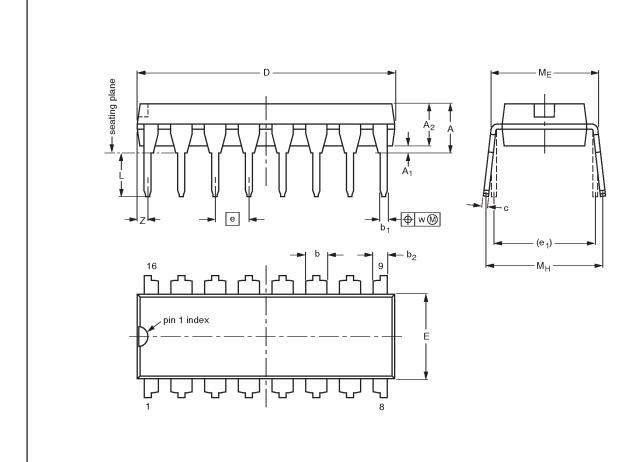
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# DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



# DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	С	D <sup>(1)</sup>	E (1)	е	e <sub>1</sub>	L	ME	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

scale

10 mm

# Note

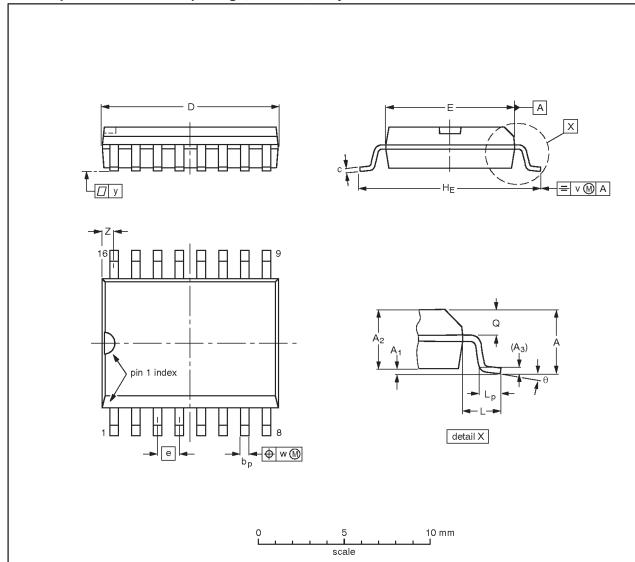
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	RENCES		EUROPEAN	ISSUE DATE	
VERSION	ERSION IEC JEDEC EIAJ				PROJECTION	ISSUE DATE	
SOT38-4						<del>92-11-17</del> 95-01-14	

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# SO16: plastic small outline package; 16 leads; body width 7.5 mm

SOT162-1



# DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	bp	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Q	v	w	у	z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	0°

# Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE		EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE	
SOT162-1	075E03	MS-013AA			<del>95 01 24</del> 97-05-22	

1990 Feb 09

# Quad 2-input NAND 30Ω driver

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Data sheet status	Product status	Definition [1]
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