

# DATA SHEET

**74F269**

**8-bit bidirectional binary counter**

Product specification

1996 Jan 05

IC15 Data Handbook

# 8-bit bidirectional binary counter

# 74F269

## FEATURES

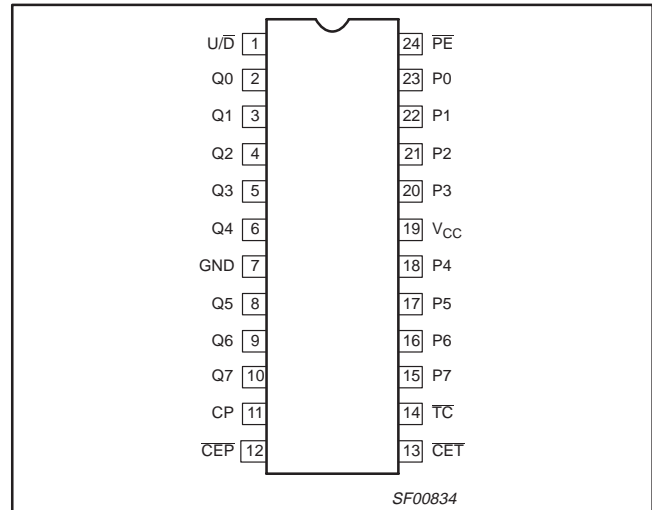
- Synchronous counting and loading
- Built-in look-ahead carry capability
- Count frequency 115MHz typ
- Supply current 95mA typ

## DESCRIPTION

The 74F269 is a fully synchronous 8-stage Up/Down Counter featuring a preset capability for programmable operation, carry look-ahead for easy cascading and a U/D input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

TYPE	TYPICAL f <sub>MAX</sub>	TYPICAL SUPPLY CURRENT (TOTAL)
74F269	115MHz	95mA

## PIN CONFIGURATION



## ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V <sub>CC</sub> = 5V ±10%, T <sub>amb</sub> = 0°C to +70°C	PKG DWG #
24-Pin Plastic Slim DIP (300mil)	N74F269N	SOT222-1
24-Pin Plastic SOL	N74F269D	SOT137-1
24-Pin Plastic SSOP type II	N74F269DB	SOT340-1

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
P0 - P7	Parallel Data inputs	1.0/1.0	20µA/0.6mA
PE	Parallel Enable input (active Low)	1.0/1.0	20µA/0.6mA
U/D	Up/Down count control input	1.0/1.0	20µA/0.6mA
CEP	Count Enable Parallel input (active Low)	1.0/1.0	20µA/0.6mA
CET	Count Enable Trickle input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock input	1.0/1.0	20µA/0.6mA
TC	Terminal Count output (active Low)	50/33	1.0mA/20mA
Q0 - Q7	Flip-flop outputs	50/33	1.0mA/20mA

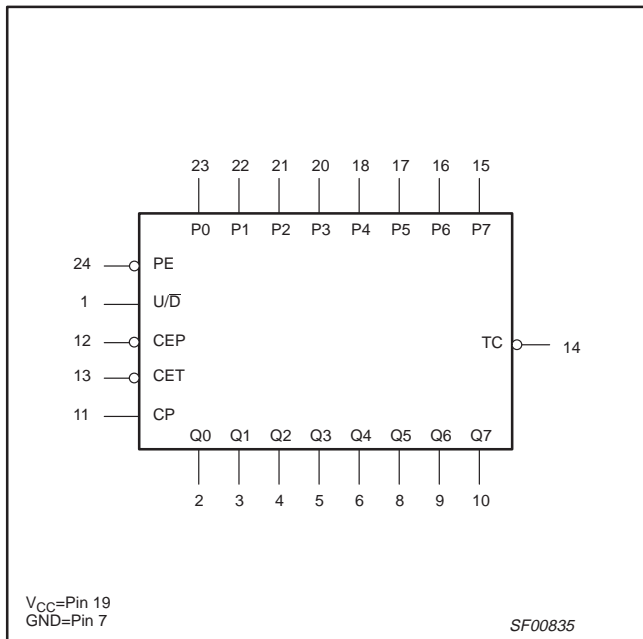
### NOTE:

One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

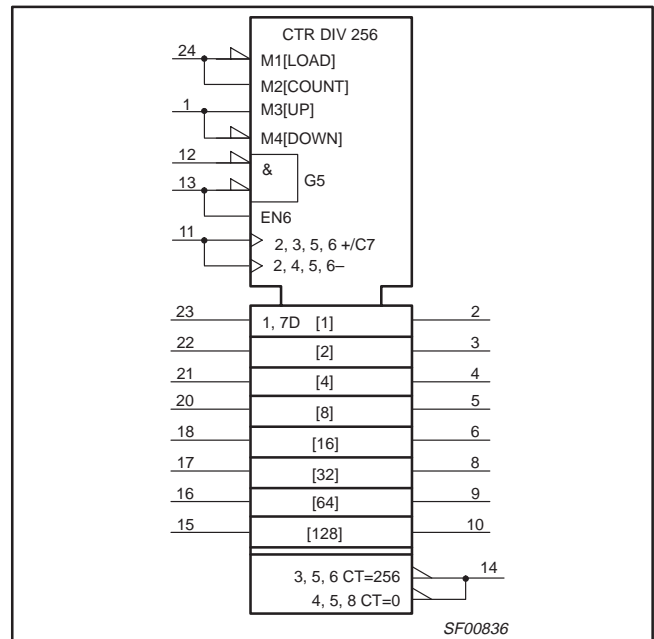
# 8-bit bidirectional binary counter

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## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



## APPLICATION

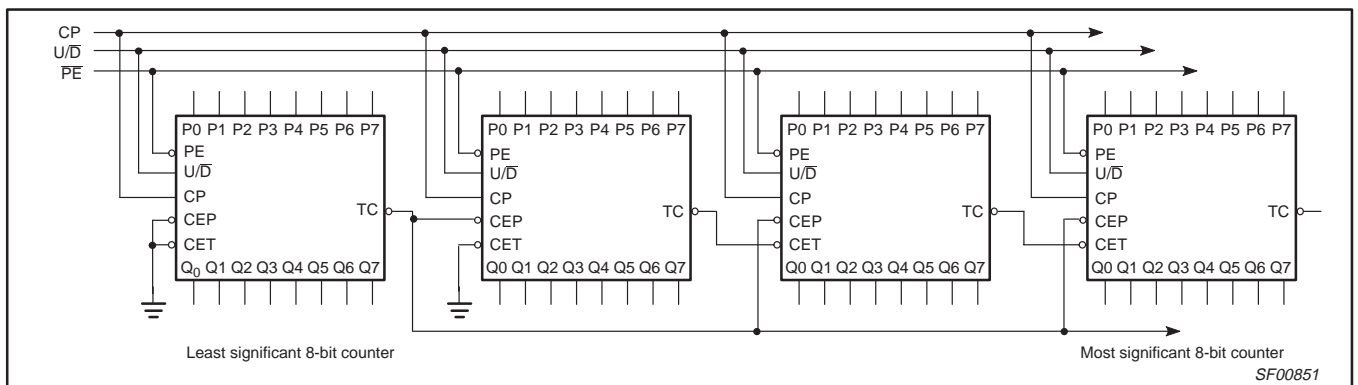


Figure 1. Synchronous Multistage Counting Scheme

## MODE SELECT FUNCTION TABLE

INPUTS						OUTPUTS		OPERATING MODE
CP	U/D	CEP	CET	PE	$P_n$	$Q_n$	TC	
↑	X	X	X	l	l	L	(a)	Parallel load
↑	X	X	X	l	h	H	(a)	
↑	h	l	l	h	X	Count Up	(a)	Count Up
↑	l	l	l	h	X	Count Down	(a)	Count Down
↑	X	h	l	h	X	$q_n$	(a)	Hold (do nothing)
↑	X	X	h	h	X	$q_n$	H	

H = High voltage level

h = High voltage level one setup prior to the Low-to-High clock transition

L = Low voltage level

l = Low voltage level one setup time prior to the Low-to-High clock transition

q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition

X = Don't care

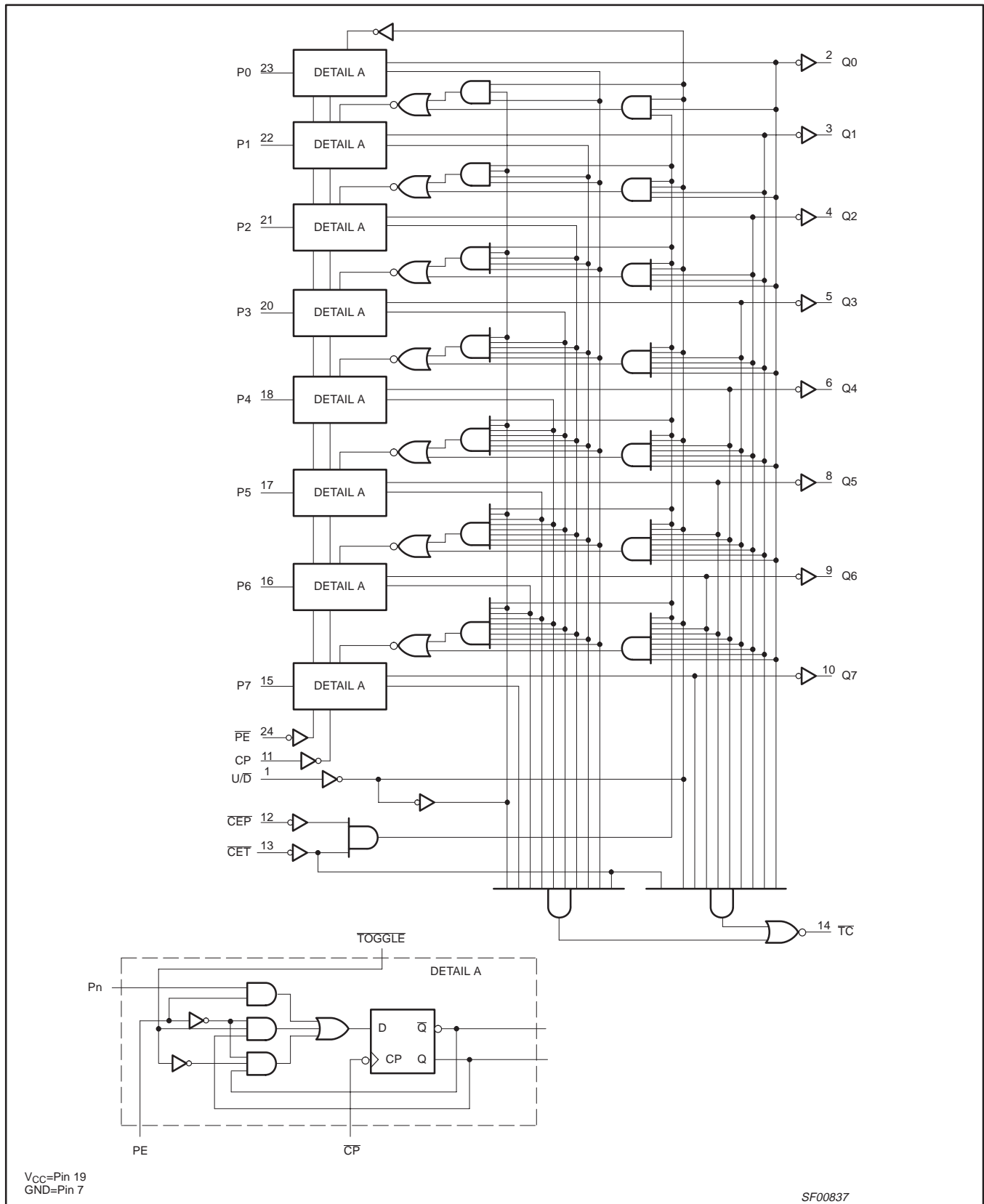
↑ = Low-to-High clock transition

(a) = TC is Low when CET is Low and the counter is at Terminal Count. Terminal Count Up is with all  $Q_n$  outputs High and Terminal Count Down is with all  $Q_n$  outputs Low.

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## LOGIC DIAGRAM



## 8-bit bidirectional binary counter

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**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limits set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	-0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	40	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature	-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current			-1	mA
I <sub>OL</sub>	Low-level output current			20	mA
T <sub>amb</sub>	Operating free-air temperature range	0		70	°C

**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>NO TAG</sup>	LIMITS			UNIT	
			MIN	TYP NO TAG	MAX		
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX	±10%V <sub>CC</sub>	2.5		V	
		V <sub>IH</sub> = MIN, I <sub>OH</sub> = MAX	±5%V <sub>CC</sub>	2.7	3.4		
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX	±10%V <sub>CC</sub>		0.30	V	
		V <sub>IH</sub> = MIN, I <sub>OL</sub> = MAX	±5%V <sub>CC</sub>		0.30		
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>			-0.73	V	
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V			100	μA	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V			20	μA	
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V			-0.6	mA	
I <sub>OS</sub>	Short-circuit output current <sup>NO TAG</sup>	V <sub>CC</sub> = MAX		-60		mA	
I <sub>CC</sub>	Supply current (total)	I <sub>CCH</sub>	V <sub>CC</sub> = MAX	PE=CET=CEP=U/D=GND, Pn=4.5V, CP=↑	93	120	mA
		I <sub>CCL</sub>			98	125	mA

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

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## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_{amb} = +25^{\circ}C$ $V_{CC} = +5V$ $C_L = 50pF, R_L = 500\Omega$			$T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$ $V_{CC} = +5V \pm 10\%$ $C_L = 50pF, R_L = 500\Omega$		
			MIN	TYP	MAX	MIN	MAX	
$f_{MAX}$	Maximum clock frequency	Waveform 1	100	115		85		MHz
$t_{PLH}$ $t_{pPHL}$	Propagation delay CP to $Q_n$ (Load, $\overline{PE} = \text{Low}$ )	Waveform 1	3.0 4.0	6.0 6.5	8.5 8.5	3.0 4.0	9.0 9.0	ns ns
$t_{PLH}$ $t_{PHL}$	Propagation delay CP to $Q_n$ (Count, $\overline{PE} = \text{High}$ )	Waveform 1	3.0 4.5	6.0 7.0	9.0 10.0	3.0 4.0	10.0 10.5	ns ns
$t_{PLH}$ $t_{PHL}$	Propagation delay CP to $\overline{TC}$	Waveform 1	4.5 5.0	6.5 6.5	9.5 9.5	4.0 5.0	10.5 10.0	ns ns
$t_{PLH}$ $t_{PHL}$	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2	3.5 3.0	6.0 6.5	9.0 9.0	3.0 3.0	10.0 10.0	ns ns
$t_{PLH}$ $t_{PHL}$	Propagation delay U/D to $\overline{TC}$	Waveform 3	4.5 4.5	7.0 7.0	9.0 9.5	4.0 4.0	10.0 10.0	ns ns

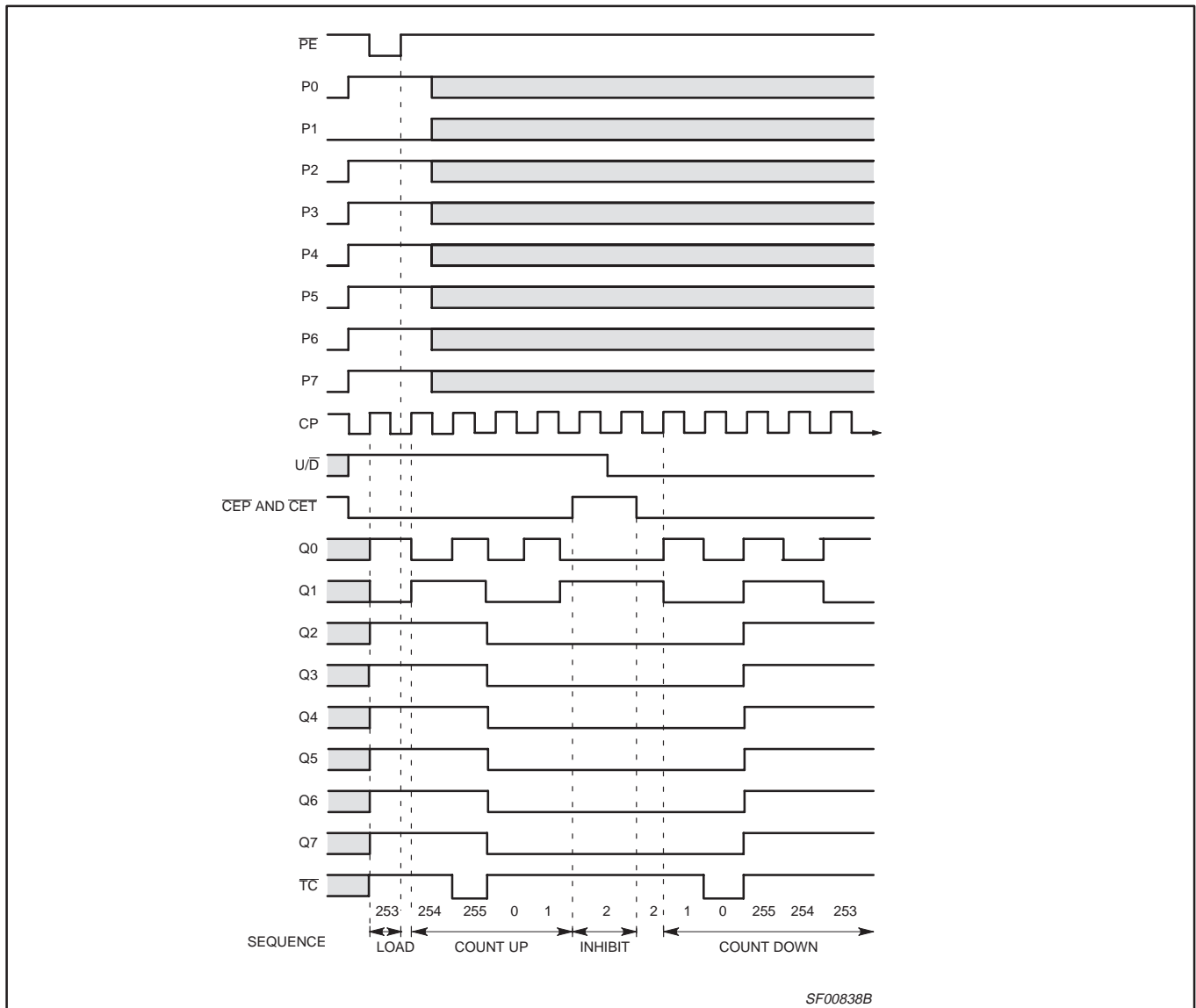
## AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS				UNIT
			$T_{amb} = +25^{\circ}C$ $V_{CC} = +5V$ $C_L = 50pF, R_L = 500\Omega$		$T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$ $V_{CC} = +5V \pm 10\%$ $C_L = 50pF, R_L = 500\Omega$		
			MIN	TYP	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $P_n$ to CP	Waveform 4	3.5 3.5		2.5 2.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $P_n$ to CP	Waveform 4	1.0 1.0		0 1.0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 4	5.5 6.5		5.5 6.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP	Waveform 4	0 0		0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	6.0 8.0		5.0 6.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	0 0		0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low U/D to CP	Waveform 6	8.0 6.5		6.5 6.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low U/D to CP	Waveform 6	0 0		0 0		ns ns
$t_w(H)$ $t_w(L)$	$\overline{CP}$ Pulse width High or Low	Waveform 1	4.0 4.5		4.0 5.0		ns ns

# 8-bit bidirectional binary counter

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## TIMING DIAGRAM



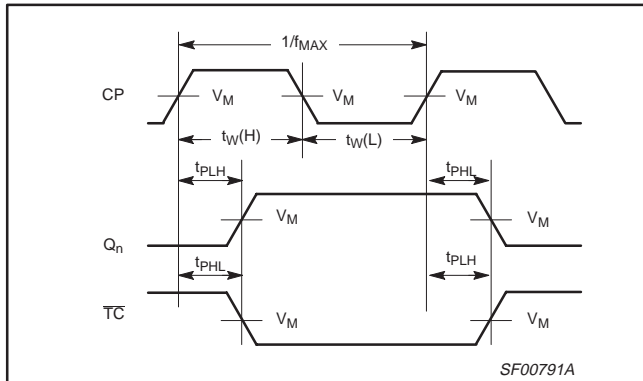
# 8-bit bidirectional binary counter

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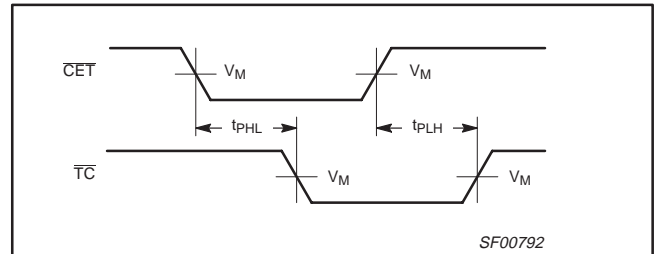
## AC WAVEFORMS

For all waveforms,  $V_M = 1.5V$ .

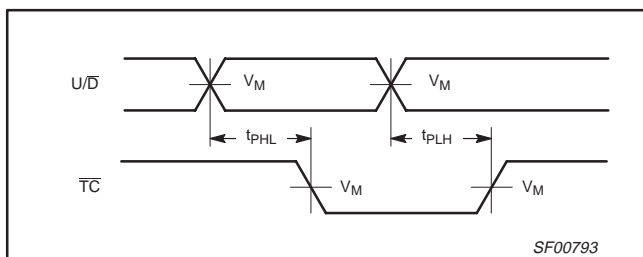
The shaded areas indicate when the input is permitted to change for predictable output performance.



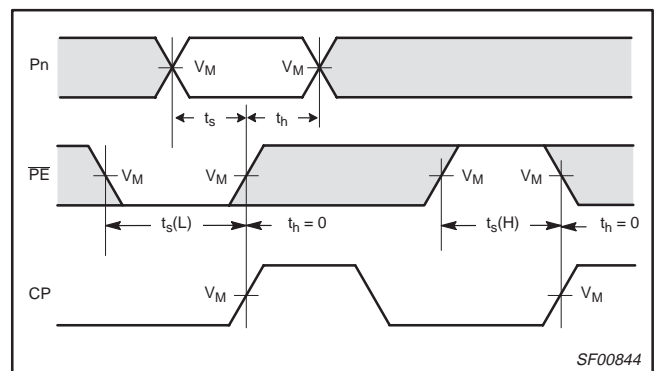
**Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency**



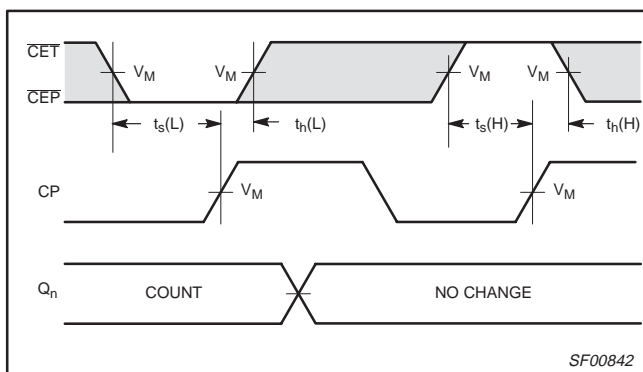
**Waveform 2. Propagation Delay, CET Input to Terminal Count Output**



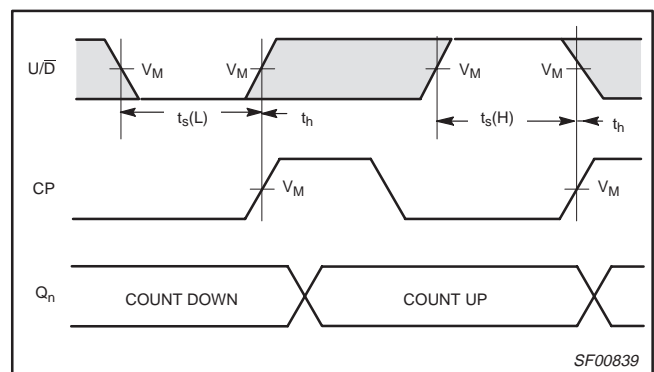
**Waveform 3. Propagation Delay, Up/Down Count Control Input to Terminal Count Output**



**Waveform 4. Parallel Data and Parallel Enable Setup and Hold Times**



**Waveform 5. Count Enables Setup and Hold Times**



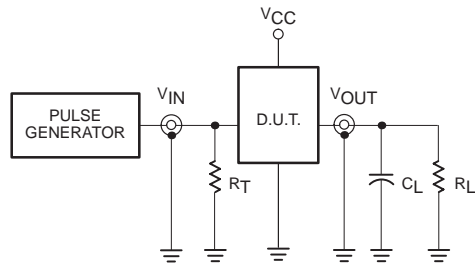
**Waveform 6. Up/Down Count Control Setup and Hold Times**



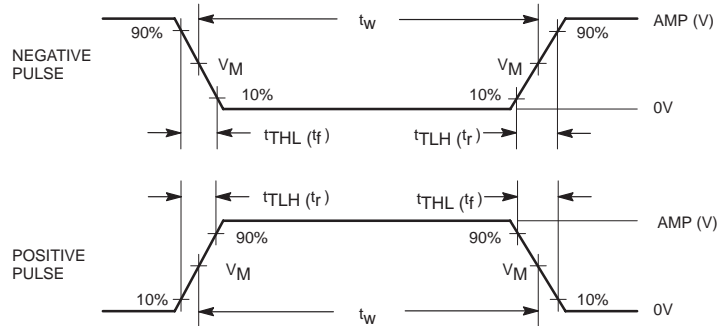
# 8-bit bidirectional binary counter

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## TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

**DEFINITIONS:**

- $R_L$  = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

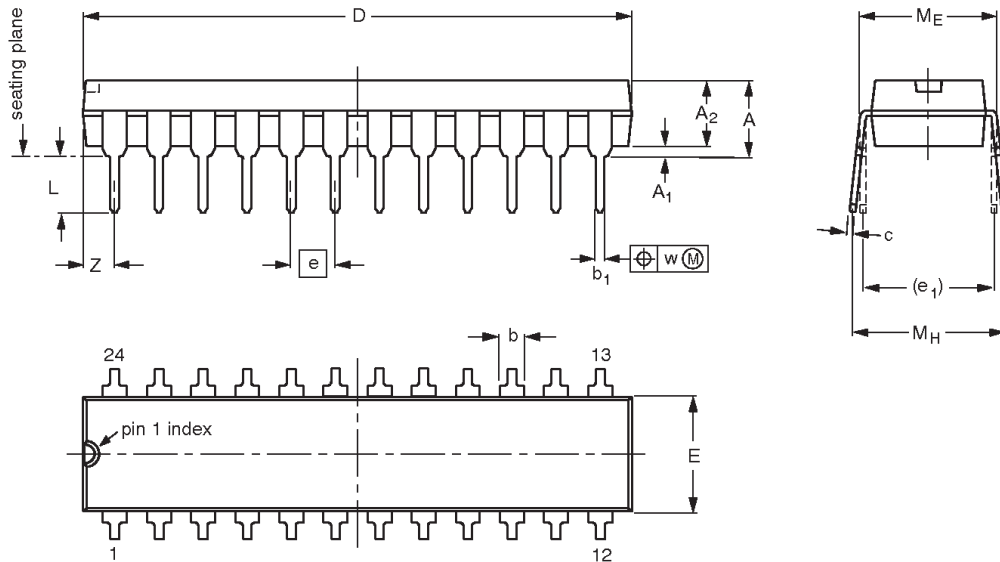
SF00006

# 8-bit bidirectional binary counter

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DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1



**DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

**Note**

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

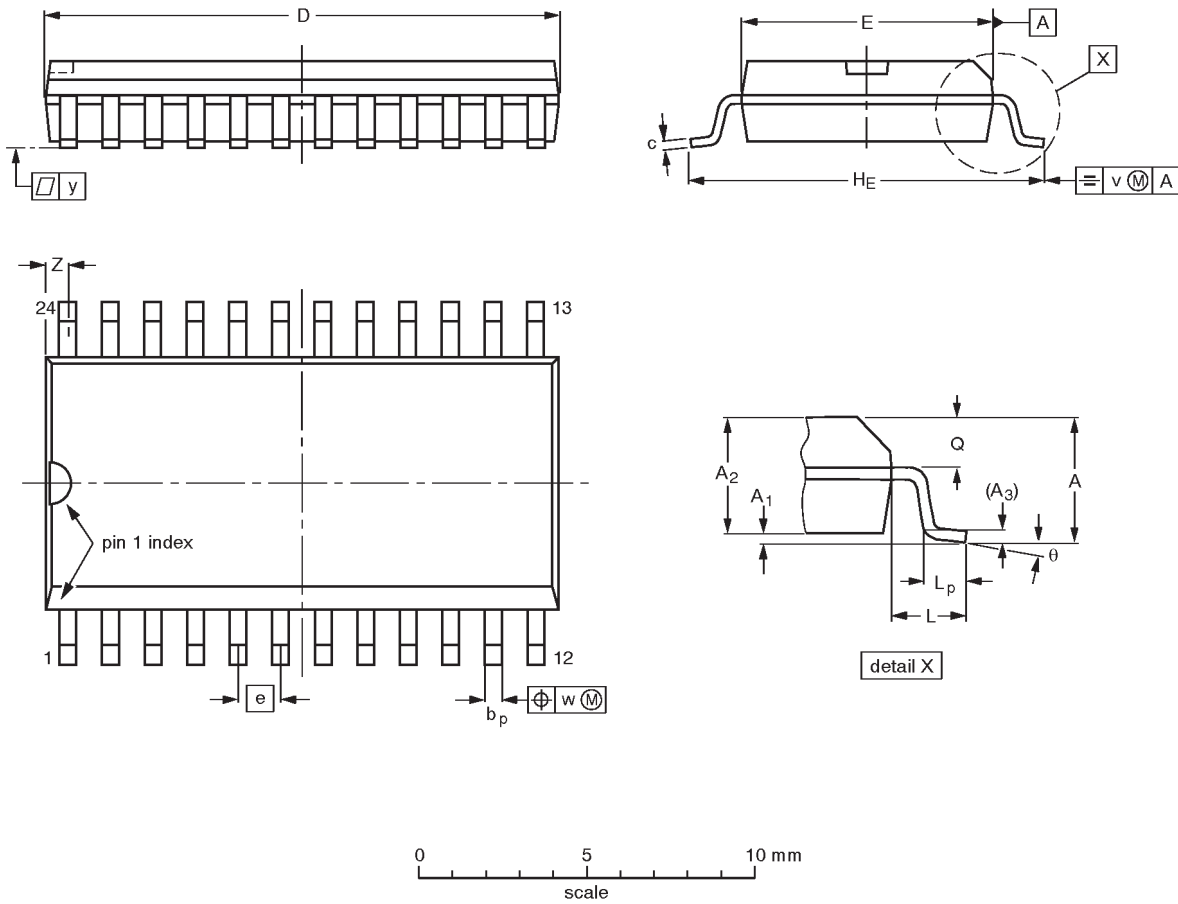
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

# 8-bit bidirectional binary counter

# 74F269

**SO24: plastic small outline package; 24 leads; body width 7.5 mm**

**SOT137-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	HE	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

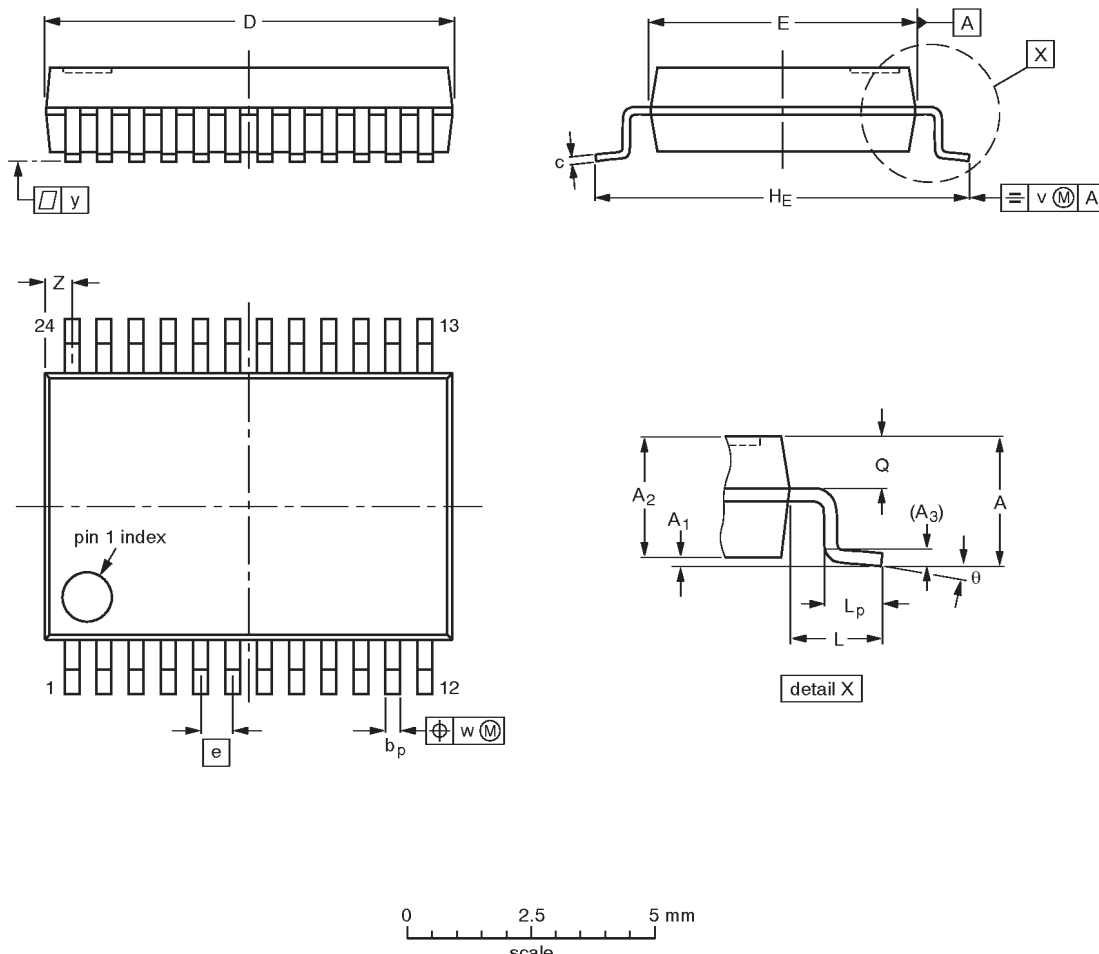
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				-92-11-17 95-01-24

8-bit bidirectional binary counter

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SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				93-09-08 95-02-04

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**NOTES**

## 8-bit bidirectional binary counter

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## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	<b>Preproduction Product</b>	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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