DATA SHEET

74F244/74F244B
Octal buffers (3-State)

Product specification

IC15 Data Handbook

1994 Dec 05

Philips Semiconductors

PHILIPS

Octal buffers (3-State) 74F244/74F244B

FEATURES

- Octal bus interface
- 3-State output buffer sink 64mA
- 15mA source current
- Guaranteed output skew less than 2.0ns (74F244B)
- Reduced ground bounce (74F244B)
- Reduced I_{CC} (74F244B)
- Reduced loading (74F244B I_{IL} = 40µA)
- Split lead frame offers increased noise immunity (74F244B)
- Industrial temperature range available (-40°C to +85°C) for 74F244
- 74F244 available in SSOP Type II package

DESCRIPTION

The 74F244 is an octal buffer that is ideal for driving bus lines of buffer memory address registers. The outputs are all capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two output enables, $\overline{OE}$a and $\overline{OE}$b, each controlling four of the 3-State outputs.

The 74F244B is functionally equivalent to the 74F244. It has been designed to reduce effects of ground noise. Other advantages are noted in the features.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F244	4.0ns	53mA
74F244B	4.0ns	33mA

ORDERING INFORMATION

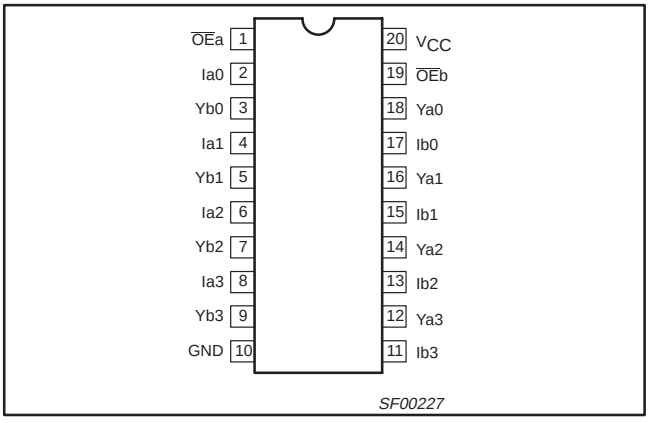
DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = -40°C to +85°C	
20-pin plastic DIP	N74F244N, N74F244BN	I74F244N	SOT146-1
20-pin plastic SOL	N74F244D, N74F244BD	I74F244D	SOT163-1
20-pin plastic SSOP II	N74F244DB		SOT339-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

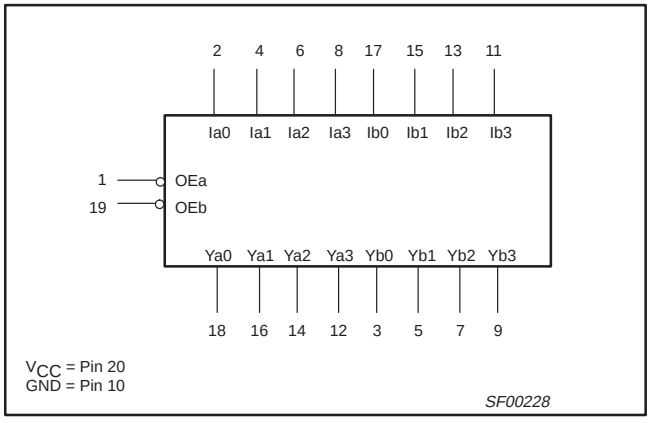
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ian, Ibn	Data inputs (74F244)	1.0/2.67	20µA/1.6mA
	Data inputs (74F244B)	1.0/0.067	20µA/40µA
$\overline{OE}$a, $\overline{OE}$b	Output enable inputs (active low) (74F244)	1.0/1.67	20µA/1.0mA
	Output enable inputs (active low) (74F244B)	1.0/0.067	20µA/40µA
Yan, Ybn	Data outputs	750/106.7	15mA/64mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

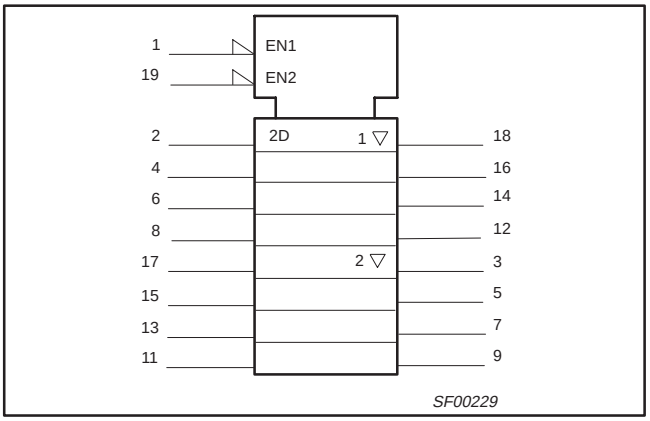
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL

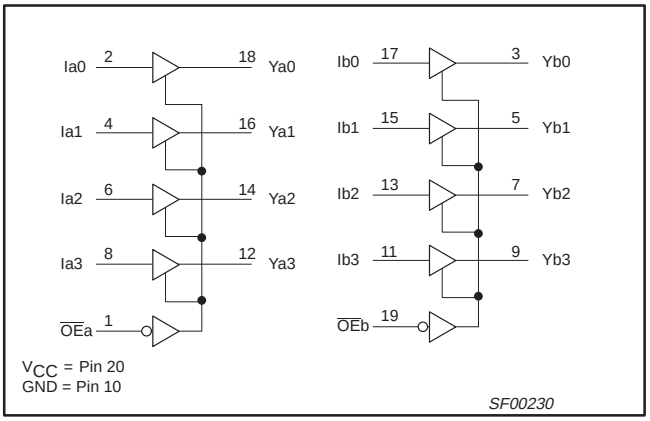


FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}a$	Ia	$\overline{OE}b$	Ib	Ya	Yb
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	Z	Z

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		128	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range (74F244 only)	-40 to +85	°C
T_{stg}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IN}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–15	mA
i_{ol}	Low-level output current				64	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range (74F244 only)	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -3mA	±10%V_{CC}	2.5			V
						±5%V_{CC}	2.7	3.4		V
					I_{OH} = -15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = MAX	±10%V_{CC}			0.55	V
				V_{IH} = MIN,		±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	74F244 $\overline{OE}$a, $\overline{OE}$b		V_{CC} = MAX, V_I = 0.5V					-1.0	mA
		74F244 Ian, Ibn							-1.6	mA
		74F244B all inputs							-40	µA
I_{OZH}	Off-state output current, high-level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	74F244	I_{CCH}	V_{CC} = MAX				40	60	mA
			I_{CCL}					60	90	mA
			I_{CCZ}					60	90	mA
		74F244B	I_{CCH}	V_{CC} = MAX				20	30	mA
			I_{CCL}					50	70	mA
			I_{CCZ}					29	40	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS FOR 74F244

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = -40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to Yn	Waveform 1	2.5 2.5	4.0 4.0	5.2 5.2	2.0 2.0	6.2 6.5	1.5 2.0	7.0 7.0	ns
t_{PZH} t_{PZL}	Output enable time to high or low	Waveform 2 Waveform 4	2.0 2.0	4.3 5.0	5.7 7.0	2.0 2.0	6.7 8.0	2.0 2.0	8.0 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low	Waveform 2 Waveform 4	1.5 1.5	2.5 2.5	5.5 5.5	1.0 1.0	6.0 5.5	1.0 1.0	6.0 5.5	ns

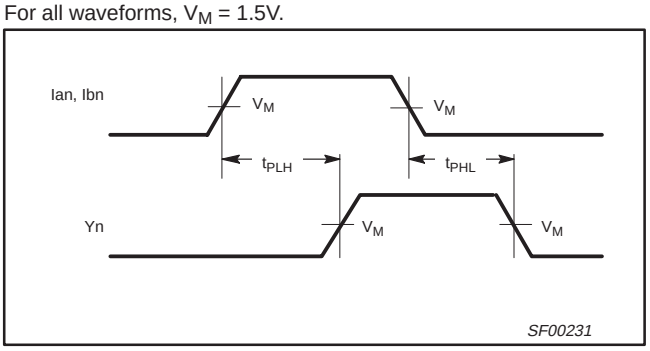
AC ELECTRICAL CHARACTERISTICS FOR 74F244B

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Ian, Ibn to Yn	Waveform 1	2.5 2.5	4.5 4.5	5.7 6.0	2.0 2.5	6.2 6.5	ns
t_{PZH} t_{PZL}	Output enable time to high or low level	Waveform 2 Waveform 4	2.0 3.0	4.0 5.5	6.0 7.5	2.0 3.0	6.5 8.0	ns
t_{PHZ} t_{PLZ}	Output disable time from high or low level	Waveform 2 Waveform 4	1.5 1.5	2.5 2.5	5.5 5.5	1.0 1.0	6.0 5.5	ns
$t_{sk(0)}$	Output skew[1, 2]	Waveform 3			1.5		2.0	ns

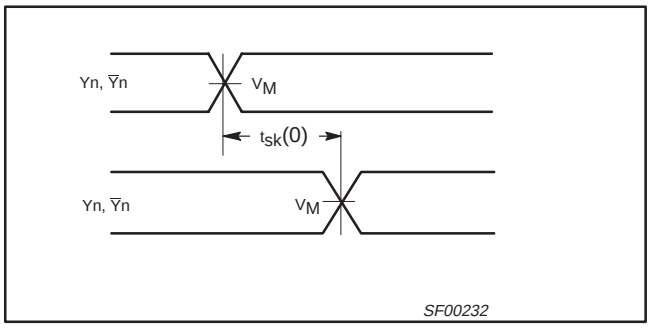
NOTES:
1. $|t_{PN}$ actual - t_{PM} actual| for any output compared to any other output where N and M are either LH or HL.
2. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

AC WAVEFORMS

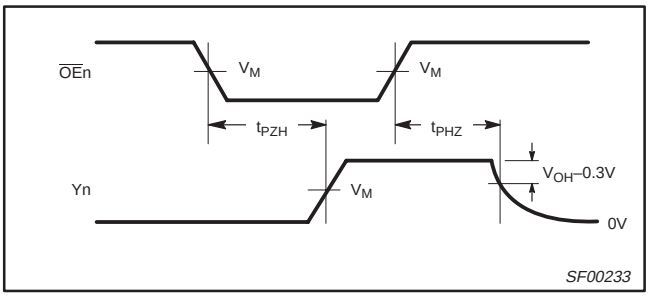
For all waveforms, V_M = 1.5V.



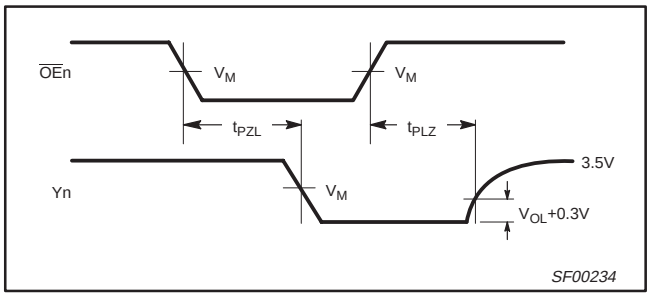
Waveform 1. Propagation Delay for data to outputs



Waveform 3. Output skew



Waveform 2. 3-State output enable time to high level and output disable time from high level

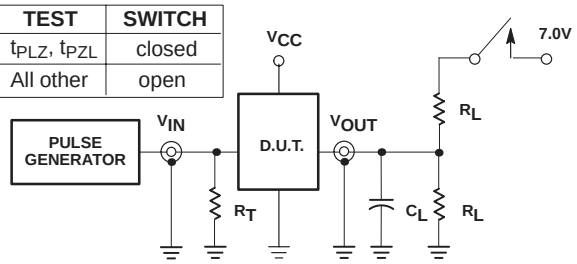


Waveform 4. 3-State output enable time to low level and output disable time from low level

TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



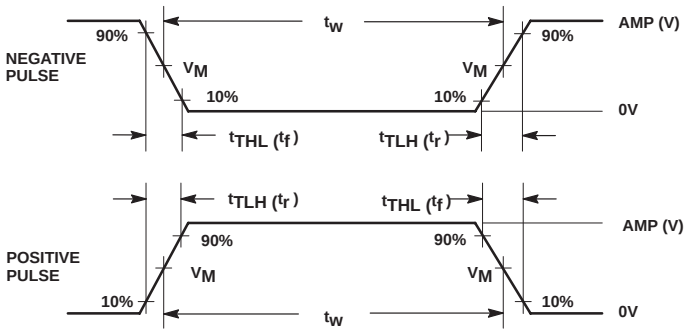
Test circuit for 3-State outputs

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

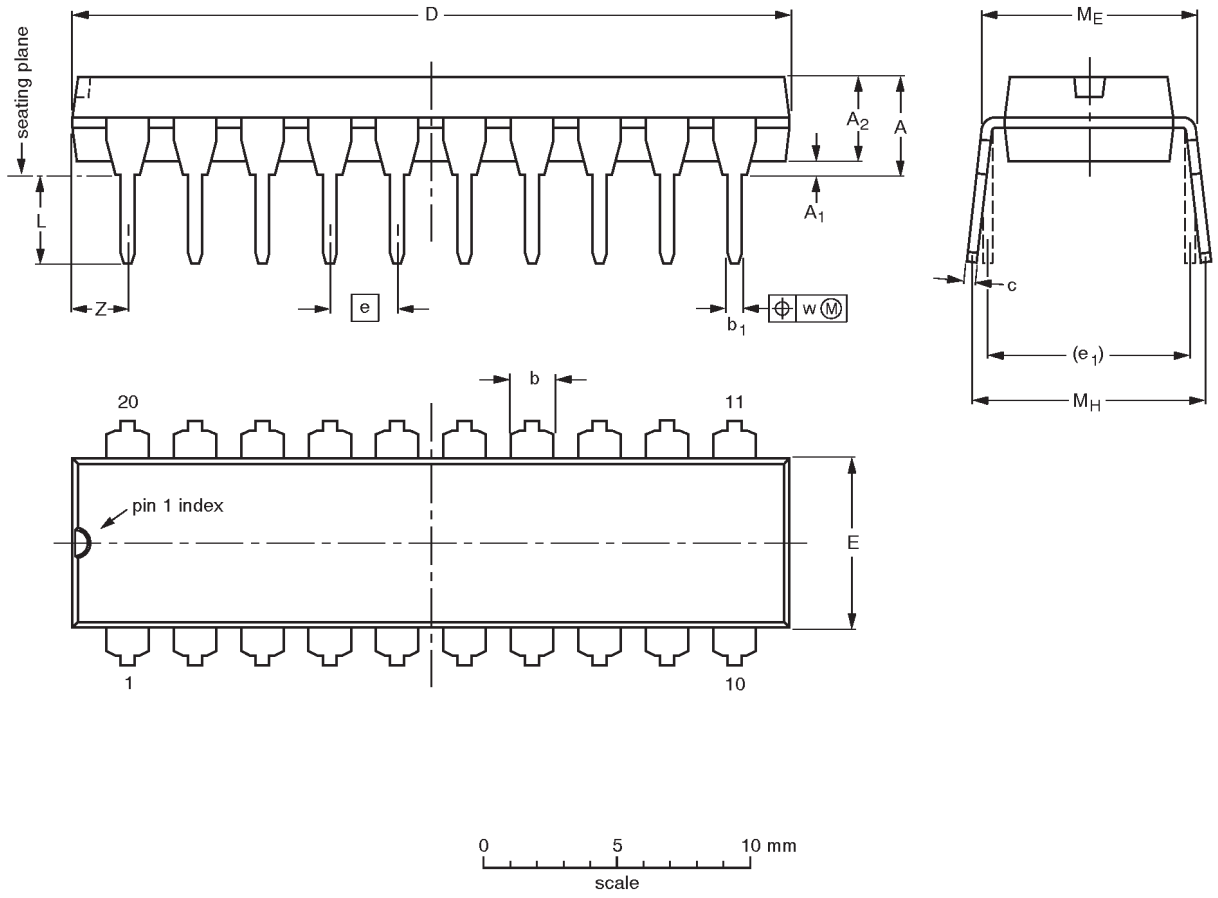


Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF000235

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

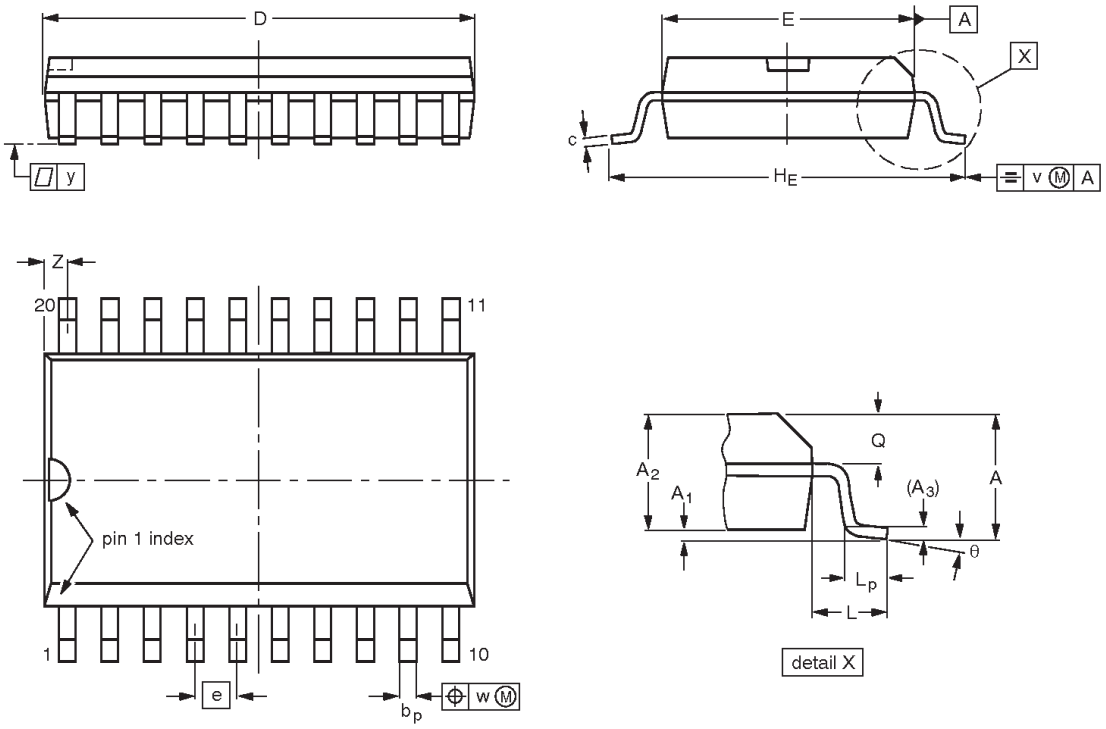
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

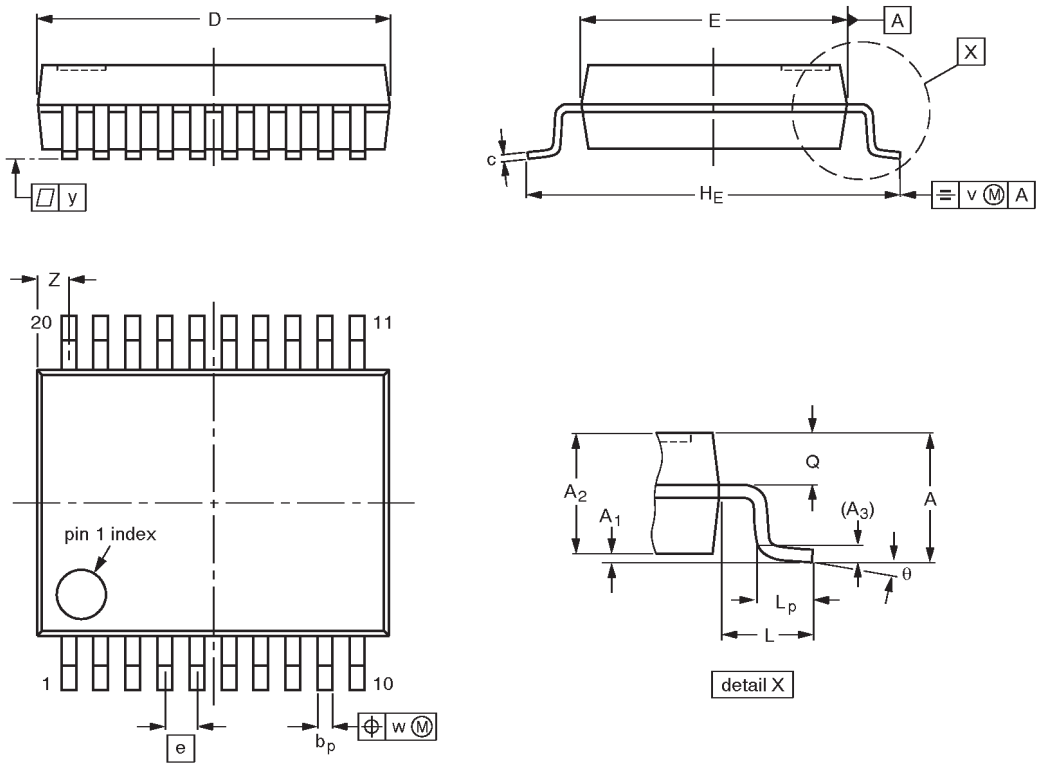
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				~~93-09-08~~ 95-02-04

NOTES

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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