DATA SHEET

74F191

Up/down binary counter with reset and ripple clock

Product specification

1995 Jul 17

IC15 Data Handbook

Philips
Semiconductors

PHILIPS

Up/Down binary counter with reset and ripple clock 74F191

FEATURES

- High speed –125MHz typical f_{MAX}
- Synchronous, reversible counting
- 4-Bit binary
- Asynchronous parallel load capability
- Cascadable without external logic
- Single up/down control input

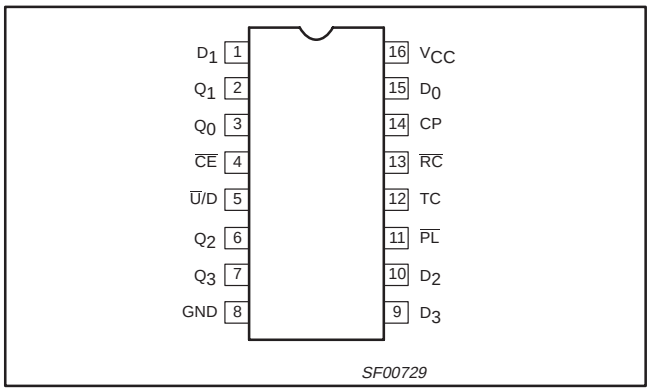
DESCRIPTION

The 74F191 is a 4-bit binary counter. It contains four edge-triggered master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operations.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel data inputs (D_0 - D_3) is loaded into the counter and appears on the outputs when the Parallel Load ($\overline{PL}$) input is Low. This operation overrides the counting function. Counting is inhibited by a High level on the count enable ($\overline{CE}$) input. When $\overline{CE}$ is Low, internal state changes are initiated. Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock ($\overline{RC}$).

The TC output is normally Low and goes High when: 1) the count reaches zero in the countdown mode or 2) reaches “15” in the count up mode. The TC output will remain High until a state change occurs, either by counting or presetting, or until $\overline{U}$/D is changed. TC output should not be used as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the $\overline{RC}$ output. When TC is High and $\overline{CE}$ is Low, the $\overline{RC}$ follows the clock pulse. The $\overline{RC}$ output essentially duplicates the Low clock pulse width, although delayed in time by two gate delays.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F191	125MHz	40mA

ORDERING INFORMATION

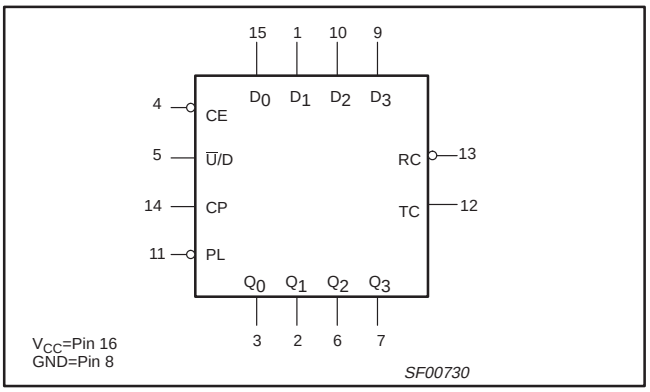
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-pin plastic DIP	N74F191N	SOT38-4
16-pin plastic SO	N74F191D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

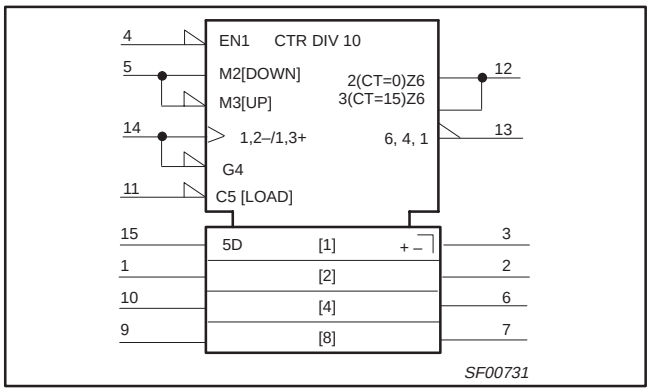
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{CE}$	Count enable input (active Low)	1.0/3.0	20µA/1.8mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{PL}$	Asynchronous parallel load control input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{U}$/D	Up/down count control input	1.0/1.0	20µA/0.6mA
Q_0 - Q_3	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{RC}$	Ripple clock output (active low)	50/33	1.0mA/20mA
TC	Terminal count output	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

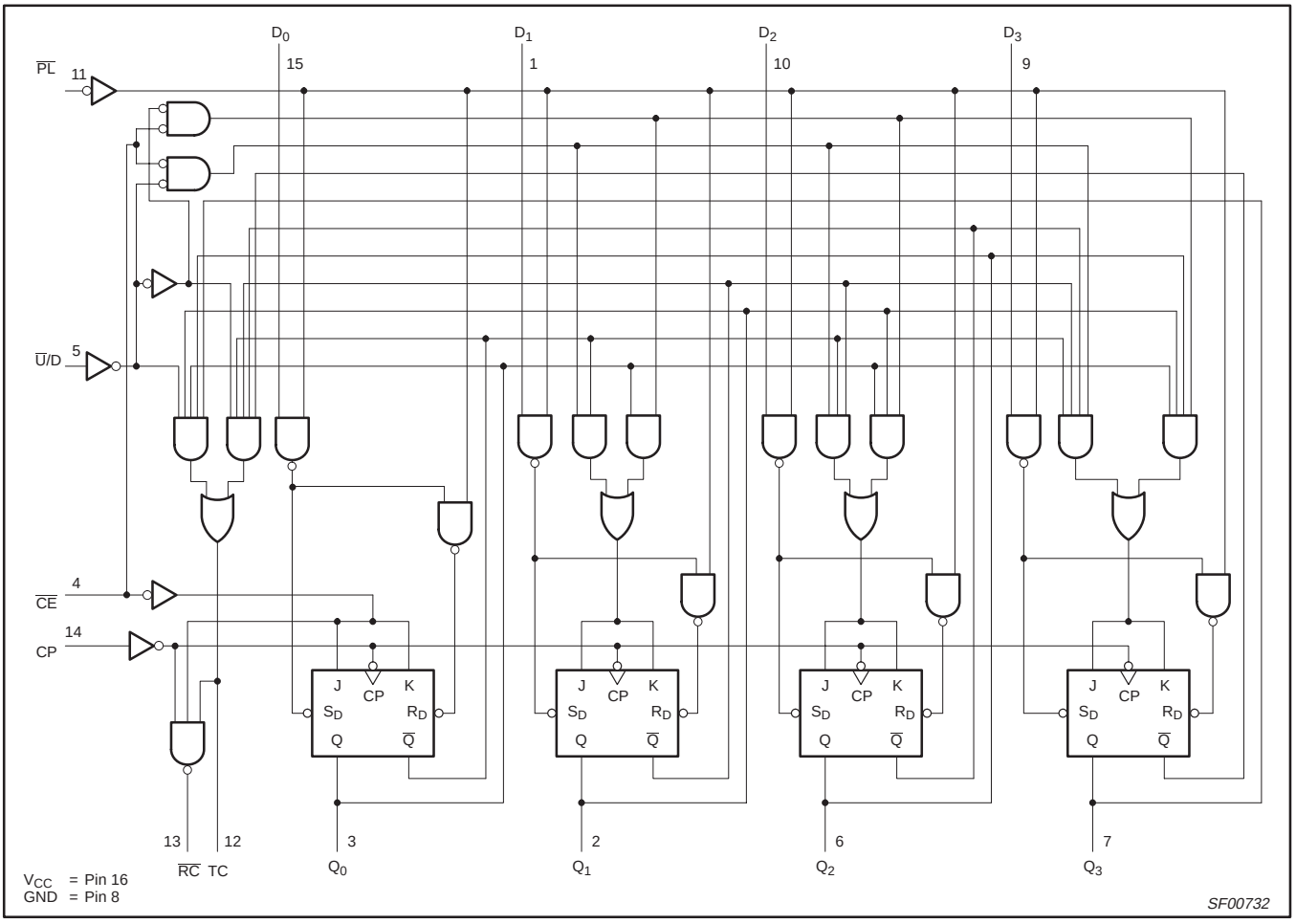
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

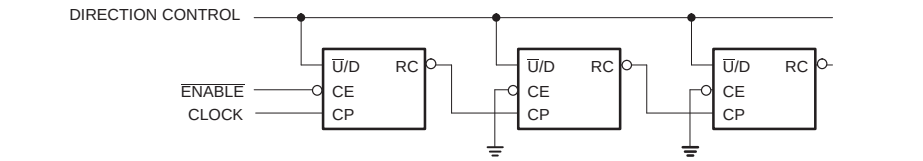
INPUTS					OUTPUTS	OPERATING MODE
$\overline{PL}$	$\overline{U}$/D	$\overline{CE}$	CP	D_n	Q_n	
L L	X X	X X	X X	L H	L H	Parallel load
H	L	I	↑	X	Count up	Count up
H	H	I	↑	X	Count down	Count down
H	X	H	X	X	No change	Hold (do nothing)

TC AND $\overline{RC}$ FUNCTION TABLE

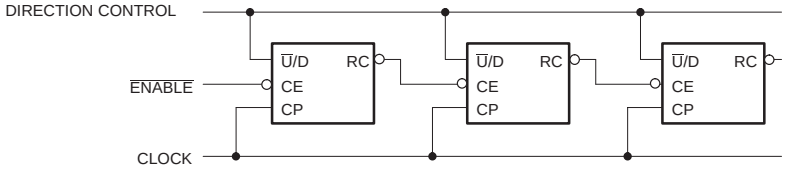
INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}$/D	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⊔	H	H	H	H	H	⊔
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊔	L	L	L	L	H	⊔

H = High voltage level steady state
L = Low voltage level steady state
X = Don't care
⊔ = Low pulse
↑ = Low-to-High clock transition
I = Low voltage level one set-up time prior to the Low-to-High clock transition

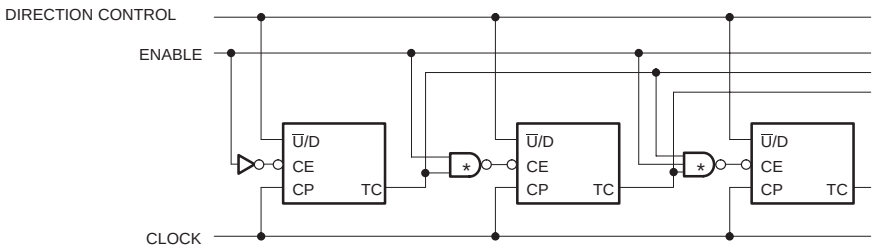
APPLICATIONS



a. N-Stage Counter Using Ripple Clock



b. Synchronous N-Stage Counter with Common Clock Using Ripple/Clock



* = Carry Gate

c. Synchronous N-Stage Counter with Common Clock and Terminal Count

SF00733

Figure 1.

The 74F191 simplifies the design of multi-stage counters, as indicated in Figure 1, each $\overline{RC}$ output is used as the clock input for the next higher stage. When the clock source has a limited drive capability this configuration is particularly advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a High signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure 1b shows a method of causing state changes to occur simultaneously in all stages. The $\overline{RC}$ output signals propagate in ripple fashion and all clock inputs are driven in parallel. The Low state duration of the clock in this configuration must be long enough to allow the negative-going edge of the $\overline{RC}$ signal to ripple through to the last stage before the clock goes High. Since the $\overline{RC}$ output of any package goes High shortly after its clock input goes High, there is no such restriction on the High state duration of the clock.

In Figure 1c, the configuration shown avoids ripple delays and their associated restrictions. The combined TC signals from all the preceding stages forms the $\overline{CE}$ input signal for a given stage. An enable signal must also be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own $\overline{CE}$, therefore, the simple inhibit scheme of Figure 1a and 1b does not apply.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min	±10%V_{CC}		0.30	0.50	V
				±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	$\overline{CE}$	V_{CC} = Max, V_I = 0.5V				–1.8	mA
		Others					–0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max		–60		–150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = Max			40	55	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} all inputs grounded and all outputs open.

AC ELECTRICAL CHARACTERISTICS

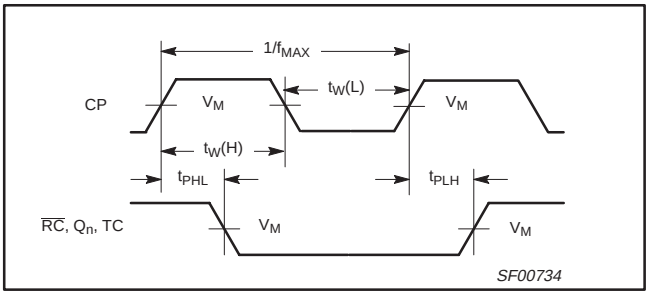
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb}= +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb}= 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency to Qn outputs	Waveform 1	100	125		90		MHz
f_{MAX}	Maximum clock frequency to $\overline{RC}$ outputs	Waveform 1	85	95		75		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	2.5 5.0	4.5 7.5	8.0 11.5	2.0 5.0	8.5 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	Waveform 1	6.5 6.0	9.0 8.0	12.5 11.0	6.0 6.0	13.0 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$	Waveform 2	2.5 3.0	4.5 5.0	7.5 7.5	2.0 2.5	8.0 8.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$	Waveform 2	2.0 3.0	4.0 5.0	7.0 7.5	2.0 3.0	7.5 8.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$	Waveform 2	8.0 4.5	11.0 7.5	16.0 10.5	8.0 4.0	17.0 11.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC	Waveform 4	4.0 3.0	6.5 6.0	9.5 9.5	3.0 3.0	10.5 10.0	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 3	2.0 6.5	4.0 9.0	7.0 12.0	1.5 6.5	7.5 13.0	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC	Waveform 3 Waveform 4	5.5 6.5	9.5 9.5	13.0 13.0	5.0 6.0	14.0 14.0	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$	Waveform 3 Waveform 4	6.0 6.0	14.0 11.0	18.0 13.5	6.0 6.0	19.5 15.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n	Waveform 5	4.5 5.5	6.5 8.0	9.5 11.5	4.0 5.0	10.5 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC	Waveform 5	5.5 6.0	8.5 10.5	12.0 13.5	5.5 6.0	13.0 14.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$	Waveform 5	8.5 7.5	16.0 10.0	18.5 13.0	8.5 7.0	21.0 13.5	ns ns

AC SETUP REQUIREMENTS

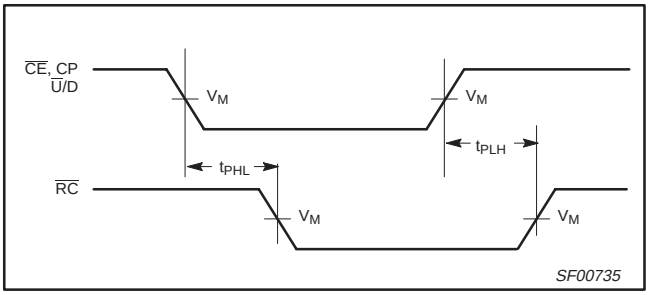
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb}= +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low D_n to $\overline{PL}$	Waveform 6	4.5 4.5			5.0 5.0		ns ns
t_h(H) t_h(L)	Hold time, High or Low D_n to $\overline{PL}$	Waveform 6	2.0 2.0			2.0 2.0		ns ns
t_s(L)	Setup time, Low $\overline{CE}$ to CP	Waveform 6	10.0			10.0		ns
t_h(L)	Hold time, Low $\overline{CE}$ to CP	Waveform 6	0			0		ns
t_s(H) t_s(L)	Setup time, High or Low $\overline{U}$/D to CP	Waveform 6	12.0 12.0			12.0 12.0		ns ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{U}$/D to CP	Waveform 6	0 0			0 0		ns ns
t_w(H) t_w(L)	CP Pulse width, High or Low	Waveform 1	3.5 6.0			3.5 6.0		ns ns
t_w(L)	$\overline{PL}$ Pulse width, Low	Waveform 5	6.0			6.0		ns
t_{rec}	Recovery time, $\overline{PL}$ to CP	Waveform 5	6.0			6.0		ns

AC WAVEFORMS

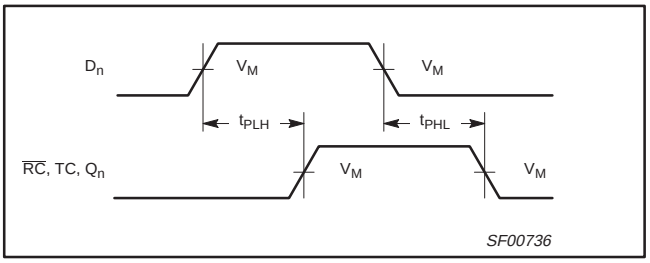
NOTE: For all waveforms, V_M = 1.5V



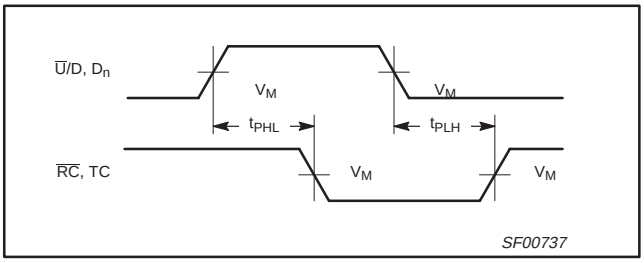
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency.



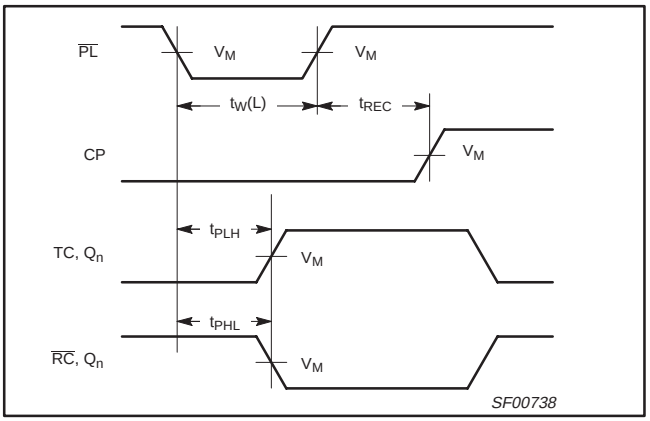
Waveform 2. Propagation Delay, Clock, Clock Enable or Up/Down to Ripple Clock Output



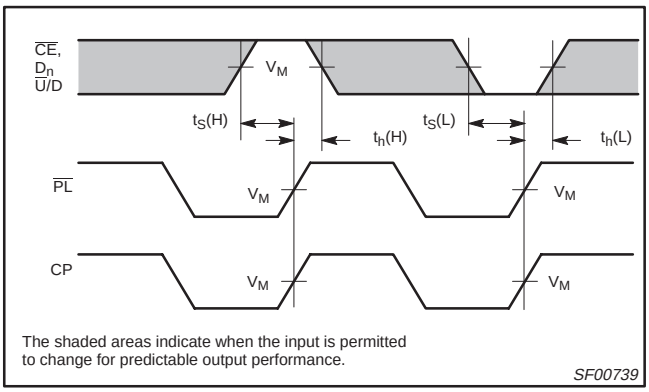
Waveform 3. Propagation Delay, Non-Inverting Path



Waveform 4. Propagation Delay, Inverting Path

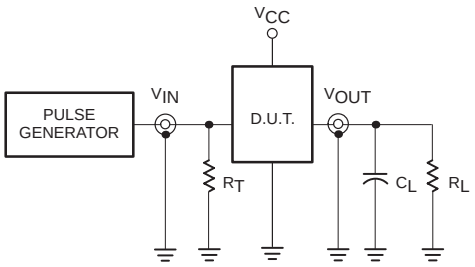


Waveform 5. Parallel Load Pulse Width, Parallel Load to Output Delay and Parallel Load to Clock Recovery Time

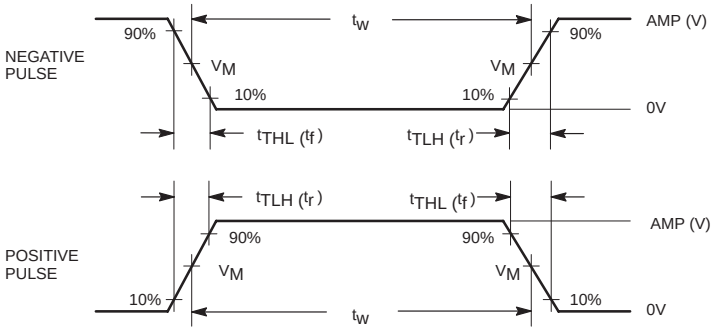


Waveform 6. Data Set Up and Hold Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

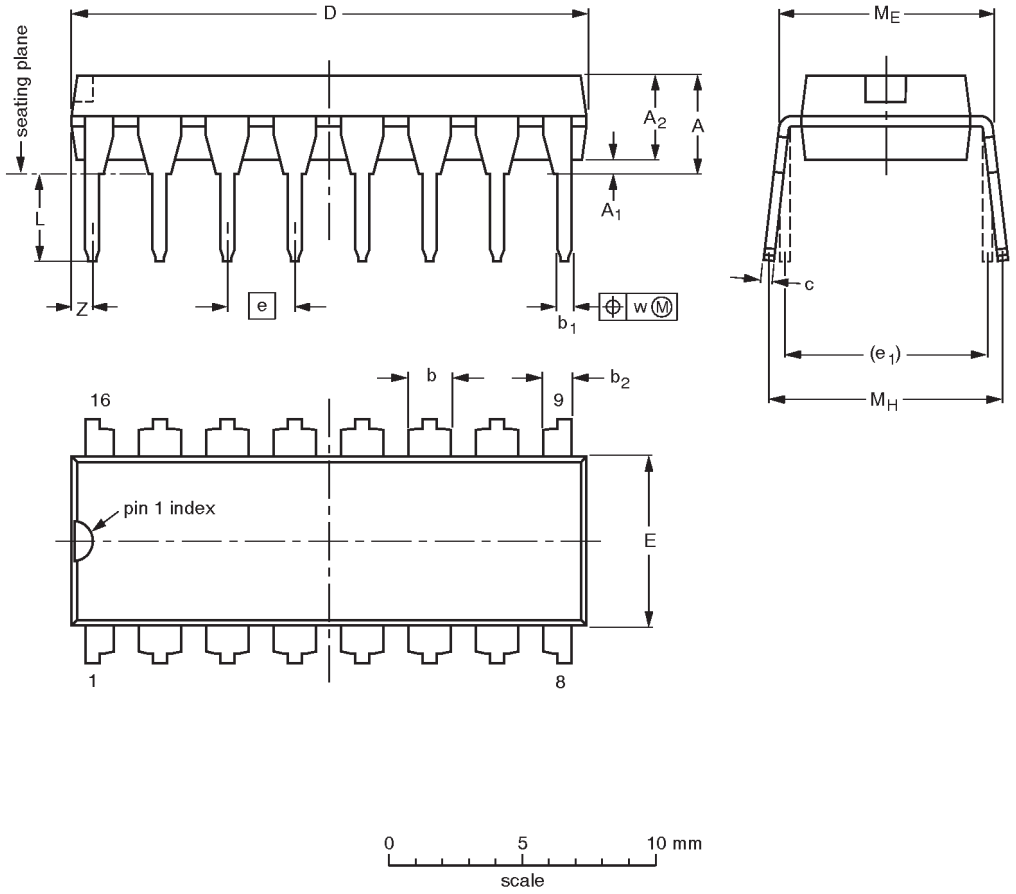
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

DIP16: plastic dual in-line package; 16 leads (300 mil) SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

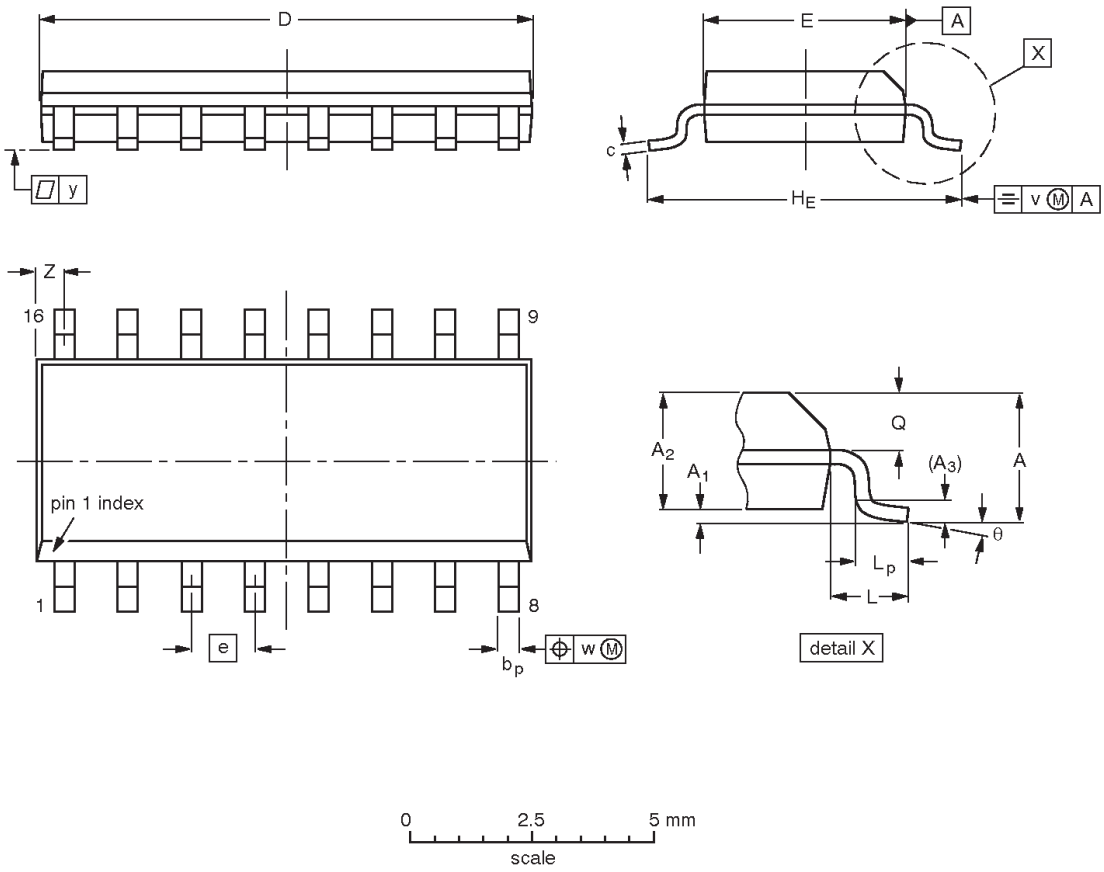
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

SO16: plastic small outline package; 16 leads; body width 3.9 mm SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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