

October 1989 Revised August 1999

74F164A

Serial-In, Parallel-Out Shift Register

General Description

The 74F164A is a high-speed 8-bit serial-in/parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the LOW-to-HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register, setting all outputs LOW independent of the clock. The 74F164A is a faster version of the 74F164.

Features

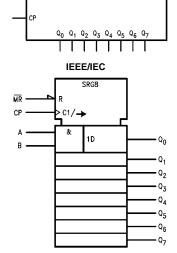
- Typical shift frequency of 90 MHz
- Asynchronous Master Reset
- Gated serial data input
- Fully synchronous data transfers
- 74F164A is a faster version of the 74F164

Ordering Code:

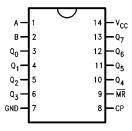
Order Number Package Number			Package Description						
74F164AS0	С	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow						
74F164AS	J	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide						
74F164AP0	С	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide						

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



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DS010613

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Unit Loading/Fan Out

Pin Names	Decemention	U.L.	Input I _{IH} /I _{IL}	
Pin Names	Description	HIGH/LOW	Output I _{OH} /I _{OL}	
A, B	Data Inputs	1.0/1.0	20 μA/-0.6 mA	
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/-0.6 mA	
MR	Master Reset Input (Active LOW)	1.0/1.0	20 μA/-0.6 mA	
Q ₀ –Q ₇	Outputs	50/33.3	-1 mA/20 mA	

Functional Description

The 74F164A is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q_0 the logical AND of the two data inputs (A • B) that existed before the rising clock edge. A LOW level on the Master Reset $(\overline{\mathsf{MR}})$ input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

Mode Select Table

Operating	I	nputs	3	Outputs		
Mode	MR	Α	В	Q_0	Q ₁ –Q ₇	
Reset (Clear)	L	Χ	Χ	L	L-L	
	Н	ı		L	q ₀ -q ₆	
Shift	Н	- 1	h	L	q ₀ -q ₆	
	Н	h	- 1	L	q ₀ -q ₆	
	Н	h	h	Н	q ₀ -q ₆	

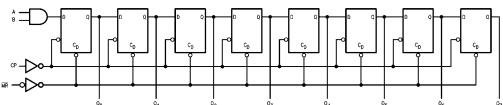
H(h) = HIGH Voltage Levels

L(I) = LOW Voltage Levels

X = Immaterial

 $q_n = \mbox{Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.} \label{eq:qn}$

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

_{150°C} Conditions

 $\begin{array}{ll} \mbox{Storage Temperature} & -65^{\circ}\mbox{C to } +150^{\circ}\mbox{C} \\ \mbox{Ambient Temperature under Bias} & -55^{\circ}\mbox{C to } +125^{\circ}\mbox{C} \\ \end{array}$

Junction Temperature under Bias -55°C to +150°C V_{CC} Pin Potential to Ground Pin -0.5V to +7.0V

Voltage Applied to Output in HIGH State (with V_{CC} = 0V)

 $\begin{array}{lll} \mbox{Standard Output} & -0.5\mbox{V to V}_{\mbox{CC}} \\ \mbox{3-STATE Output} & -0.5\mbox{V to } +5.5\mbox{V} \end{array}$

Current Applied to Output

Free Air Ambient Temperature $0^{\circ}\text{C} \text{ to } +70^{\circ}\text{C}$ Supply Voltage +4.5V to +5.5V

Recommended Operating

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

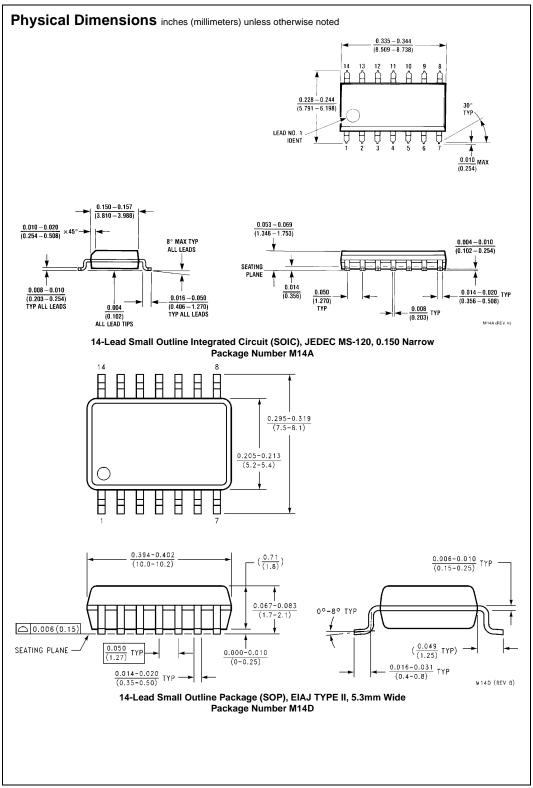
Symbol	Parameter		Min	Тур	Max	Units	v _{cc}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal	
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage				-1.2	V	Min	$I_{IN} = -18 \text{ mA}$
V _{OH}	Output HIGH	10% V _{CC}	2.5			V Min		I _{OH} = -1 mA
	Voltage	5% V _{CC}	2.7			v v	IVIIII	$I_{OH} = -1 \text{ mA}$
V _{OL}	Output LOW Voltage	10% V _{CC}			0.5	V	Min	I _{OL} = 20 mA
I _{IH}	Input HIGH Current				5.0	μА	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test				7.0	μΑ	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current				50	μΑ	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test		4.75			V	0.0	$I_{\text{ID}} = 1.9 \mu\text{A}$ All other pins grounded
I _{OD}	Output Leakage Circuit Current				3.75	μΑ	0.0	V _{IOD} = 150 mV All other pins grounded
I _{IL}	Input LOW Current				-0.6	mA	Max	$V_{IN} = 0.5V$
los	Output Short-Circuit Current		-60		-150	mA	Max	V _{OUT} = 0V
Icc	Power Supply Current			35	55	mA	Max	CP = HIGH MR = GND, A, B = GND

AC Electrical Characteristics

Symbol	Parameter	$T_{A} = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_{L} = 50 \text{ pF}$			$T_{A} = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V$ $C_{L} = 50 \text{ pF}$		$T_A = 0$ °C to +70°C $V_{CC} = 5.0V$ $C_L = 50$ pF		Units
		Min	Тур	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	80	120		60		80		MHz
t _{PLH}	Propagation Delay	3.0	4.8	7.5	2.5	9.0	3.0	7.5	20
t _{PHL}	CP to Q _n	3.5	5.0	8.0	3.0	8.5	3.5	8.0	ns
t _{PHL}	Propagation Delay MR to Q _n	5.0	7.0	10.0	4.0	12.5	5.0	10.5	ns

AC Operating Requirements

		$T_A = +25$ °C $V_{CC} = +5.0$ V		$T_A = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V$		$T_A = 0$ °C to +70°C $V_{CC} = 5.0V$		Units
Symbol	Parameter							
		Min	Max	Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	4.5		5.5		4.5		
t _S (L)	A or B to CP	4.0		4.0		4.0		ns
t _H (H)	Hold Time, HIGH or LOW	1.0		1.0		1.0		115
t _H (L)	A or B to CP	1.0		1.0		1.0		
t _W (H)	CP Pulse Width	4.0		4.0		4.0		no
t _W (L)	HIGH or LOW	7.0		7.0		7.0		ns
t _W (L)	MR Pulse Width, LOW	4.0		5.0		4.0		ns
t _{REC}	Recovery Time	5.0		6.5		5.0		ns
	MR to CP	0.0		0.0		3.0		5



Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770 (18.80 - 19.56)0.090 (2.286) 14 13 12 14 13 12 11 10 9 8 INDEX AREA 0.250 ± 0.010 (6.350 ± 0.254) PIN NO. 1 PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA $\frac{0.030}{(0.762)}$ MAX OPTION 1 OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ 0.300 - 0.320(7.620 - 8.128)0.060 0.145 - 0.2004° TYP Optional (1.651) (3.683 - 5.080) $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 0.020 (0.508) 0.125 - 0.150 0.075 ± 0.015 $\overline{(3.175 - 3.810)}$ (1.905 ± 0.381) (7.112) MIN 0.014 - 0.023 $\frac{0.100 \pm 0.010}{(2.540 \pm 0.254)} \text{ TYP}$ (0.356 - 0.584) $\frac{0.050 \pm 0.010}{(1.270 - 0.254)}$ TYP 0.325 ^{+0.040} -0.015 8.255 + 1.016 N144 (REV.F)

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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