

# DATA SHEET

**74F138**

1-of-8 decoder/demultiplexer

Product specification

1991 Feb 14

IC15 Data Handbook

# 1-of-8 decoder/demultiplexer

# 74F138

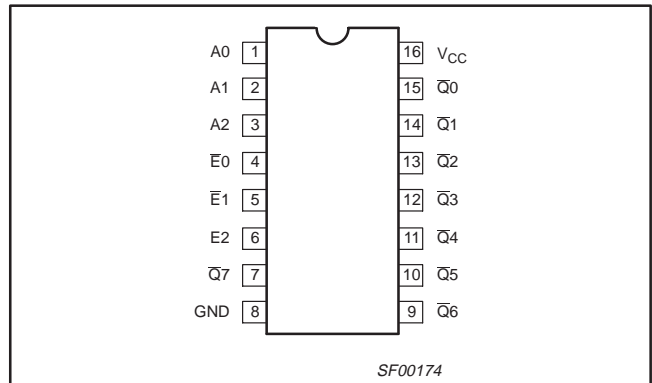
## FEATURE

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Industrial temperature range available (−40°C to +85°C)

## DESCRIPTION

The 74F138 decoder accepts three binary weighted inputs (A0, A1, A2) and when enabled, provides eight mutually exclusive, active low outputs (Q0 – Q7). The device features three enable inputs; two active low (E0, E1) and one active high (E2). Every output will be high unless E0 and E1 are low and E2 is high. This multiple enable function allows easy parallel expansion of the device to 1-of-32 (5 lines to 32 lines) decoder with just four 74F138s and one inverter (see Figure 1). The device can be used as an eight output demultiplexer by using one of the active low enable inputs as the data input and the remaining enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active high or active low state.

## PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F138	5.8ns	13mA

## ORDERING INFORMATION

DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V <sub>CC</sub> = 5V ±10%, T <sub>amb</sub> = 0°C to +70°C	INDUSTRIAL RANGE V <sub>CC</sub> = 5V ±10%, T <sub>amb</sub> = −40°C to +85°C	
16-pin plastic DIP	N74F138N	I74F138N	SOT38-4
16-pin plastic SO	N74F138D	I74F138D	SOT109-1

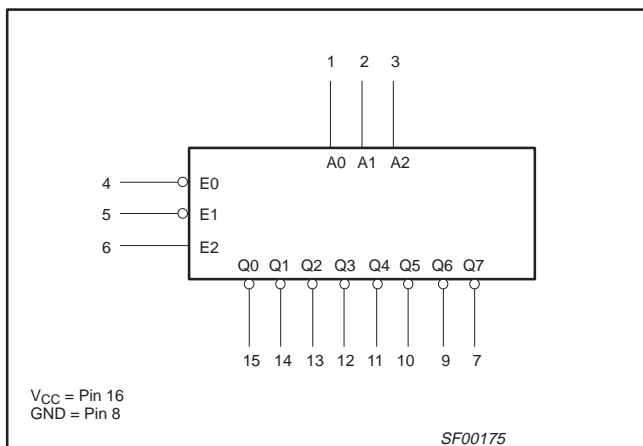
## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A2	Address inputs	1.0/1.0	20µA/0.6mA
E0, E1	Enable inputs (active Low)	1.0/1.0	20µA/0.6mA
E2	Enable input (active High)	1.0/1.0	20µA/0.6mA
Q0 – Q7	Data outputs	50/33	1.0mA/20mA

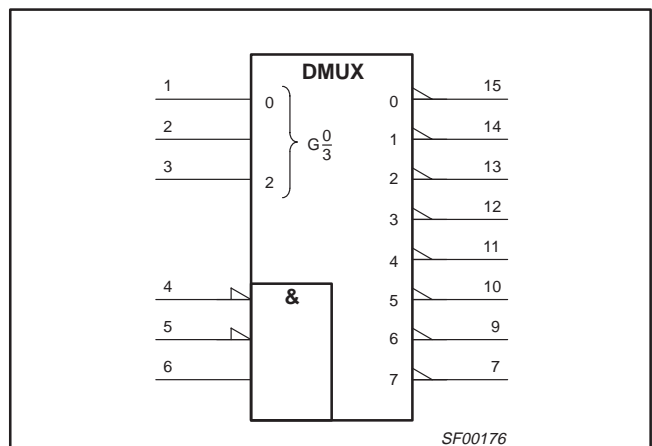
### NOTE:

One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

## LOGIC SYMBOL



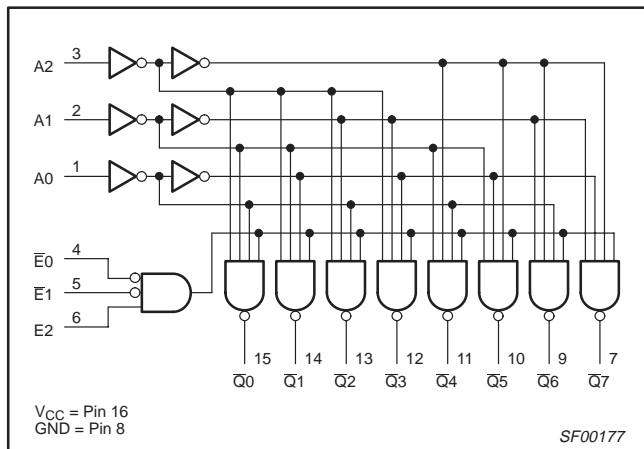
## IEC/IEEE SYMBOL



# 1-of-8 decoder/demultiplexer

# 74F138

## LOGIC DIAGRAM



## FUNCTION TABLE

INPUTS						OUTPUTS							
E0	E1	E2	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

### NOTES:

- H = High voltage level
- L = Low voltage level
- X = Don't care

## APPLICATION

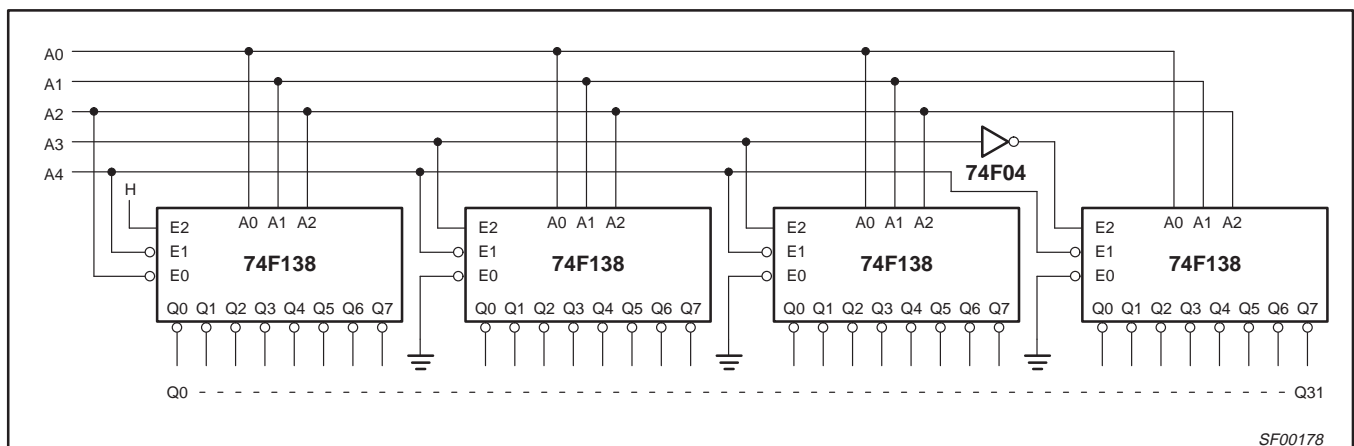


Figure 1. Expansion of 1-of-8 Decoding

## 1-of-8 decoder/demultiplexer

74F138

**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limit set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
$V_{CC}$	Supply voltage		-0.5 to +7.0	V
$V_{IN}$	Input voltage		-0.5 to +7.0	V
$I_{IN}$	Input current		-30 to +5	mA
$V_{OUT}$	Voltage applied to output in High output state		-0.5 to $V_{CC}$	V
$I_{OUT}$	Current applied to output in Low output state		40	mA
$T_{amb}$	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	-40 to +85	°C
$T_{stg}$	Storage temperature range		-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-1	mA
$I_{OL}$	Low-level output current			20	mA
$T_{amb}$	Operating free-air temperature range	Commercial range	0	+70	°C
		Industrial range	-40	+85	°C

**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>		LIMITS			UNIT
				MIN	TYP <sup>2</sup>	MAX	
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}$	$I_{OH} = \text{MAX}$	$\pm 10\%V_{CC}$	2.5		V
				$\pm 5\%V_{CC}$	2.7	3.4	V
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}$	$I_{OL} = \text{MAX}$	$\pm 10\%V_{CC}$		0.30	0.50
				$\pm 5\%V_{CC}$		0.30	0.50
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-0.73	-1.2	V
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$				100	$\mu\text{A}$
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$				20	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$				-0.6	mA
$I_{OS}$	Short-circuit output current <sup>3</sup>	$V_{CC} = \text{MAX}$		-60		-150	mA
$I_{CC}$	Supply current <sup>4</sup> (total)	$V_{CC} = \text{MAX}$			13	20	mA

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_{amb} = 25^\circ\text{C}$ .
- Not more than one output should be shorted at a time. For testing  $I_{OS}$ , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.
- Measure  $I_{CC}$ . outputs must be open,  $V_{IN}$  on all inputs = 4.5V.

# 1-of-8 decoder/demultiplexer

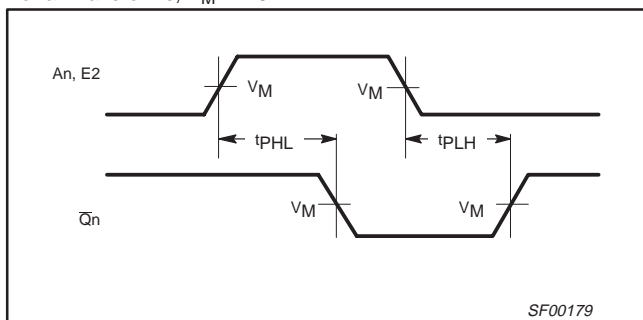
# 74F138

## AC ELECTRICAL CHARACTERISTICS

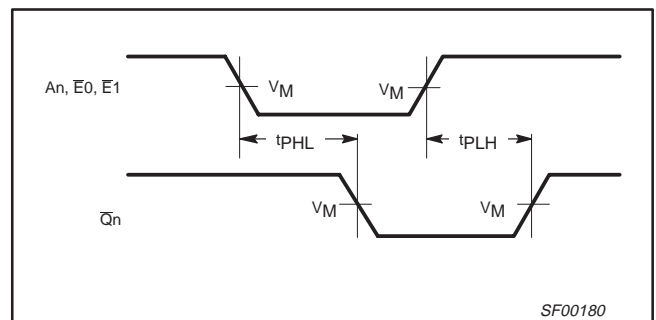
SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT	
			$V_{CC} = +5.0V$ $T_{amb} = +25^{\circ}C$ $C_L = 50pF$ $R_L = 500\Omega$			$V_{CC} = +5.0V \pm 10\%$ $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$ $C_L = 50pF$ $R_L = 500\Omega$		$V_{CC} = +5.0V \pm 10\%$ $T_{amb} = -40^{\circ}C \text{ to } +85^{\circ}C$ $C_L = 50pF$ $R_L = 500\Omega$		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
$t_{PLH}$ $t_{PHL}$	Propagation delay An to $\bar{Q}_n$	Waveform 1, 2	3.5 4.0	5.6 6.1	7.0 8.0	3.5 4.0	8.0 9.0	3.0 3.5	8.5 9.0	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay $\bar{E}0$ or $\bar{E}1$ to $\bar{Q}_n$	Waveform 2	3.5 3.0	6.4 5.3	7.0 7.0	3.5 3.0	8.0 7.5	3.0 3.0	8.0 7.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay E2 to $\bar{Q}_n$	Waveform 1	4.0 3.5	6.2 5.6	8.0 7.5	4.0 3.5	9.0 8.5	4.0 3.5	9.5 8.5	ns

## AC WAVEFORMS

For all waveforms,  $V_M = 1.5V$



Waveform 1. Propagation Delay for Inverting Outputs



Waveform 2. Propagation Delay for Non-Inverting Outputs

## TEST CIRCUIT AND WAVEFORMS

**Test Circuit for Totem-Pole Outputs**

**Input Pulse Definition**

**DEFINITIONS:**

- $R_L$  = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

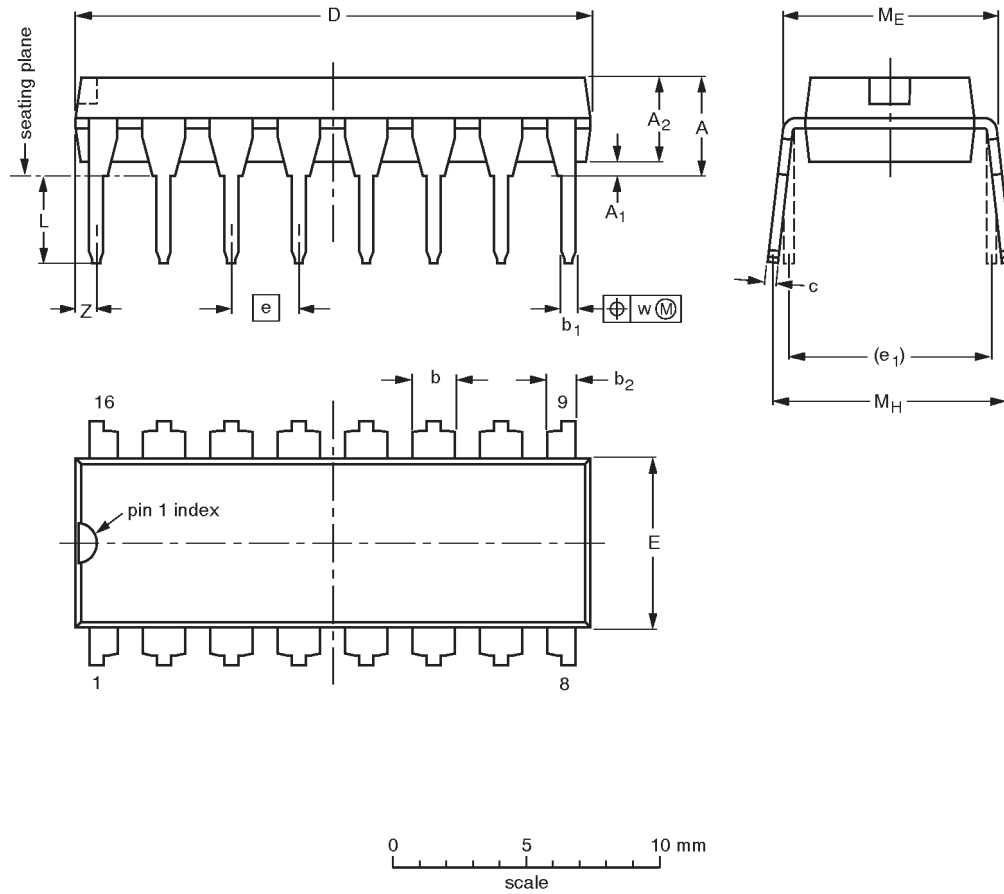
SF00006

# 1-of-8 decoder/demultiplexer

# 74F138

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

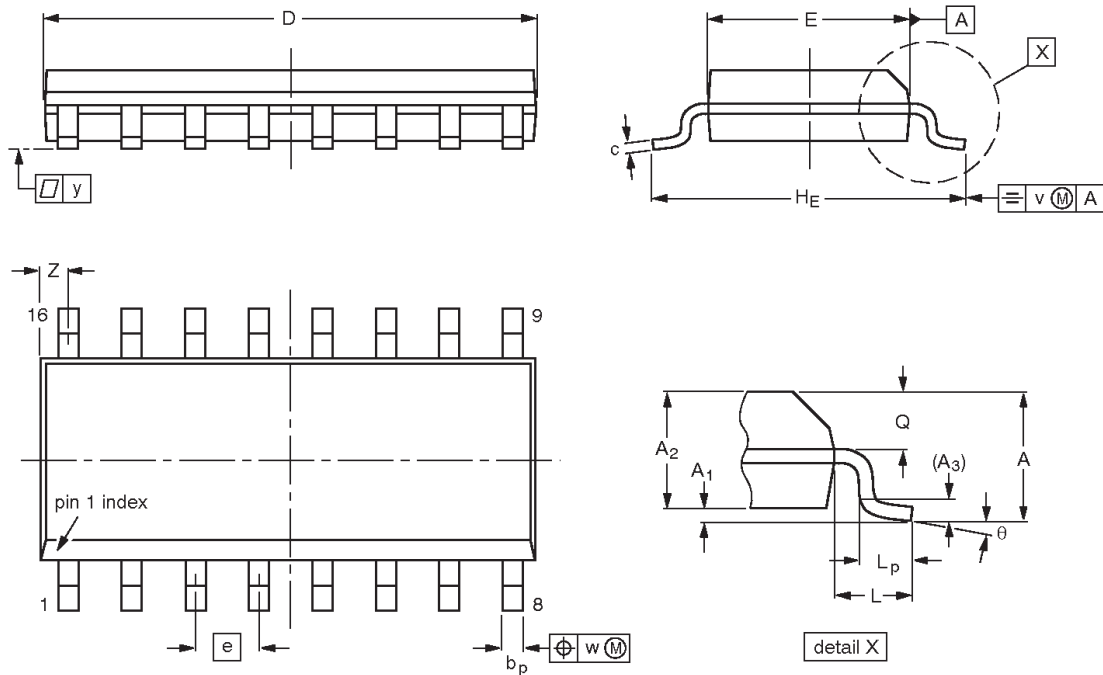
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

# 1-of-8 decoder/demultiplexer

# 74F138

**SO16: plastic small outline package; 16 leads; body width 3.9 mm**

**SOT109-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23 97-05-22

## 1-of-8 decoder/demultiplexer

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**Data sheet status**

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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 811 East Arques Avenue  
 P.O. Box 3409  
 Sunnyvale, California 94088-3409  
 Telephone 800-234-7381

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