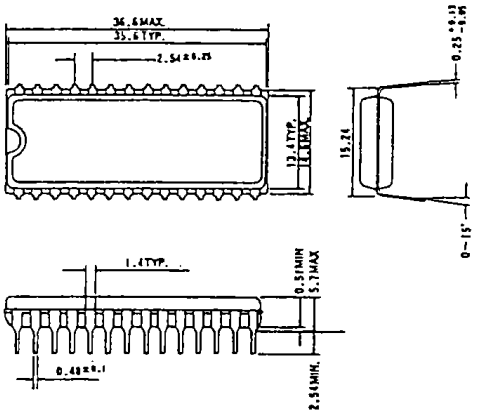
SM5828B

8-bit Advanced Shift Register

iable-length 8-bit shift register fabricated using NPC's original molybdenum-gate
ne external input pins of the IC allow 1 to 128-step shift register settings. The
ximum frequency of 20 MHz ensures high-speed operation.
used, data is retained even when the shift clock is stopped.

■ PACKAGE DIMENSIONS (Unit: mm)

• Plastic (SM5828BP)



ings
allel input/output
n circulation and non-
ing clock frequency 20
V ±0.5 V
compatible
ic, ceramic)
e CMOS construction

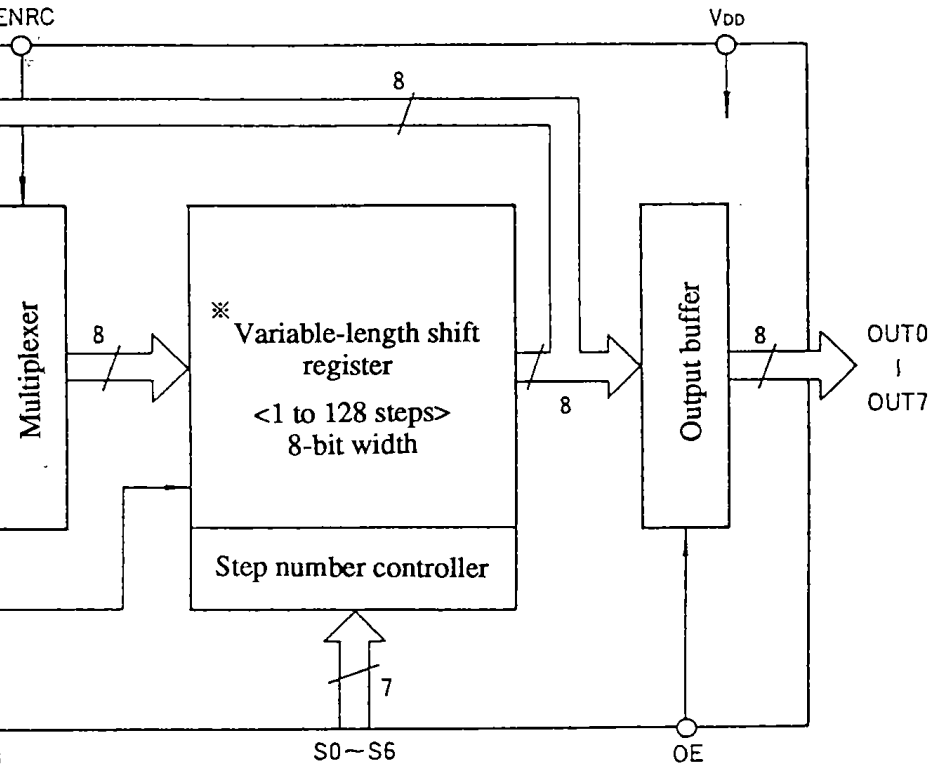
ES

Package
28-pin plastic DIP
28-pin ceramic DIP

• Ceramic (SM5828BC)

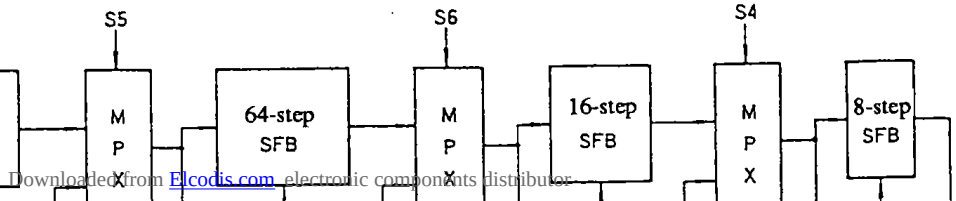
VIEW

AM



ation of the variable-length shift register

shows the configuration of the variable-length shift register. According to the 6, the multiplexer selects the output of each shift register block, realizing 1 to 128-. The last 1-step register is always used.



ame	Description
N0	Data input (0)
N1	Data input (1)
N2	Data input (2)
N3	Data input (3)
N4	Data input (4)
N5	Data input (5)
N6	Data input (6)
N7	Data input (7)
S6	Data length select (6)
S5	Data length select (5)
S4	Data length select (4)
S3	Data length select (3)
CLK	Clock input
Vss	Ground
S2	Register length select (2)
S1	Register length select (1)
S0	Register length select (0)
UT7	Data output (7)
UT6	Data output (6)
UT5	Data output (5)
UT4	Data output (4)
UT3	Data output (3)
UT2	Data output (2)
UT1	Data output (1)
UT0	Data output (0)
OE	Output enable
NRC	Circulation and non-circulation control
VDD	Power supply (5 ± 0.5 V)

RISTICS

SM5828BP ... Ta = -20 to 70 °C, VDD = 4.5 to 5.5 V, Vss = 0 V
SM5828BC... Ta = -30 to 85 °C, VDD = 4.5 to 5.5 V, Vss = 0 V unless otherwise noted.)

Pin	Symbol	Condition	Rating			Unit	Remarks
			MIN	TYP	MAX		
V_{DD}	I_{ST}	V_{DD} - 5.5V		0.01	100	μA	
V_{DD}	I_{DD}	Note			100	mA	See Figure 2.
*1	V_{IH}		2.4			V	
	V_{IL}				0.5		
*2	V_{OH}	I_{OH} = – 0.4mA	2.5			V	
	V_{OL}	I_{OL}= 1.6mA			0.4		
*1	I_{IL}	V_{IN} = 0V		7	20	μA	
*1	I_{LH}	V_{IN} = V_{DD}			1	μA	
*2	I_{ZH}	V_{OUT} = V_{DD}			5	μA	
	I_{ZL}	V_{OUT} = 0V			5		

ENRC, IN0 to IN7, S0 to S6, CLK, OE
OUT1 to OUT7

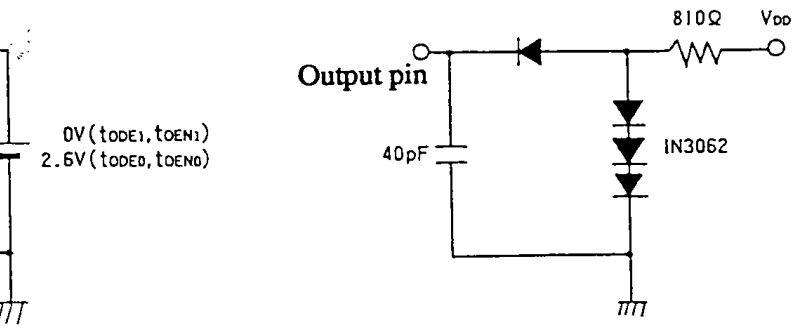
lock frequency f_{CLK} = 20 MHz, OE pin = 0 V
lock input voltage V_{IH} = 2.4 V, V_{IL} = 0.5 V

RISTICS

(VDD = 4.5 to 5.5 V, Vss = 0 V unless otherwise noted)

Pin	Symbol	Condition	BP type (–20 to 70°C) BC type(–20 to 85°C)			BC type (–30 to 70°C)			Unit	Remarks
			MIN	TYP	MAX	MIN	TYP	MAX		
CLK	f_{CLK}	V_{IH} = 2.4V, V_{IL} = 0.5V			20			20	MHz	
CLK	t_{cr}				100			100	nsec	
CLK	t_{cf}				100			100	nsec	
CLK	t_{WH}		20			20			nsec	
N0 to 7	t_{S1}	Register length: LR = 1 to 16 steps Figure 1	60			55			nsec	Figure 1
		Register length: LR								

(Note 2) Load condition 2



TING

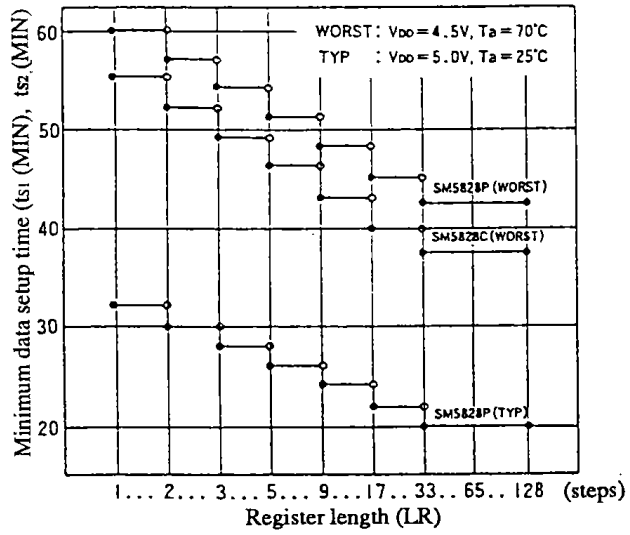
steps by using the register length select pins S0 to S6.

S4)+8(S3)+4•(S2)+2•(S1)+(S0)+1

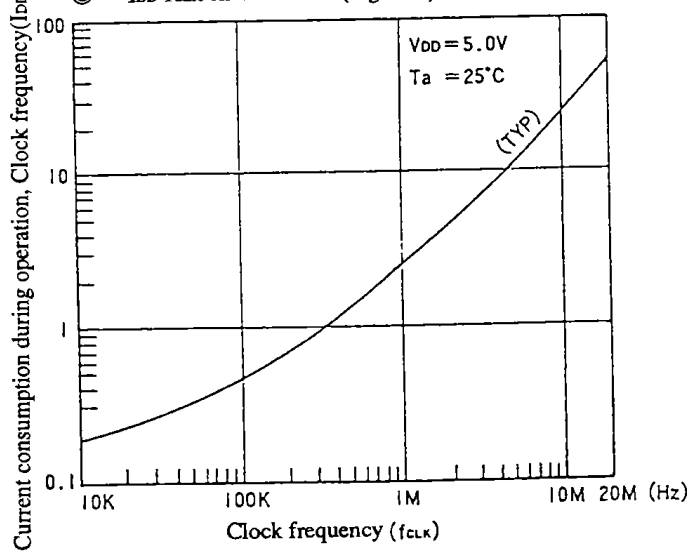
4	S3	S2	S2	S0
1	1	1	1	1
1	1	1	1	0
1	1	1	0	1
1	1	1	0	0
	.			
	.			
	.			
0	0	0	0	1
0	0	0	0	0
	.			
	.			
	.			
0	0	0	1	0
0	0	0	0	1
0	0	0	0	0

ACTERISTICS

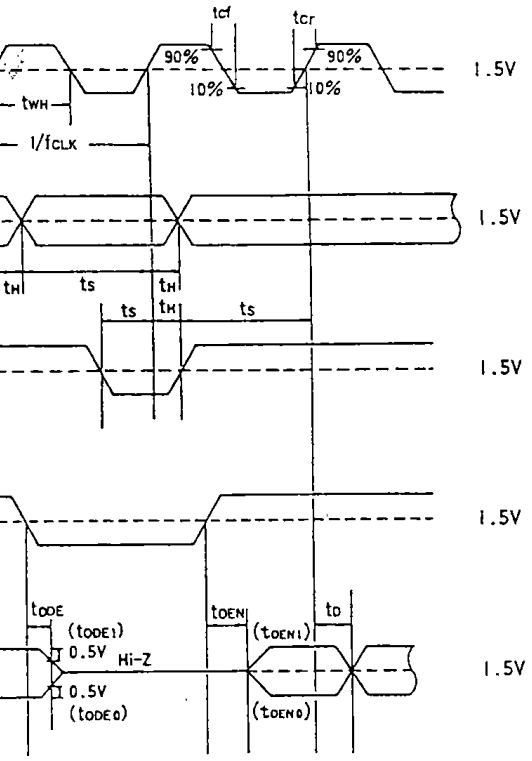
◎ t_{s1}, t_{s2} (MIN) — - LR characteristic (Figure 1)



◎ - IDD-fCLK characteristic (Figure 2)



◎ - t_{OEN}, t_{ODE}, t_D - Ta characteristic (Figure 3)



ON (Block diagram of a 16-bit FIR digital filter using the SM5828B)