Features

- **Single Chip Synthesizer + Effects, Typical Application Includes:**
  - **Wavetable Synthesis, Serial Midi In & Out, Parallel MIDI**
  - **Effects: Reverb + Chorus, on MIDI and/or Audio In**
  - **Surround on 2 or 4 Speakers with Intensity/Delay Control**
  - **Equalizer: 4 Bands, Parametric**
  - **Audio-In Processing through Echo, Equalizer, Surround**
- **Low Chip Count**
  - **Synthesizer, ROM/Flash, DAC**
  - **Effects RAM is Built-in (32K x 16)**
- **Low Power**
  - **23 mA Typ. Operating**
  - **Single 3.3V Supply**
  - **Built-in 1.8V Regulator with Power Down Mode**
- **High Quality Wavetable Synthesis**
  - **16-bit Samples, 48 kHz Sampling Rate, 24 dB Digital Filter per Voice**
  - **Up to 64 Voices Polyphony**
  - **Up to 16 Mega x 16 ROM for Firmware, and PCM Data**
- **Available Wavetable Firmware and Sample Sets**
  - **CleanWave8 Low Cost General MIDI 1 Megabyte Firmware + Sample Set**
  - **CleanWave32 High Quality 4 Megabyte Firmware + Sample Set**
  - **CleanWave64 Top Quality 8 Megabyte Firmware + Sample Set**
  - **Other Sample Sets Available under Special Conditions**
- **Fast Product to Market**
  - **Enhanced P16 Processor with C Compiler**
  - **Built-in ROM Debugger**
  - **Flash Programmer through Dedicated Pin**
- **Small Footprint**
  - **14 x 14 mm, 0.5 mm Pitch, 100-lead LQFP Package**
- **Typical Applications**
  - **Portable Telephones**
  - **Computer Karaokes, Portable Karaokes**
  - **Keyboards, Portable Keyboards Instruments**

1. Description

The ATSAM2533 is a low cost derivative of the ATSAM97xx series. It retains the same high quality synthesis with up to 64 voices polyphony. The ATSAM2533 maximum wavetable memory is 32 MBytes and the parallel communication is through a standard 8-bit port.

The integrated 32K x 16 RAM allows for high quality effects without additional components.

The highly integrated architecture from ATSAM2533 combines a specialized high performance RISC-based digital signal processor (Synthesis/DSP) and a general purpose 16-bit CISC-based control processor on a single chip. An on-chip memory management unit (MMU) allows the synthesis/DSP and the control processor to share external ROM and/or RAM memory devices. An intelligent peripheral I/O interface function handles other I/O interfaces, such as the 8-bit parallel, the on-chip MIDI

Audio Processing

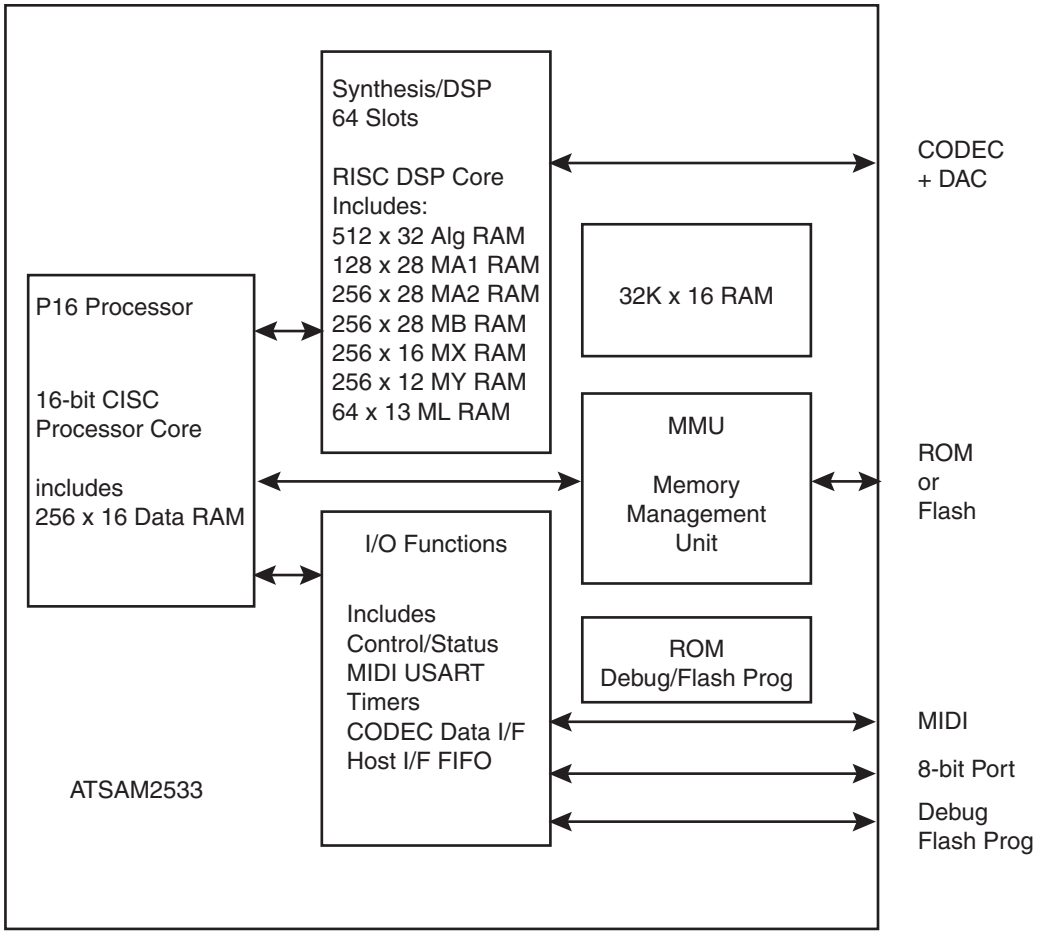
ATSAM2533 Low-power Synthesizer with Effects and Built-in RAM

6396A–DRMSD–15-Oct-08

UART, and the CODEC control interface, with minimum intervention from the control processor.

2. ATSAM2533 IC Architecture Block Diagram

Figure 2-1. ATSAM2533 IC Architecture Block Diagram



3. Functional Description

3.1 Synthesis/DSP Engine

The synthesis/DSP engine operates on a frame timing basis with the frame subdivided into 64 processes slots. Each process is itself divided into 16 micro-instructions known as an “algorithm” Up to 32 synthesis/DSP algorithms can be stored on-chip in the Alg RAM memory, allowing the device to be programmed for a number of audio signal generation/processing applications. The synthesis/DSP engine is capable of generating 64 simultaneous voices using algorithms such as wavetable synthesis with interpolation, alternate loop and 24dB resonant filtering for each voice. Slots may be linked together (ML RAM) to allow implementation of more complex synthesis algorithms.

A typical application will use half the capacity of the synthesis/DSP engine for synthesis, thus providing state of the art 32-voice wavetable polyphony. The remaining processing power will be used for typical functions like reverberation, chorus, audio in processing, surround effect, equalizer, etc.

Frequently accessed synthesis/DSP parameter data are stored into 5 banks of on-chip RAM memory. Sample data or delay lines, which are accessed relatively infrequently are stored in external ROM or internal 32K x16 RAM memory. The combination of localized micro-program memory and localized parameter data allows micro-instructions to execute in 20 ns (50 MIPS). Separate busses from each of the on-chip parameter RAM memory banks allow highly parallel data movement to increase the effectiveness of each micro-instruction. With this architecture, a single micro-instruction can accomplish up to 6 simultaneous operations (add, multiply, load, store, etc.), providing a potential throughput of 300 million operations per second (MOPS).

3.2 Enhanced P16 Control Processor and I/O Functions

The Enhanced P16 control processor is the new version of P16 processor with added instructions allowing C compiling. The P16 control processor is a general purpose 16-bit CISC processor core, which runs from external memory. It includes 256 words of local RAM data memory.

The P16 control processor writes to the parameter RAM blocks within the synthesis/DSP core in order to control the synthesis process. In a typical application, the P16 control processor parses and interprets incoming commands from the MIDI UART or from the parallel 8-bit interface and then controls the Synthesis/DSP by writing into the parameter RAM banks in the DSP core. Slowly changing synthesis functions, such as LFOs, are implemented in the P16 control processor by periodically updating the DSP parameter RAM variables.

The P16 control processor interfaces with other peripheral devices, such as the system control and status registers, the on-chip MIDI UART, the on-chip timers and the parallel 8-bit interface through specialized “intelligent” peripheral I/O logic. This I/O logic automates many of the system I/O transfers to minimize the amount of overhead processing required from the P16.

The parallel 8-bit interface is implemented using one address lines (A0), a chip select signal, read and write strobes from the host and an 8-bit data bus (D0-D7).

Karaoke and keyboard applications can take advantage of the parallel 8-bit interface to communicate with the ATSAM2533 at high speed, with the MIDI IN and MIDI OUT signals remaining available.

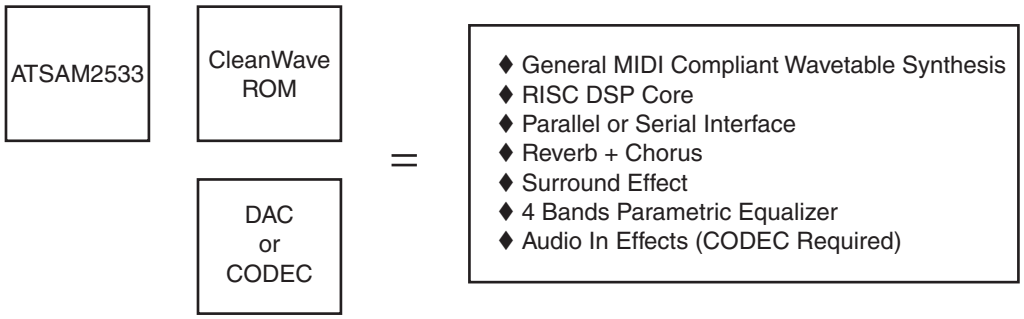
3.3 Memory Management Unit (MMU)

The Memory Management Unit (MMU) block allows external ROM/Flash and/or internal 32K x 16 RAM memory resources to be shared between the synthesis/DSP and the P16 control processor. This allows a single device (i.e. internal RAM) to serve as delay lines for the synthesis/DSP and as data memory for the P16 control processor.

4. Typical Design Applications

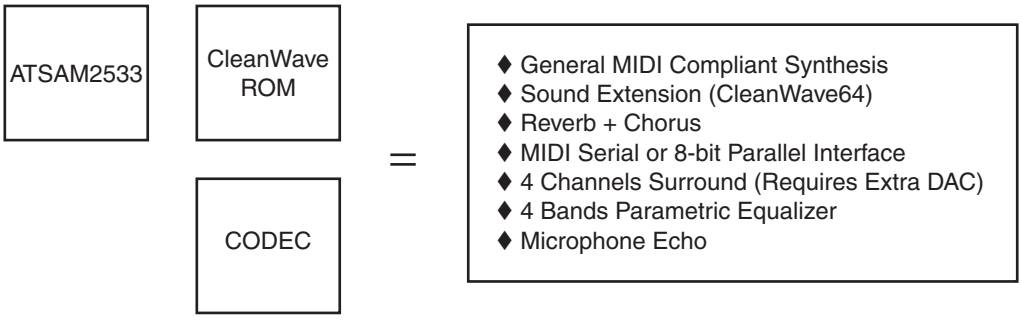
4.1 Portable Telephone

Figure 4-1. Portable Telephone



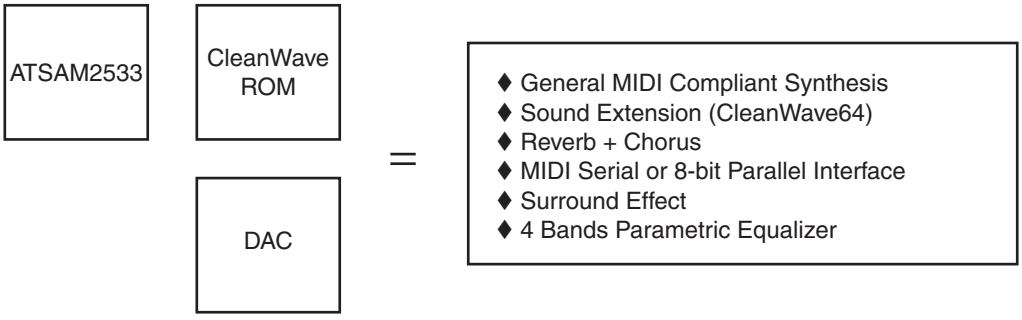
4.2 Low Cost Karaoke, Hand-held Karaoke

Figure 4-2. Low Cost Karaoke, Hand-held Karaoke



4.3 Low Cost Keyboard Instrument

Figure 4-3. Low Cost Keyboard Instrument



5. Pinout

5.1 Pin Description by Function 100-pin LQFP Package

- 5VT indicates a 5 volt tolerant input or i/O pin.

Table 5-1. ATSAM2523 Pinout by Name

Name	Pin#	TYPE	Function
GND	1, 12, 26, 41, 51, 69, 76, 77, 84	PWR	Power ground - all GND pins should be returned to digital ground
VD18	79	PWR	Power for the internal PLL, + 1.8V nominal (1.8V ± 10%). These pins can be connected to the output of the regulator OUTVC18 (pin 34). A 100 nF decoupling capacitor should be connected between this pin and PLL ground (pin77)
VD33	13, 25, 33, 42, 50, 59, 68, 75, 83, 100	PWR	Periphery power + 3V to 3.6V. All VD33 pins should be returned to nominal +3.3V.
OUTVC18	34	PWR	3.3V to 1.8 V regulator output. The built-in regulator gives 1.8V for internal use (core supply). PLL supply pin VD18 could also be connected to this pin. Decoupling capacitors 470pF in parallel with 2.2 or 4.7µF must be connected between OUTVC18 and GND.
D0-D7	4-11	I/O 5VT	8 bit data bus to host processor. Information on these pins is parallel MIDI
$\overline{CS}$	2	IN 5VT	Chip select from host, active low.
$\overline{WR}$	99	IN 5VT	Write from host, active low.
$\overline{RD}$	3	IN 5VT	Read from host, active low.
A0	98	IN 5VT	Select address of slave 8-bit interface registers: 0: data registers (read/write) 1: status register (read) control register (write) This pin has a built-in pull down.
IRQ	97	OUT	Slave 8bit interface interrupt request. High when data is ready to be transferred from chip to host. Reset by a read from host (CS/=0 and RD/=0)
$\overline{RESET}$	82	IN 5VT	Master reset input, active low.
X1,X2	80, 81	–	Crystal connection. Crystal frequency should be Fs * 256 (typ 12.288 MHz) Xtal frequency is internally multiplied by 4 to provide the IC master clock. An external 12.288 MHz clock can also be used on X1 (Analog or 3.3V CMOS logic). X2 cannot be used to drive external ICs, use CKOUT instead.
CKOUT	88	OUT	Buffered X2 output, can be used to drive external DAC master clock (256 * Fs)
DABD0-1	91, 92	OUT	Two stereo serial audio data output (4 audio channels). Each output holds 64 bits (2 x 32) of serial data per frame. Audio data has up to 20 bits precision.
CLBD	89	OUT	Audio data bit clock, provides timing to DABD0-1, DAAD.
WSBD	90	OUT	Audio data word select. The timing of WSBD can be selected to be I2S or Japanese compatible.
DAAD	93	IN 5VT	Stereo serial audio data input.
P0-P3	49, 52-54	I/O 5VT	General purpose programmable I/O pins. These pins have a built-in pull down.

Table 5-1. ATSAM2523 Pinout by Name (Continued)

Name	Pin#	TYPE	Function
DBCLK	85	IN 5VT	Debug clock, should be connected to VD33 under normal operation. If DBCLK is found low just after RESET, then the internal ROM debugger/Flash programmer is started
DBDATA	87	I/O 5VT	Debug data, allows serial communication for debug/Flash programming. This pin has a built-in pull down.
DBACK	86	OUT	Debug ack, toggled each time a bit is received/sent on DBDATA
MIDI IN	96	IN 5VT	MIDI IN, input. This pin has a built-in pull up.
MIDI OUT	94	OUT	MIDI OUT, output.
WA0-23	35-40, 43-48, 55-58, 60-67	OUT	External memory address (ROM/Flash). Up to 32 Mega bytes.
WD0-15	14-24, 27-31	I/O 5VT	External ROM/Flash data.
$\overline{\text{WCS}}$	70	OUT	External ROM/Flash chip select, active low.
$\overline{\text{WWE}}$	72	OUT	External Flash write enable, active low.
$\overline{\text{WOE}}$	71	OUT	External ROM/Flash output enable, active low.
TEST0-1	95, 78	IN	Test pins, should be returned to GND.
$\overline{\text{PDWN}}$	32	IN	Power down, active low. When power down is active, $\overline{\text{WCS}}$, $\overline{\text{WWE}}$, $\overline{\text{WOE}}$, address and data lines are floated. All other outputs are set to 0. The crystal oscillator is stopped, OUTVC18 is set to 0 and 1.8V supply voltage is removed from the core. To exit from power down, $\overline{\text{PDWN}}$ must be set to VD33, then $\overline{\text{RESET}}$ applied. When unused this pin must be connected to VD33.
NC	73, 74	–	Not connected pins.

5.2 Pinout by Pin Number

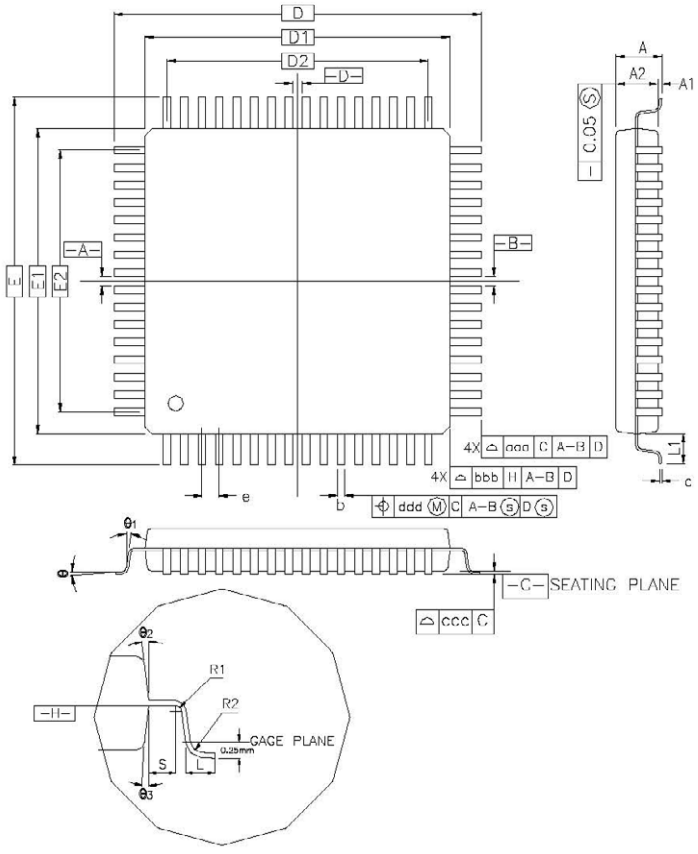
Table 5-2. ATSAM2523 Pinout by Pin Number

Pin#	Signal Name	Pin#	Signal Name	Pin#	Signal Name	Pin#	Signal Name
1	**GND**	26	**GND**	51	**GND**	76	**GND**
2	$\overline{CS}$	27	WD11	52	P1	77	**GND**
3	$\overline{RD}$	28	WD12	53	P2	78	TEST1
4	D0	29	WD13	54	P3	79	VD18
5	D1	30	WD14	55	WA12	80	X1
6	D2	31	WD15	56	WA13	81	X2
7	D3	32	$\overline{PDWN}$	57	WA14	82	$\overline{RESET}$
8	D4	33	**VD33**	58	WA15	83	**VD33**
9	D5	34	OUTVC18	59	**VD33**	84	**GND**
10	D6	35	WA0	60	WA16	85	DBCLK
11	D7	36	WA1	61	WA17	86	DBACK
12	**GND**	37	WA2	62	WA18	87	DBDATA
13	**VD33**	38	WA3	63	WA19	88	CKOUT
14	WD0	39	WA4	64	WA20	89	CLBD
15	WD1	40	WA5	65	WA21	90	WSBD
16	WD2	41	**GND**	66	WA22	91	DABD0
17	WD3	42	**VD33**	67	WA23	92	DABD1
18	WD4	43	WA6	68	**VD33**	93	DAAD
19	WD5	44	WA7	69	**GND**	94	MIDI_OUT
20	WD6	45	WA8	70	$\overline{WCS}$	95	TEST0
21	WD7	46	WA9	71	$\overline{WOE}$	96	MIDI_IN
22	WD8	47	WA10	72	$\overline{WWE}$	97	IRQ
23	WD9	48	WA11	73	NC	98	A0
24	WD10	49	P0	74	NC	99	$\overline{WR}$
25	**VD33**	50	**VD33**	75	**VD33**	100	**VD33**

6. Marking

7. Mechanical Dimensions

Figure 7-1. 100-lead Quad Flat Pack (LQFP100)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	12.00			0.472		
E2	12.00			0.472		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

8. Electrical Characteristics

8.1 Absolute Maximum Ratings(*)

All voltages with respect to 0V, GND = 0V.

Temperature under bias ..... -55°C to +125°C Storage Temperature ..... -65°C to +150°C Voltage on any 5 volt tolerant pin ..... -0.3 to 5.5V Voltage on any non 5 volt tolerant pin ..... -0.3 to V_{D33} + 0.3V Supply Voltage ..... V_{D33} .....-0.3V to 3.6V V_{D18} .....-0.3V to 2V Maximum IOL per I/O pin..... 10 mA Maximum IOH per I/O pin ..... 10 mA Maximum Output current from OUTVC18 pin (max duration = 1sec) IREGO ..... 70 mA	*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8.2 Recommended Operating Conditions

Table 8-1. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Mx	Unit
V_{D33}	Supply voltage	3	3.3	3.6	V
V_{D18}	Supply voltage (PLL)	1.65	1.8	1.95	V
IREGO	OUTVC18 output current	-	30		mA
T_A	Operating ambient temperature	-25	-	70	°C

8.3 DC Characteristics

Table 8-2. DC Characteristics (T_A = 25°C, V_{D33} = 3.3V ± 10%, V_{D18} = 1.8V ± 10%)

Symbol	Parameter	Min	Typ	Mx	Unit
V_{IL}	Low level input voltage	-0.3	-	0.8	V
V_{IH}	High level input voltage on 5VT pins	2	-	5.5	V
V_{IH}	High level input voltage on non-5VT pins	2	-	3.6	V
V_{OL}	Low level output voltage IOL=4mA	-	-	0.4	V
V_{OH}	High level output voltage IOH=4mA	VD33-0.4	-	-	V
ID18	Power supply current at (crystal freq.=12.288 MHz)		0.7		mA
ID33			22		mA
–	Power down supply current		0.6		mA
Rud	Pull-up or Pull-down resistor	8	13	25	kOhm

9. Timings

All timing conditions: V_{D33} =3.3V, V_{D18} =1.8V, T_A = 25°C, all outputs except X2 have load capacitance = 30 pF.

All timings refer to tck, which is the internal master clock period.

The internal master clock frequency is 4 times the frequency at pin X1. Therefore tck = txtal/4.

The sampling rate is given by 1/(tck*1024). The maximum crystal frequency/clock frequency at X1 is 12.288 MHz (48 kHz sampling rate).

9.1 Crystal Frequency Selection Considerations

There is a trade-off between the crystal frequency and the support of widely available external ROM/Flash components. Table 9-1 allows to select the best fit for a given application;

Table 9-1. Crystal Frequency Selection Chart

Sample Rate (kHz)	Xtal (MHz)	tck (ns)	ROM tA (ns)
48	12.288	20.35	92
44.1	11.2896	22.14	101
37.5	9.60	26.04	120
31.25	8.00	31.25	146

Using 12.288 MHz crystal frequency allows to use widely available ROM/Flash with 90 ns access time, while providing state of the art 48 kHz sampling rate.

9.2 PC Host Interface

9.2.1 Timings

Figure 9-1. Host Interface Read Cycle

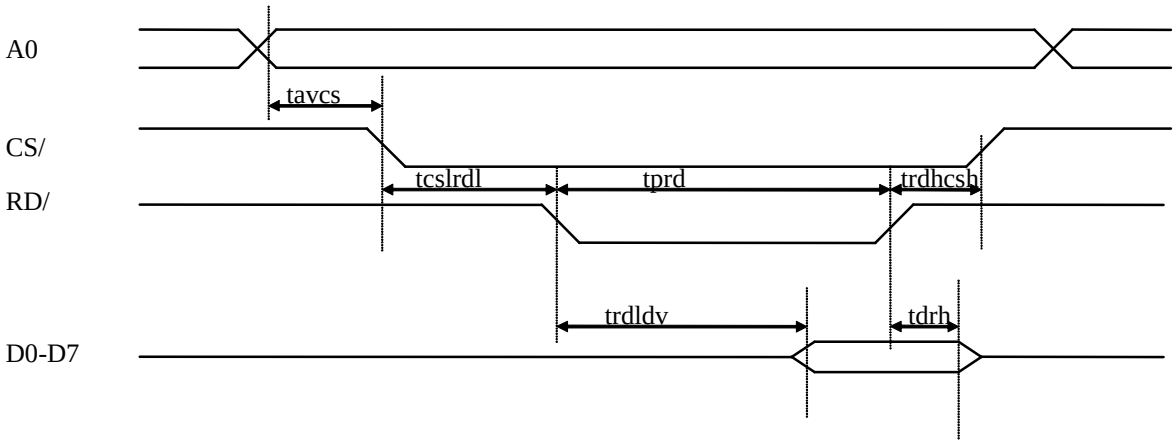


Figure 9-2. Host Interface Write Cycle

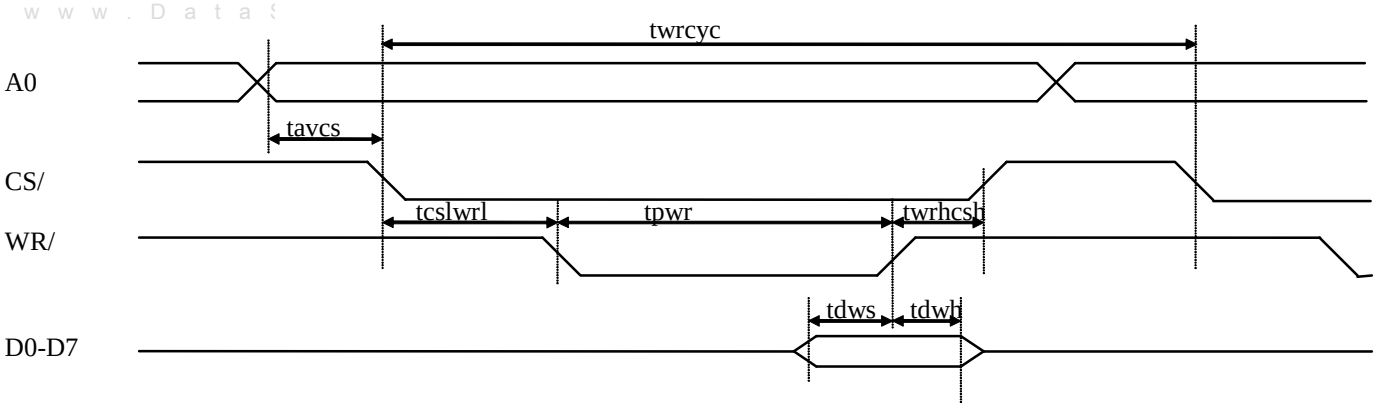


Table 9-2. Timing Parameters

Symbol	Parameter	Min	Typ	Mx	Unit
tavcs	Address valid to chip select low	0	-	-	ns
tcslrdl	Chip select low to $\overline{RD}$ low	5	-	-	ns
trdhcsh	$\overline{RD}$ high to $\overline{CS}$ high	5	-	-	ns
tprd	$\overline{RD}$ pulse width	50	-	-	ns
trdldv	Data out valid from $\overline{RD}$	-	-	20	ns
tdrh	Data out hold from $\overline{RD}$	5	-	10	ns
tcslrwrl	Chip select low to $\overline{WR}$ low	5	-	-	ns
twrhcsh	$\overline{WR}$ high to $\overline{CS}$ high	5	-	-	ns
tpwr	$\overline{WR}$ pulse width	50	-	-	ns
tdws	Write data setup time	10	-	-	ns
tdwh	Write data hold time	0	-	-	ns
twrcyc	Write cycle	128	-	-	tck

9.2.2 IO Status Register

7	6	5	4	3	2	1	0
TE	RF	X	X	X	X	X	X

Status register is read when A0 = 1, $\overline{RD}$ = 0, $\overline{CS}$ = 0.

- **TE: Transmit Empty**

If 0, data from ATSAM2533 to host is pending and IRQ is high. Reading the data at A0 = 0 will set TE to 1 and clear IRQ.

- **RF: Receiver Full**

If 0, then ATSAM2533 is ready to accept DATA from host.

9.3 External ROM/Flash Timings

Figure 9-3. RO/Flash Read Cycle

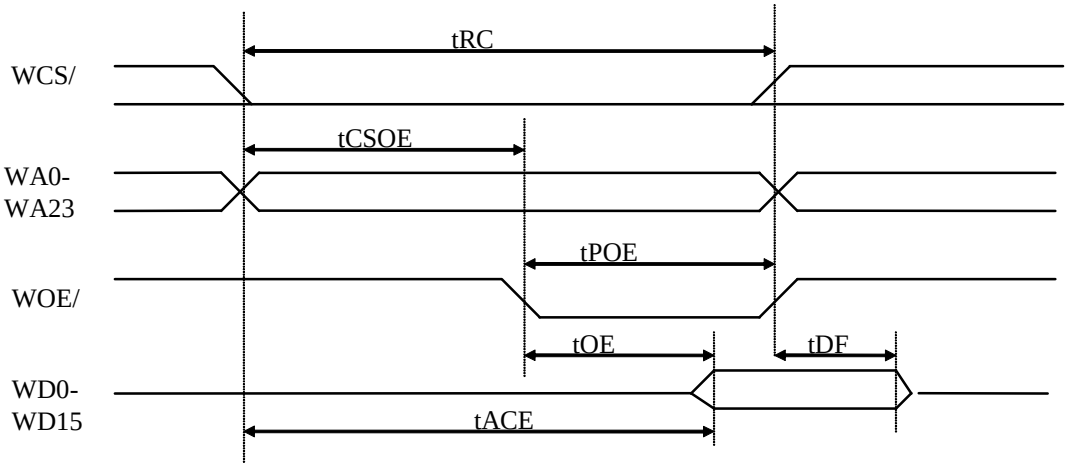


Table 9-3. External ROM/Flash Timing Parameters

Symbol	Parameter	Min	Typ	Mx	Unit
tRC	Read cycle time	5*tck	-	6*tck	ns
tCSOE	Chip select low/address valid to $\overline{WOE}$ low	2*tck-5	-	3*tck+5	ns
tPOE	Output enable pulse width	-	3*tck	-	ns
tACE	Chip select/address access time	5*tck-5	-	-	ns
tOE	Output enable access time	3*tck-5	-	-	ns
tDF	Chip select or $\overline{WOE}$ high to input data Hi-Z	0	-	2*tck-5	ns

9.4 External Flash Write Timings

Figure 9-4. External Flash Write Cycle

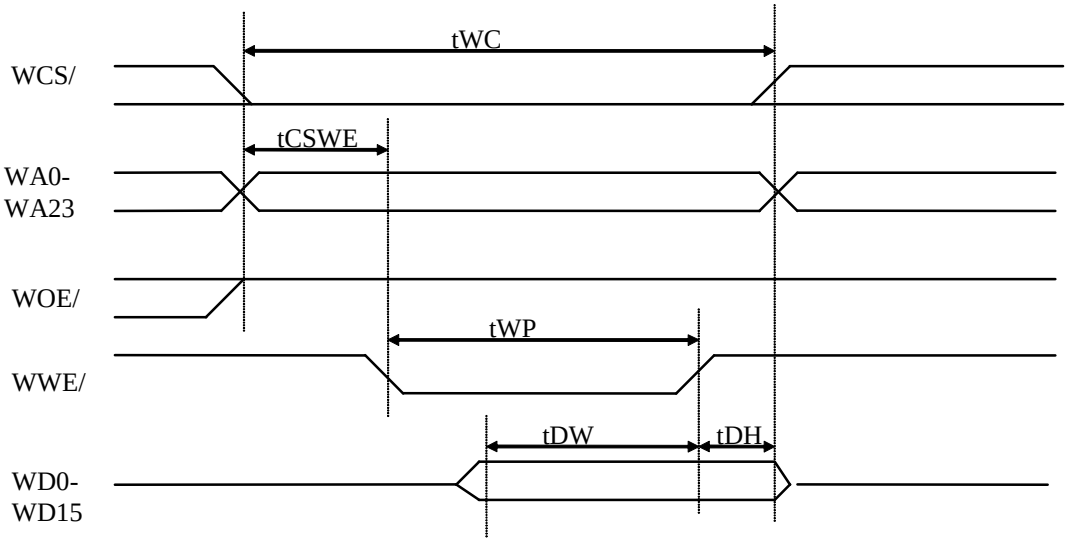


Table 9-4. External Flash Write Timing Parameters

Symbol	Parameter	Min	Typ	Mx	Unit
tWC	Write cycle time	5*tck	-	6*tck	ns
tCSWE	Write enable low from $\overline{CS}$ or Address or $\overline{WOE}$	2*tck-10	-	-	ns
tWP	Write pulse width	-	4*tck	-	ns
tDW	Data out setup time	4*tck-10	-	-	ns
tDH	Data out hold time	10	-	-	ns

9.5 Digital Audio Timing

Figure 9-5. Digital Audio Timing

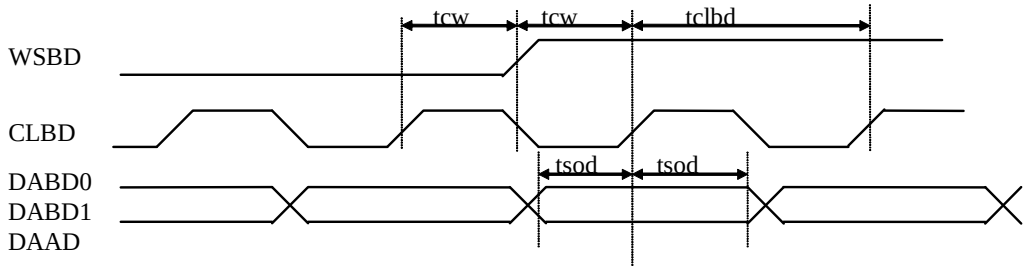
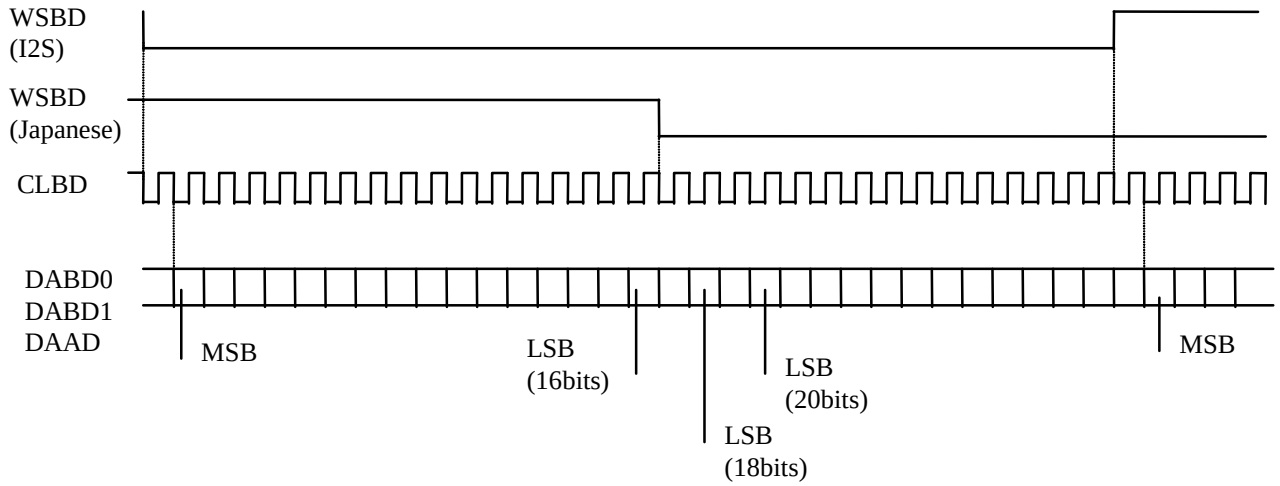


Table 9-5. Digital Audio Timing Parameters

Symbol	Parameter	Min	Typ	Mx	Unit
tcw	CLBD rising to WSBD change	8*tck-10	-	-	ns
tsod	DABD valid prior/after CLBD rising	8*tck-10	-	-	ns
tclbd	CLBD cycle time	-	16*tck	-	ns

Figure 9-6. Digital Audio Frame Format



Note:

- Selection between I2S and Japanese format is a firmware option.
- DAAD is 16 bits only.

10. Reset and Power-down

During power-up, the $\overline{\text{RESET}}$ input should be held low until the crystal oscillator and PLL are stabilized, which can take about 20ms.

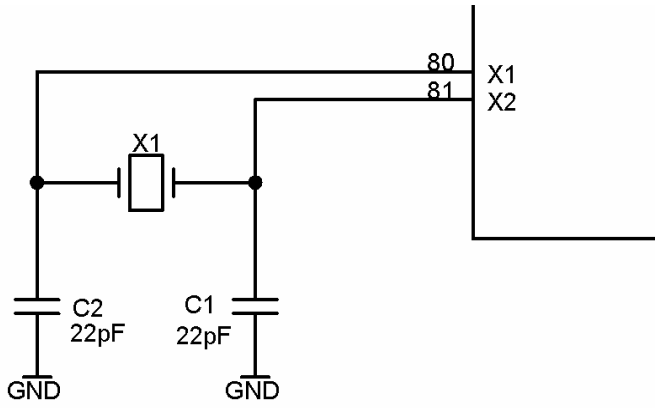
After the low to high transition of $\overline{\text{RESET}}$, following happens:

- The Synthesis/DSP enters an idle state.
- P16 program execution starts from address 0100H in ROM space ($\overline{\text{WCS}}$ low).

If $\overline{\text{PDWN}}$ is asserted low and VD18 connected to OUTVC18, then the crystal oscillator and PLL will be stopped. The chip enters a deep power down sleep mode, as power is removed from the core. To exit power down, $\overline{\text{PDWN}}$ has to be asserted high, then $\overline{\text{RESET}}$ applied.

11. Recommended Crystal Compensation

Figure 11-1. Recommended Crystal Compensation



12. Recommended Board Layout

Like all HCMOS high integration ICs, following simple rules of board layout are mandatory for reliable operation:

- GND, VD33, VD18 distribution, decouplings

All GND, VD33, VD18 pins should be connected. A GND plane is strongly recommended below the ATSAM2533. The board GND + VD33 planes could be in grid form to minimize EMI.

Recommended VD18 decoupling is 0.1 µF close to the VD18 pin and 470 pF in parallel with 2.2 or 4.7 µF close to OUTVC18 pin. VD33 requires 0.1 uF at each corner of the IC with an additional 10 µFT capacitor that should be placed close to the crystal.

- Crystal, LFT

The paths between the crystal, the crystal compensation capacitors and the ATSAM2533 should be short and shielded. The ground return from the compensation capacitors should be the GND plane from ATSAM2533.

- Busses

Parallel layout from D0-D7 and WA0-WA23/WD0-WD15 should be avoided. The D0-D7 bus is an asynchronous type bus. Even on short distances, it can induce pulses on WA0-WA23/WD0-WD15 which can corrupt address and/or data on these busses.

A ground plane should be implemented below the D0-D7 bus, which is connected to the host and to the ATSAM2533 GND.

A ground plane should be implemented below the WA0-WA23/WD0-WD15 bus, which is connected to the ROM/Flash grounds and to the ATSAM2533.

- Analog section

A specific AGND ground plane should be provided, which is connected to the GND ground by a single trace. No digital signals should cross the AGND plane.

Refer to the CODEC vendor recommended layout for correct implementation of the analog section.

13. Revision History

Table 13-1.

Document Ref.	Comments	Change Request Ref
6396A	First issue.	

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