HD14006B

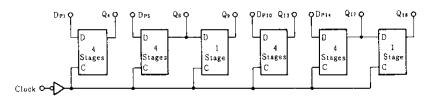
18-bit Static Shift Register

The HD14006B shift register is comprised of four separate shift register sections sharing a common clock: two sections have four stages and two sections have five stages with an output tap on both the fourth and fifth stages. This makes it possible to obtain a shift register of 4, 5, 8, 9, 10, 12, 13, 14, 16, 17 or 18 bits by appropriate selection of inputs and outputs. This part is particularly useful in serial shift registers and time delay circuits.

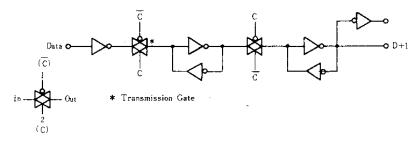
■ FEATURES

- Output Transitions Occur on the Falling Edge of the Clock Pulse
- Quiescent Current = 5nA/pkg typ @5V
- Fully Static Operation
- 8MHz Shift Rate Typical
- Can be Cascaded to Provide Longer Shift Register Lengths
- Supply Voltage Range = 3 to 18V
- Capable of Driving One Lowpower Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4006B and MC14006B

■BLOCK DIAGRAM

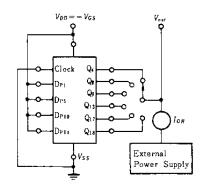


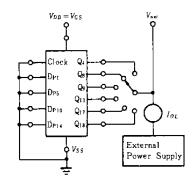
■LOGIC DIAGRAM



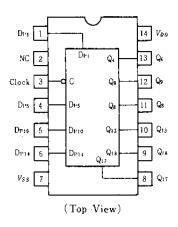
■ DC CHARACTERISTIC TEST CIRCUIT







PIN ARRANGEMENT



TRUTH TABLE

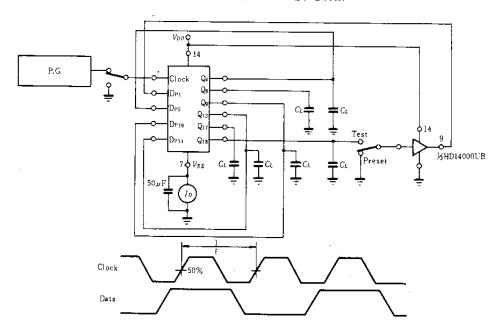
D _n	С	Q _{n+1}
0		0
1 .		1
×		Q,

× : Don't Care

■ ELECTRICAL CHARACTERISTICS

Characteristic	Sumb - 1		Trade C. Pro	2	40℃		25 ℃			85 °C		
Characteristic Symbol V_{D_1}		$V_{DD}(\mathbf{V})$	Test Conditions		max	min	typ	max	min	max	Unit	
Output Voltage		5.0	$V_{in} = V_{DD}$ or 0	_	0.05		0	0.05	-	0.05	v	
	V_{oL}	10		_	0.05	_	0	0.05	-	0.05		
		15			0.05	_	0	0.05		0.05		
		5.0		4.95	_	4.95	5.0	_	4.95		v	
	Von	10	$V_{in}=0$ or V_{DD}	9.95	_	9.95	10		9.95	-		
		15		14.95		14.95	15		14.95	_		
		5.0	$V_{out}=4.5$ or 0.5 V	_	1.5	_	2.25	1.5		1.5	v	
	V_{tL}	10	$V_{out} = 9.0 \text{ or } 1.0 \text{V}$		3.0	_	4.50	3.0	_	3.0		
Input Voltage		15	$V_{out} = 13.5 \text{ or } 1.5 \text{V}$		4.0	_	6.75	4.0	_	4.0		
		5.0	V _{out} =0.5 or 4.5V	3.5	_	3.5	2.75		3.5	_	v	
	V_{tB}	10	$V_{out} = 1.0 \text{ or } 9.0 \text{V}$	7.0		7.0	5.50	-	7.0	_		
		15	$V_{\text{out}} = 1.5 \text{ or } 13.5 \text{V}$	11.0		11.0	8.25	_	11.0			
Output Drive Current		5.0	$V_{OH}=2.5\mathrm{V}$	-1.0	-	-0.8	-1.7	-	-0.6		mA	
	Іон	5.0	$V_{OH}=4.6V$	-0.2	_	-0.16	-0.36		-0.12	_		
		10	$V_{0H} = 9.5 \text{V}$	-0.5	_	-0.4	-0.9		-0.3			
		15	$V_{OH} = 13.5 \text{V}$	-1.4	_	-1.2	-3.5	_	-1.0		ı	
		5.0	$V_{OL}=0.4V$	0.52	_	0.44	0.88	_	0.36		mА	
	IoL	10	$V_{OL}=0.5V$	1.3		1.1	2.25		0.9	_		
		15	$V_{ol} = 1.5 \text{V}$	3.6	_	3.0	8.8	_	2.4	_		
Input Current	I_{in}	15			±0.3	_	±0.00001	±0.3		±1.0	μΑ	
Input Capacitance	Cin	_	$V_{in} = 0$			_	5.0	7.5	_		pF	
Quiescent Current	I_{DD}	5.0	Zero Signal,	_	20		0.005	20	_	150		
		10		_	40	_	0,010	40		300	μΑ	
		15	per Package	_	80		0.015	80		600		
	I_T	5.0	Dynamic $+I_{DD}$,	-	_	_	1.3		_		μA	
Total Supply Current*		10	Per Gate,		_	_	2.6					
		15	$C_L = 50 \text{pF}$, $f = 1 \text{kHz}$	_	-		3.9				,	

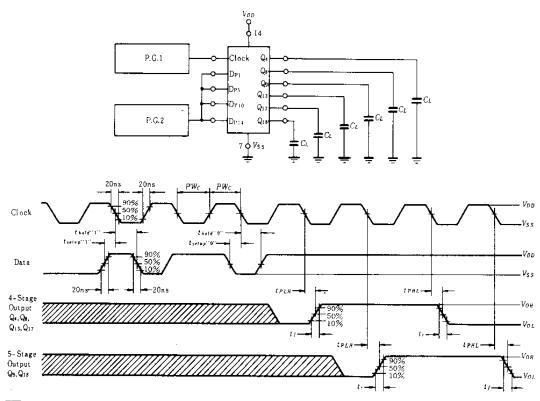
■POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



SWITCHING CHARACTERISTICS $(C_L = 50 \,\mathrm{pF}, Ta = 25 \,^{\circ}\mathrm{C})$

Characteristic	Symbol	$V_{DD}(\mathbf{V})$	min	typ	max	Unit
		5.0	-	180	400	ns
Output Rise Time		10	_	90	200	
·		15	_	65	160	
		5.0	_	100	200	ns
Output Fall Time	t_f	10	_	50	100	
		15		37	80	
		5.0	_	305	600	ns
Propagation Delay Time	t _{PLH} ,	10	-	110	275	
	t _{PHL}	15	_	80	200	
	PW_c	5.0	250	100		ns
Clock Pulse Width		10	125	60		
		15	95	40		
		5.0		5.0	2.0	MHz
Clock Pulse Frequency	PRF	10		8.3	4.0	
		15	_	12	6.0	
		5.0	-	_	15	μ5
Clock Pulse Rise and Fall Time	t_{+}, t_{f}	10	_	_	15	
		15	_	_	15	
		5.0	0	-50	_	ns
Setup Time	tseeup	10	0	-15	_	
		15	0	-8.0		1
		5.0	220	75		
Hold Time	ŧ hate	10	110	25	_	ns
		15	90	20		1

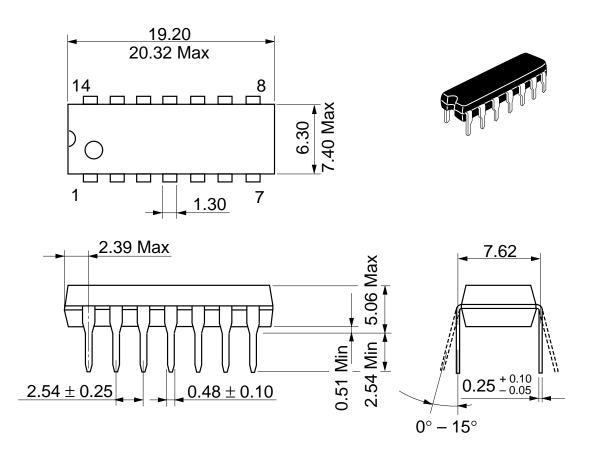
■ SWITCHING TIME TEST CIRCUIT



Output state can change since data previously clocked in might be in either state.



Unit: mm



Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g

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