TAIWAN SEMICONDUCTOR

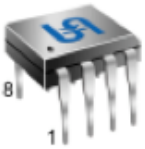
RoHS COMPLIANCE

TS393/TS2903

Low Power Low Offset Voltage Dual Comparators

SOP-8

DIP-8



Pin assignment:

1. Output A
2. Input A (-)
3. Input A (+)
4. Gnd
8. Vcc
7. Output B
6. Input B (-)
5. Input B (+)

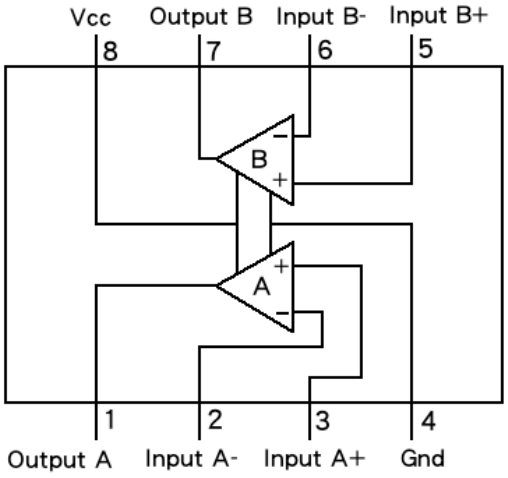
General Description

The TS393/TS2903 is dual independent precision voltage comparators capable of single-supply or split-supply operation. The specifications as low as 2.0 mV make this device an excellent ground level with single-supply operation. Input offset-voltage selection for many applications in consumer automotive, and It is designed to permit a common mode range-to- industrial electronics.

Features

- Output voltage compatible with DTL, ECL, TTL, MOS and CMOS Logic levels
- Low input bias current 25nA
- Low input offset current ±0.5nA
- Low input offset voltage ±2mV(typ)
- Input common mode range to ground level
- Differential input voltage range equal to power supply voltage
- Very low supply current drain (0.4mA) - independent of supply voltage
- Wide single-supply range 2V~36V
- Split-supply range ±1V to ±18V

Block Diagram



Ordering Information

Part No.	Package	Packing
TS393CD C3	DIP-8	50pcs / Tube
TS393CS RL	SOP-8	2.5Kpcs / 13” Reel
TS2903CD C3	DIP-8	50pcs / Tube
TS2903CS RL	SOP-8	2.5Kpcs / 13” Reel

Absolute Maximum Rating

Parameter		Symbol	Limit	Unit
Supply Voltage		V_{CC}	+36 or ±18	V
Differential Input Voltage		V_{IDR}	36	V
Input Common Mode Voltage Range		V_{ICR}	-0.3 to 36	V
Input Current		I_{IN}	50	mA
Output Short Circuit to Ground		I_{SC}	Continuous	
Output Sink Current		I_{SINK}	20	mA
Operating Temperature Range	TS393	T_{OPR}	0 ~ +70	°C
	TS2903		-40 ~ +85	
Junction Temperature		T_J	150	°C
Storage Temperature Range		T_{STG}	-65 ~ +150	°C
Lead Temperature 1.6mm(1/16”) from case for 10Sec.		T_{LEAD}	260	°C

Electrical Characteristics (V_{CC} = 5V, Ta=25°C; unless otherwise specified.)

Characteristics	Symbol	TS393			TS2903			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (note 3)	Vio	--	2	5	--	2	7	mV
Input Offset Current $I_{IN(+)}$ - $I_{IN(-)}$, V_{CM}=0V	Iio	--	--	50	--	50	50	nA
Input Offset Current (note 4) $I_{IN(+)}$ - $I_{IN(-)}$, V_{CM}=0V	I_{IB}	--	--	250	--	200	250	nA
Input Common Mode Voltage Range Vcc=30V	V_{ICR}	-0	--	V_{CC}-1.5	0	--	V_{CC}-1.5	V
Voltage Gain R_L ≥15K, Vcc=15V, Vo=1V~11V	A_{VOL}	50	200	--	25	100	--	V/mV
Large Signal Response Time Vin=TTL Logic Swing. Vref = 1.4V, V_{RL}=5V. R_L=5.1KΩ	--	--	300	--	--	300	--	nS
Response Time (note 6) V_{RL}=5V. R_L=5.1KΩ	t_{TLH}	--	1.3	--	--	1.5	--	uS
Output Sink Current V_{IN}(-)=1V, V_{IN}(+)=0V, Vo≤1.5V	I_{SINK}	6.0	16	--	6.0	16	--	mA
Output Saturation Voltage V_{IN}(-)=1V, V_{IN}(+)=0V, I_{SINK}≤4mA	V_{OL}	--	250	400	--	250	400	mV
Output Leakage Current V_{IN}(-)=0V, V_{IN}(+)=1V, Vo=5V	I_{OL}	--	0.1	--	--	0.1	--	nA
Supply Current R_L = ∞, V_{CC} =5V R_L = ∞, V_{CC} =36V	Icc	-- --	0.4 1.0	1.0 2.5	-- --	0.4 1.0	1.0 2.5	mA

Note 1. The max. Output current may be as high as 20mA, independent of the magnitude of V_{CC}, output short circuits to V_{CC} can cause excessive heating and eventual destruction.

Note 2. This magnitude of input current will only occur if the input leads are driven more negative than ground or the negative supply voltage. This is due to the input PNP collector base junction becoming forward biased acting as an input clamp diode. There is also a lateral PNP parasitic transistor action on the IC chip. This phenomena can cause the output voltage of the comparators to go to the V_{CC} voltage level (or ground if overdrive is large) during the time the input is driven negative. This will not destroy the device and normal output states will recover when the inputs become -0.3V of ground or negative supply.

Note 3. At output switch point, V_O=1.4Vdc, R_S=0Ω with V_{CC} from 5Vdc to 30Vdc, and over the full input common-mode

Note 4. Due to the PNP transistor inputs, bias current will flow out of the inputs, this current is essentially constant independent of the output state, therefore, no loading changes will exist on the input lines.

Note 5. Input common mode of either input should not be permitted to go more than 0.3V negative of ground or minus supply. The upper limit of common mode range is V_{CC} - 1.5V but either or both inputs can betaken to as high as 30volts without damage.

Note 6. Response time is specified with a 100mV step and 5.0mV of overdrive. With larger magnitudes of overdrive faster response times are obtainable.

Electrical Characteristics Curve

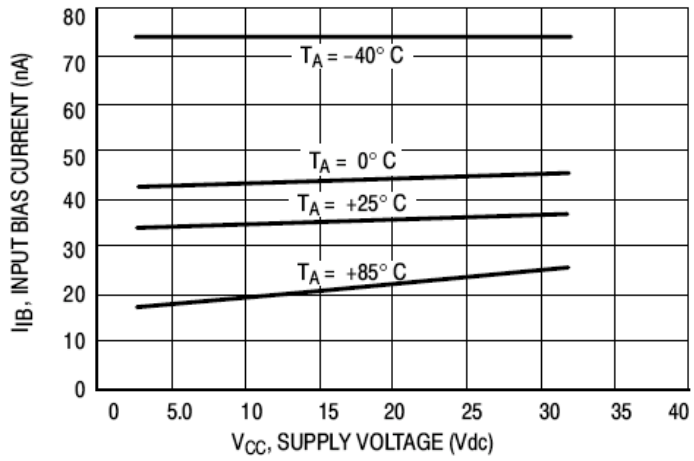


Figure 1. Input Bias Current vs. Power Supply Voltage

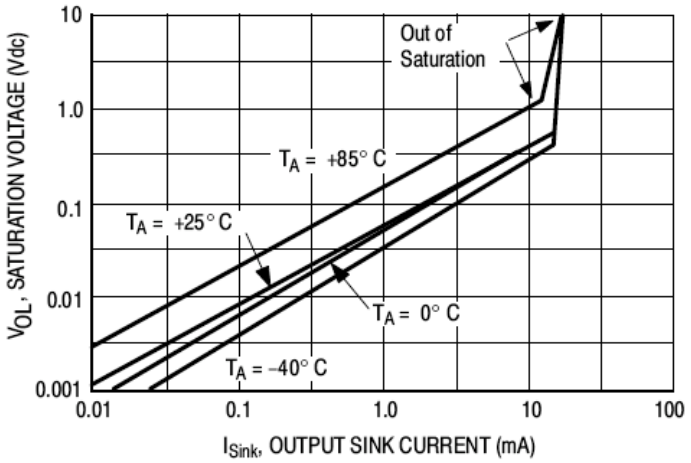


Figure 2. Output Saturation Voltage vs. Output Sink Current

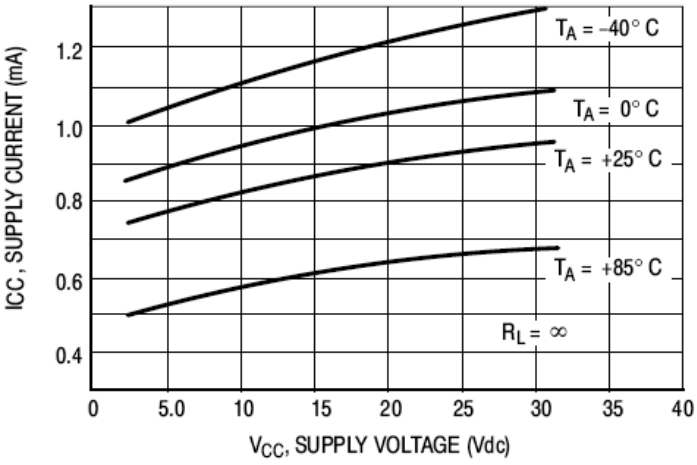


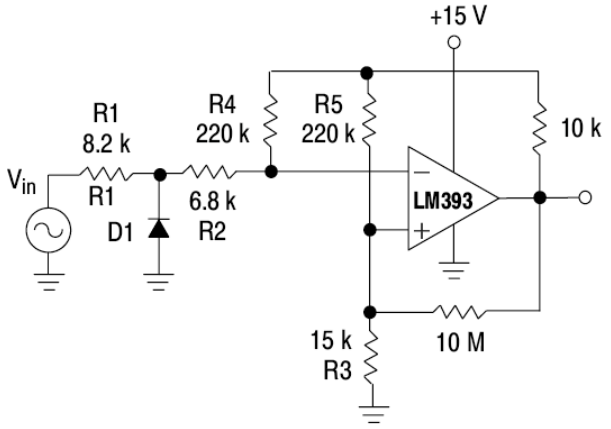
Figure 3. Power Supply Current vs. Power Supply Voltage

Application information

This dual comparator feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitive coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors<10KΩ should be used. The addition of positive feedback (<10 mV) is also recommended.

It is good design practice to ground all unused pins. Differential input voltages may be larger than supply voltage without damaging the comparator's inputs. Voltages more negative than -0.3V should not be used.

Application information (Continued)

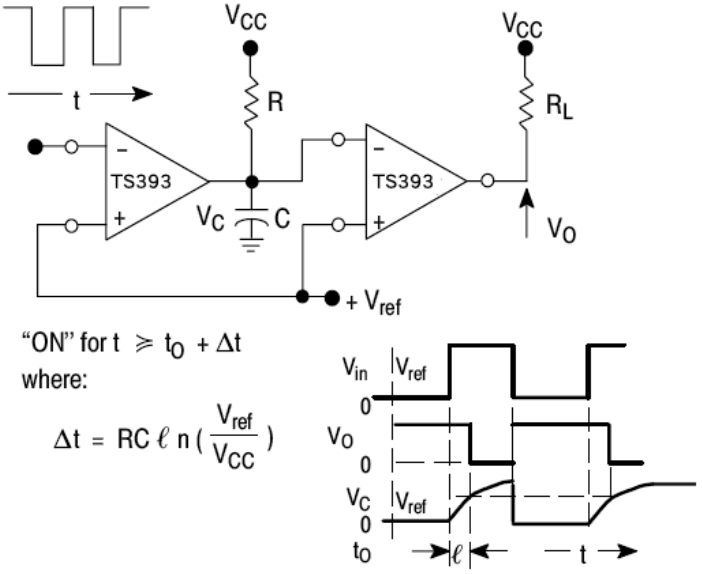


D1 prevents input from going negative by more than 0.6 V.

$$R1 + R2 = R3$$

$$R3 \leq \frac{R5}{10}$$ for small error in zero crossing.

Figure 4. Zero Crossing Detector (Single Supply)

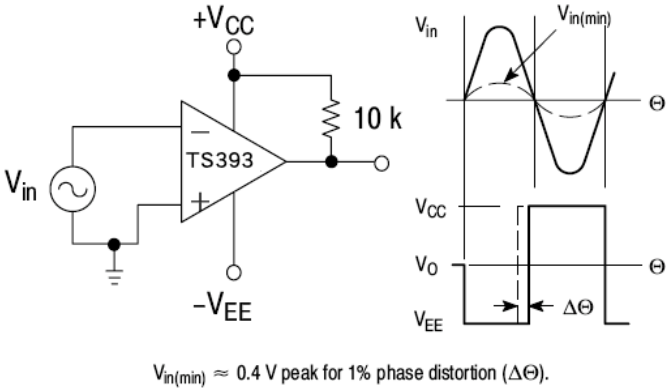


"ON" for $t \geq t_O + \Delta t$

where:

$$\Delta t = RC\,\ell n\left(\frac{V_{ref}}{V_{CC}}\right)$$

Figure 5. Zero Crossing Detector (Single Supply)



$V_{in(min)} \approx 0.4$ V peak for 1% phase distortion ($\Delta\Theta$).

Figure 6. Time Delay Generator

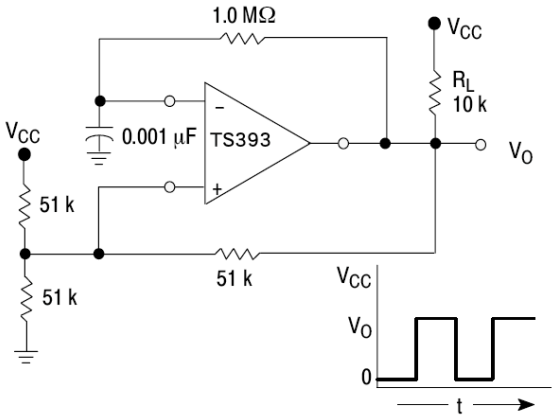
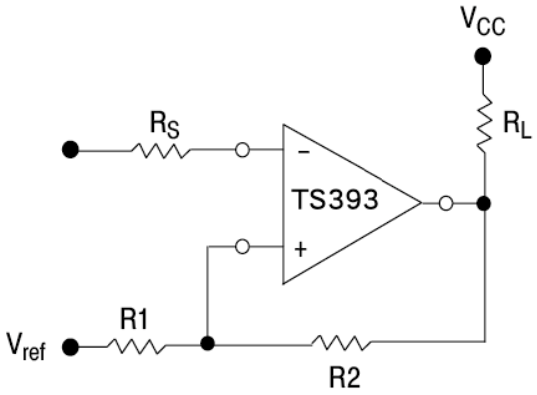


Figure 7. Free-Running Square-Wave Oscillator



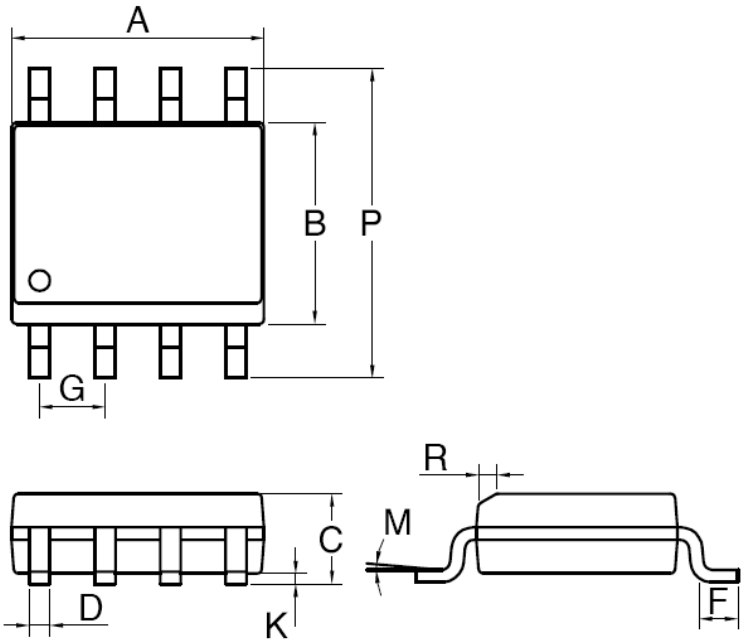
$$R_S = R1 \,||\, R2$$

$$V_{th1} = V_{ref} + \frac{(V_{CC} - V_{ref})\ R1}{R1 + R2 + R_L}$$

$$V_{th2} = V_{ref} - \frac{(V_{ref} - V_O\ Low)\ R1}{R1 + R2}$$

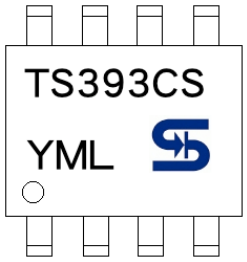
Figure 8. Comparator with Hysteresis

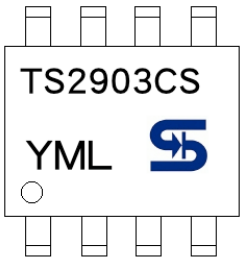
SOP-8 Mechanical Drawing



SOP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX.
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27BSC		0.05BSC	
K	0.10	0.25	0.004	0.009
M	0º	7º	0º	7º
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

Marking Diagram





Y = Year Code
M = Month Code
(**A**=Jan, **B**=Feb, **C**=Mar, **D**=Apl, **E**=May, **F**=Jun, **G**=Jul, **H**=Aug, **I**=Sep, **J**=Oct, **K**=Nov, **L**=Dec)
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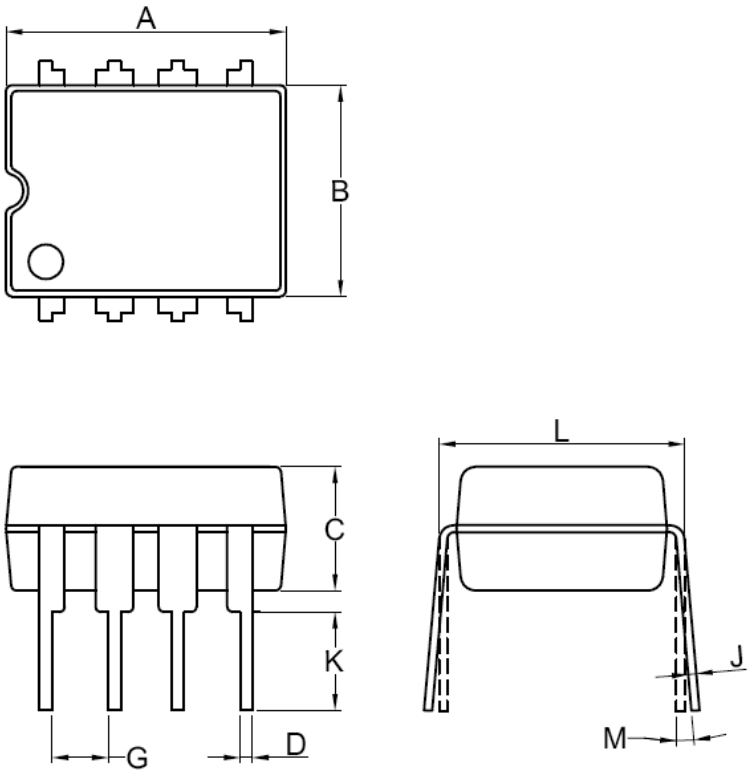
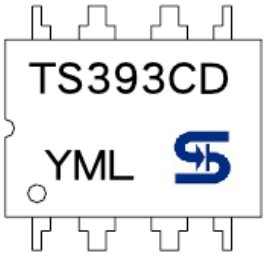
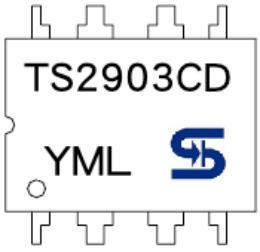
DIP-8 Mechanical Drawing



DIP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.07	9.32	0.357	0.367
B	6.22	6.48	0.245	0.255
C	3.18	4.45	0.125	0.135
D	0.35	0.55	0.019	0.020
G	2.54 (typ)		0.10 (typ)	
J	0.29	0.31	0.011	0.012
K	3.25	3.35	0.128	0.132
L	7.75	8.00	0.305	0.315
M	-	10^{o}	-	10^{o}

Marking Diagram





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