

TS256MRMMC

256MB RS-MMC

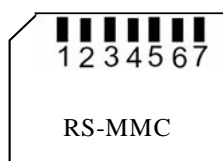
Description

TS256MRMMC is a 256MB Reduced-Size MultiMediaCard (RS-MMC). It's a highly integrated with flash memory, and is accessed via a dedicated serial interface optimized for fast and reliable data transmission. TS256MRMMC is designed to provide an inexpensive, mechanically robust storage medium in card form for multimedia consumer applications and mobile devices (handheld PCs, digital cameras, MP3 players, etc.) to store, copy, and move information like a small hard drive.

Placement



Front



Back

Features

- Storage Capacity: 256MB
- Operating Voltage: 2.7 ~ 3.6V
- Operating Temperature: -25°C ~ 85°C
- Data Transfer Rate(Maximum):
Read:2MB/sec,Write:2MB/sec
- Fully compatible with MultiMediaCard system specification version 3.31
- Embedded data error correction
- Low power consumption
- Form Factor: 24mm x 18mm x 1.4mm

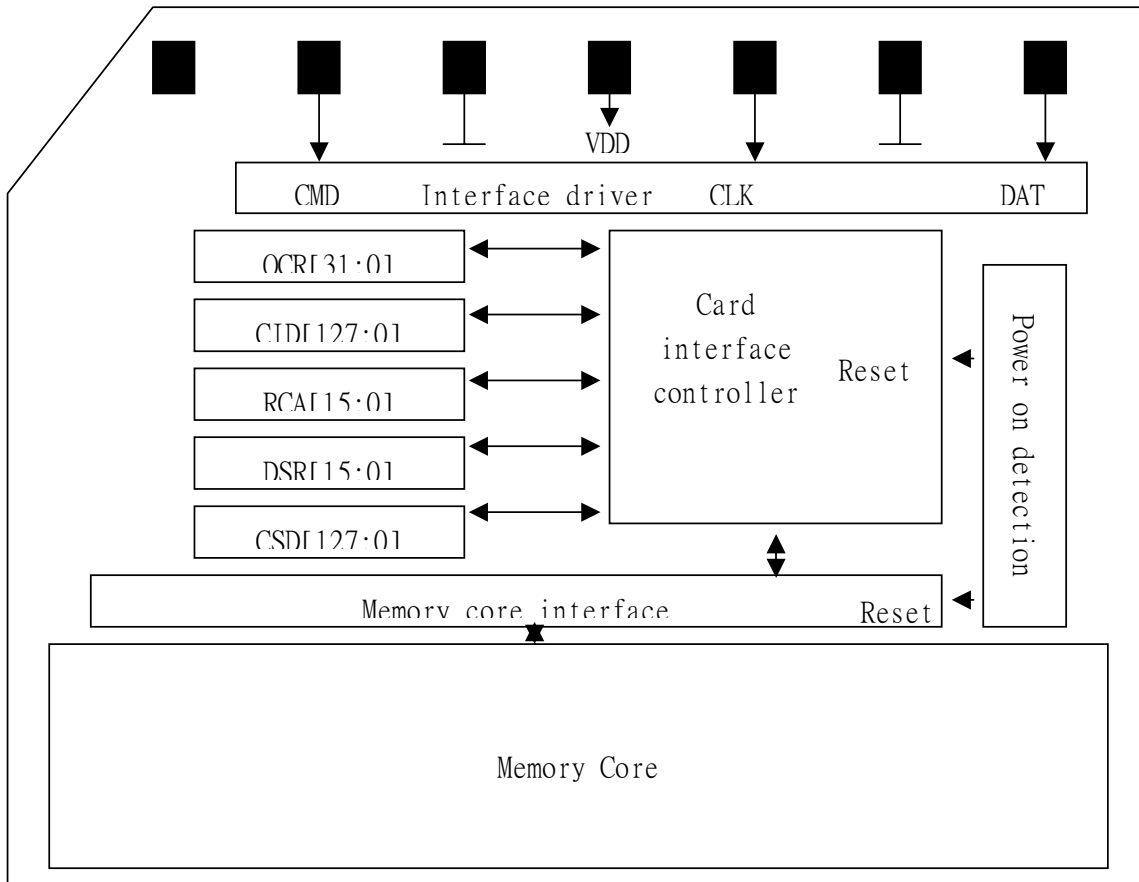
Pin Definition

Pin No.	MMC Mode			SPI Mode		
	Name	Type	Description	Name	Type	Description
1	RSV	NC	Reserved	CS	I	Chip select
2	CMD	I/O/PP/OD	Command/Response	DI	I/PP	Data in
3	VSS1	S	Ground	VSS	S	GND
4	VCC	S	Power supply	VDD	S	VCC
5	CLK	I	Clock	SCLK	I	Clock
6	VSS2	S	Ground	VSS2	S	GND
7	DAT	I/O/PP	Data	DO	O/PP	Data out

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Architecture



Temperature Characteristics

Parameter	Min	Max	Unit
Storage temperature	-40	85	°C
Operating temperature	-25	85	°C
Junction temperature	-20	95	°C

Electrical Characteristics

• General

Parameter	Min	Max	Unit
Peak Voltage on all lines	-0.5	3.6	V
All Inputs			
Input Leakage Current	-10	10	uA
All Outputs			
Output Leakage Current	-10	10	uA

• Power Supply Voltage

Parameter	Symbol	Min.	Max.	Unit	Remark
Supply Voltage (low voltage range)	V _{DDL}	1.65	1.95	V	1.95V – 2.7V is not supported
Supply Voltage (high voltage range)	V _{DDH}	2.7	3.6	V	
Supply Voltage Differentials (Vss1, Vss2)		-0.5	0.5	V	

• Bus Signal Line Load

The total capacitance C_L of each line of the MultiMediaCard bus is the sum of the bus master capacitance C_{HOST} , the bus capacitance C_{BUS} itself and the capacitance C_{CARD} of each card connected to this line:

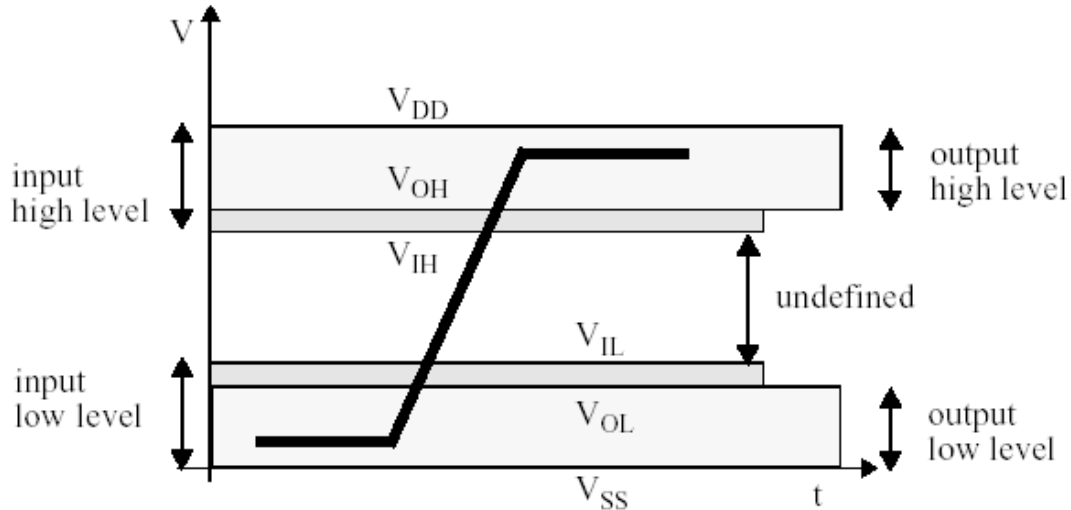
$$C_L = C_{HOST} + C_{BUS} + N \cdot C_{CARD}$$

where N is the number of connected cards. Requiring the sum of the host and bus capacitance's not to exceed 30 pF for up to 10 cards, and 40 pF for up to 30 cards, the following values must not be exceeded:

Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance for CMD	R _{CMD}	4.7	100	kΩ	To prevent bus floating
Pull-up resistance for DAT	R _{DAT}	50	100	kΩ	To prevent bus floating
Bus signal line capacitance	C _L	—	250	pF	fpp ≤ 5 MHz, 30 cards
Bus signal line capacitance	C _L	—	100	pF	fpp ≤ 20 MHz, 10 cards
Single card capacitance	C _{CARD}	—	7	pF	
Maximum signal line inductance		—	16	nH	fpp ≤ 20 MHz

• Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.



• Open-Drain Mode Bus Signal Level

Parameter	Symbol	Min.	Max.	Unit	Conditions
Output HIGH Voltage	V_{OH}	$V_{DD}-0.2$		V	$I_{OH} = -100\mu A$
Output LOW Voltage	V_{OL}		0.3	V	$I_{OH} = 2mA$

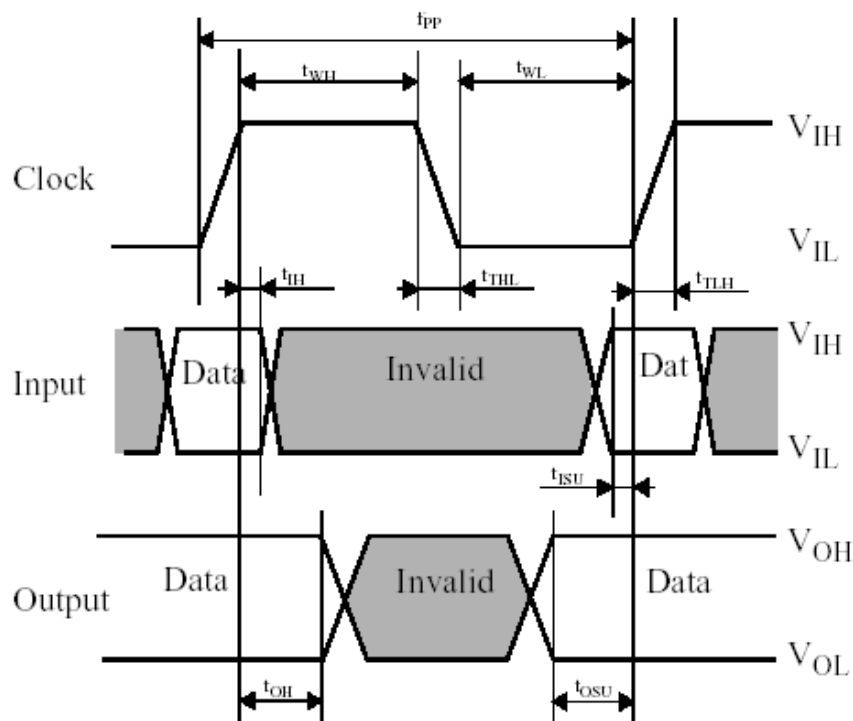
The input levels are identical with the push-pull mode bus signal levels.

• Push-Pull Mode Bus Signal Level

To meet the requirements of the JEDEC specification JESD8-1A, the card input and output voltages shall be within the following specified ranges for any V_{DD} of the allowed voltage range:

Parameter	Symbol	Min.	Max.	Unit	Conditions
Output HIGH Voltage	V_{OH}	$0.75 \cdot V_{DD}$		V	$I_{OH} = -100\mu A @ V_{DD}(\text{Min})$
Output LOW Voltage	V_{OL}		$0.125 \cdot V_{DD}$	V	$I_{OL} = -100\mu A @ V_{DD}(\text{Min})$
Input HIGH Voltage	V_{IH}	$0.625 \cdot V_{DD}$	$V_{DD} + 0.3$	V	
Input LOW Voltage	V_{IL}	$V_{SS} - 0.3$	$0.25 \cdot V_{DD}$	V	

• Bus Timing



Data must be always be sampled on the rising edge of the clock.

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK(All values are referred to $\min(V_{IH})$ and $\max(V_{IL})$)					
Clock frequency data transfer mode(PP)10 cards	f_{PP}	0	20	MHz	$C_L \leq 100\text{pF}$ (10 cards)
Clock frequency data transfer mode(PP)30 cards	f_{PP}	0	5	MHz	$C_L \leq 250\text{pF}$ (30 cards)
Clock frequency identification mode(OD)	f_{OD}	0	400	kHz	
Clock low time	t_{WL}	10		ns	$C_L \leq 100\text{pF}$ (10 cards)
Clock high time	t_{WH}	10		ns	$C_L \leq 100\text{pF}$ (10 cards)
Clock rise time	t_{TLH}		10	ns	$C_L \leq 100\text{pF}$ (10 cards)
Clock fall time	t_{THL}		10	ns	$C_L \leq 100\text{pF}$ (10 cards)
Clock low time	t_{WL}	50		ns	$C_L \leq 250\text{pF}$ (30 cards)
Clock high time	t_{WH}	50		ns	$C_L \leq 250\text{pF}$ (30 cards)
Clock rise time	t_{TLH}		50	ns	$C_L \leq 250\text{pF}$ (30 cards)
Clock fall time	t_{THL}		50	ns	$C_L \leq 250\text{pF}$ (30 cards)

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Parameter	Symbol	Min.	Max.	Unit	Remark
Inputs CMD, DAT(referenced to CLK)					
Input setup time	t_{ISU}	3		ns	
Input hold time	t_{IH}	3		ns	
Outputs CMD, DAT(referenced to CLK)					
Output setup time	t_{OSU}	5		ns	
Output hold time	t_{OH}	5		ns	

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Reliability and Durability

Temperature	Operation: -25°C / 85°C Storage: -40°C (168h) / 85°C (500h) Junction temperature: max. 95°C
Moisture and corrosion	Operation: 25°C / 95% rel. humidity Stress: 40°C / 93% rel. hum./500h Salt Water Spray: 3% NaCl/35C; 24h acc. MIL STD Method 1009
ESD protection	Contact Pads: +/-4kV, Human body model according to ANSI EOS/ESD-S5.1-1998 Non Contact Pads area: +/-8kV(coupling plane discharge) +/-15kV(air discharge) Human body model according to IEC61000-4-2
Durability	10.000 mating cycles; test procedure: t.b.d.
Bending	t.b.d.
Torque	t.b.d.
Drop test	1.5m free fall
UV light exposure	UV: 200nm, 15Ws/cm ² according to ISO 7816-1
Visual inspection Shape and form	No warp page; no mold skin; complete form; no cavities surface smoothness sigma -0.1 mm/cm ² within contour; no cracks; no pollution (fat, oil dust, etc.)
Minimum moving force of WP witch	40gf (Ensures that the WP switch will not slide while it is inserted to the connector.)
WP Switch cycles	minimum 1000 Cycles(@Slide force 0.4N to 5N)

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