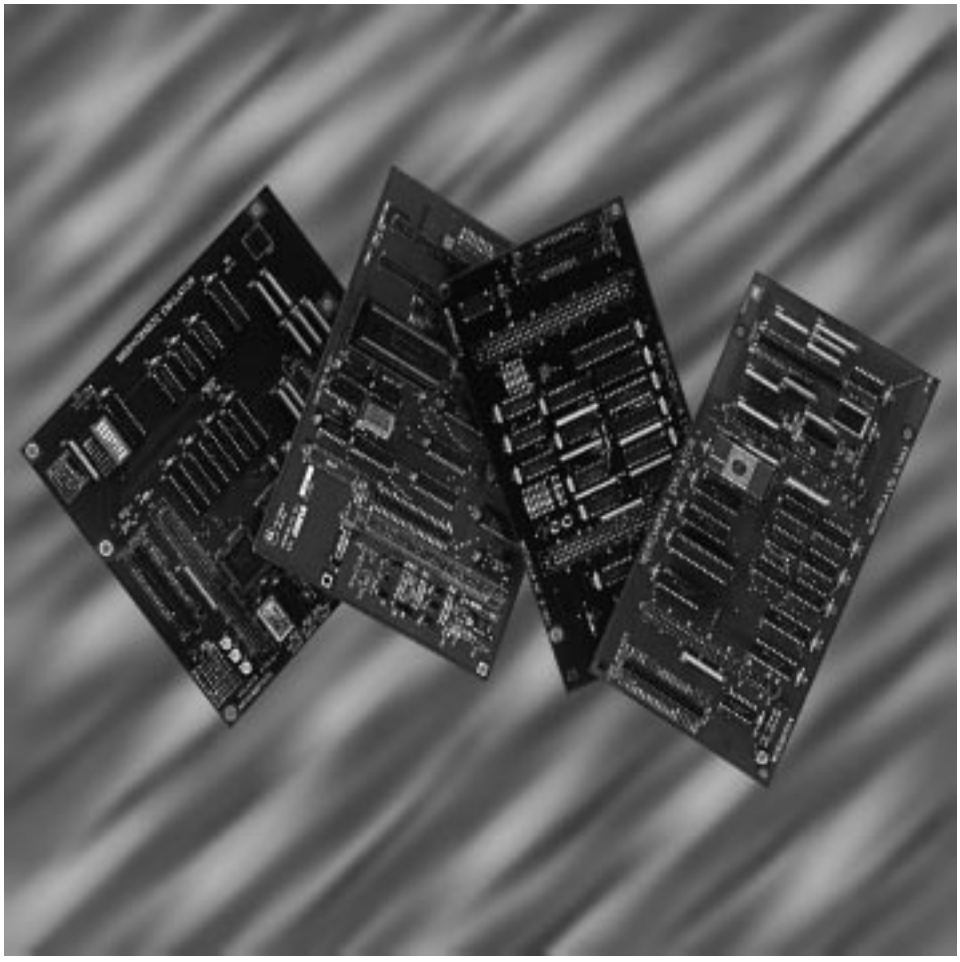
EML08GP32UM/D
REV. 1

M68EML08GP32

EMULATION MODULE
USER'S MANUAL



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Section 1. General Description

1.1 Contents

1.2 Introduction

This user's manual explains connection, configuration, and operation information specific to the M68EML08GP32 emulator module (GP32EM). The GP32EM allows emulations and debugging of target systems based on these microcontroller units (MCUs):

- MC68HC908GP20 (GP20)
- MC68HC908GP32 (GP32)
- MC68HC908JL3 (JL3)

The GP32EM is a low-voltage emulator operating in the range +2.0 to +5.0 Vdc.

This section describes Motorola's two development systems that use the GP32EM, and it explains the GP32EM's layout.

1.3 Development Systems

The GP32EM can be part of two Motorola development systems:

- M68MMDS0508 modular development system (MMDS)
- M68MMEVS0508 evaluation system (MMEVS)

1.3.1 Motorola Modular Development System (MMDS)

The MMDS is an emulator system that provides a bus state analyzer and real-time memory windows. The unit's integrated design environment includes an editor, an assembler, user interface, and source-level debugger.

A complete MMDS consists of:

- Station module — The metal MMDS enclosure containing the control board and the internal power supply
- Emulator module (EM) — A separately purchased printed circuit board that enables system functionality for a specific set of MCUs
- Two logic clip cable assemblies — Twisted-pair cables that connect the station module to the target system, a test fixture, a clock, an oscillator, or any other circuitry useful for evaluation or analysis. One end of each cable assembly has a molded connector, which fits into station-module pod A or pod B. Leads at the other end of each cable terminate in female probe tips. Ball clips come with the cable assemblies.
- 9-lead RS-232 serial cable — Cable that connects the station module to the host computer RS-232 port
- 9- to 25-pin adapter — A molded assembly that connects the 9-pin cable to a 25-pin serial port
- System software — Software on 3-1/2 inch diskettes
- MMDS documentation — *MMDS Operations Manual*, Motorola document order number MMDS0508OM/D; a system software manual, included with the P&E Microcomputer System, Inc.’s MMDS0508 software package; and the appropriate emulator user's manual

MMDS baud rates are selected by the user at 2400, 4800, 9600, 19,200, 38,400, or 57,600.

As mentioned, the GP32EM gives the MMDS the ability to emulate target systems based on MC68HC908GP20, MC68HC908GP32, and MC68HC908JL3 MCUs. By substituting a different EM, MMDS can be enabled to emulate target systems based on a different MCU. (A local Motorola representative can explain all the EMs available.)

1.3.2 Motorola Modular Evaluation System (MMEVS)

An MMEVS is an economical, two-board tool for designing, debugging, and evaluating target systems based on MC68HC05 or MC68HC08 MCUs.

A complete MMEVS consists of:

- Platform board (PFB) — The bottom board, which supports the emulator module; has connectors for power and for a terminal or host computer
- Emulator module (EM) — A separately purchased printed circuit board that enables system functionality for a specific set of MCUs; fits onto the PFB
- RS-232 serial cable — A separately purchased cable that connects the PFB to the host computer RS-232 port
- System software — Software on 3-1/2 inch diskettes
- MMEVS documentation — *MMEVS Operations Manual*, Motorola document order number MMEVSOM/D, and the appropriate emulator user's manual

An MMEVS features automatic selection of the communication baud rate from these choices: 2400, 4800, 9600, 19,200, 38,400, or 57,600.

With a GP32EM, the MMEVS emulates target systems based on MC68HC908GP20, MC68HC908GP32, and MC68HC908JL3 MCUs. By substituting a different EM, the MMEVS can be enabled to emulate target systems based on a different MCU. (A local Motorola representative can explain all the EMs available.)

Section 2. Configuration and Operation explains how to configure and use the GP32EM as part of an MMDS or MMEVS system.

1.4 EM Layout

Figure 1-1 shows the layout of the GP32EM.

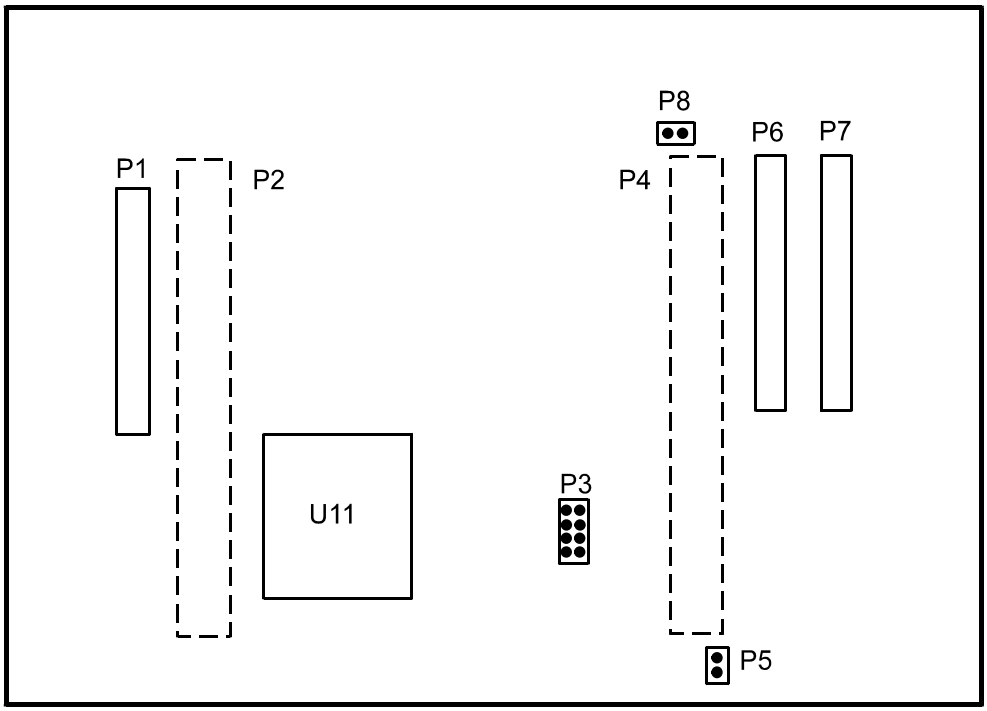


Figure 1-1. M68EML08GP32 Emulator Module

The main elements of the GP32EM are:

- Connector P1 — Permits connection to a logic analyzer
- DIN connectors P2 and P4 — Connect the EM to the MMDS control board or the MMEVS platform board
- Jumper header P3 — Selects the MCU clock source
- Connector P5 — For factory use only
- Connectors P6 and P7 — Customer-specific interfaces to the target system
- Connector P8 — To connect a 20-kΩ pullup resister between V_{DDAD} to V_{DD}

The GP32EM requires these user-supplied cables for connection to other components of a development system:

- An 80-lead target cable and target head adapter to connect the target system to connectors P6 and P7

1.5 Specifications

Table 1-1 lists GP32EM specifications.

Table 1-1. M68EML08GP32 Specifications

Characteristics	Specifications
MCU extension I/O ports	HCMOS compatible
Operating temperature	0° to +40°C
Storage temperature	–40° to +85°C
Relative humidity	0 to 90%, non-condensing
Power requirements	+5 Vdc and +12 Vdc (charge pump), provided from the MMDS control board or MMEVS platform board
Dimensions	8 x 6.5 inches; 230 x 165 mm
Weight	10.4 ounces; 295 g

General Description

Section 2. Configuration and Operation

2.1 Contents

2.2 Introduction

This section explains configuration and operation of the M68EML08GP32 (GP32EM) when it is installed in an MMDS (Motorola modular development system) or MMEVS (Motorola modular evaluation system). For other parts of system installation or configuration, see the MMDS or MMEVS hardware manuals.

NOTE: *A GP32EM already installed in an MMDS station module can be reconfigured. To do so, switch off station-module power, then follow the guidance in this section. Similarly, GP32EM that is already installed on the MMEVS platform board can be reconfigured, provided that platform-board power is disconnected.*

CAUTION: *Be sure to switch off or disconnect power when reconfiguring an installed EM. Reconfiguring EM jumper headers with the power on can damage system circuits.*

ESD CAUTION: *Ordinary amounts of static electricity from clothing or the work environment can damage or degrade electronic devices and equipment. For example, the electronic components installed on printed circuit boards are extremely sensitive to electrostatic discharge (ESD). Wear a ground wrist strap whenever handling any printed circuit board. This strap provides a conductive path for safely discharging static electricity to ground.*

2.3 System Limitations

To use the ADC (analog-to-digital converter) when emulating JL3, bit 4 of ADICLK at address $3E must be set. It is cleared out of reset. Otherwise, the ADC will run on a clock four times faster.

2.4 Setting Jumper Headers

The GP32EM has two jumper headers. **Table 2-1** contains a summary of settings for these headers. **2.4.1 Clock Source Header (P3)** and **2.4.2 Factory Test Select Header (P5)** give additional information about each jumper header.

Table 2-1. Jumper Headers

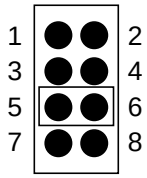
Jumper Header	Type	Description
P3		Jumper between pins 1 and 2; selects an external clock source for the MCU EXTAL input signal from target head connectors Jumper between pins 3 and 4; selects the onboard 32.768-kHz crystal oscillator Jumper between pins 5 and 6 (factory default); selects the clock signal from the MMDS control board or MMEVS platform board Jumper between pins 7 and 8; selects an on-board 32 MHz clock signal
P5		Factory use only; should be left open

Table 2-1. Jumper Headers (Continued)

Jumper Header	Type	Description
P8	1 2 	Jumper installed (factory default); on-board V_{DD} is selected as the source for V_{DDAD}. No jumper installed; V_{DDAD} is supplied from the target system.

2.4.1 Clock Source Header (P3)

Jumper header P3 in **Figure 2-1** determines the clock signal source. The factory configuration (the fabricated jumper between pins 5 and 6) selects the clock signal from the MMDS control board or MMEVS platform board. You must use the system software to select the appropriate clock frequency.

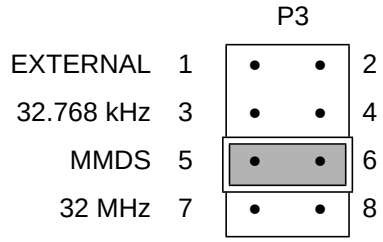


Figure 2-1. Jumper Header P3

Alternately, three other clock signal sources can be selected, as shown in **Figure 2-1**.

- To select the target system as the clock source, install the fabricated jumper between pins 1 and 2. Ensure that the clock source (OSC1) is connected to the EM through the target cable, connector P6 pin 3.
- To select the on-board 32.768-kHz crystal oscillator, install the fabricated jumper between pins 3 and 4.
- To select an on-board 32-MHz clock signal as the clock source, install the fabricated jumper between pins 7 and 8.

NOTE: *Only one jumper should be inserted on jumper header P3 at a time. Inserting multiple jumpers in P3 might damage the GP32EM.*

2.4.2 Factory Test Select Header (P5)

Jumper header P5 is for factory test use only and should be used only by Motorola factory personnel.

If the factory setting is changed, proper operation of the system cannot be guaranteed. **Figure 2-2** shows the default factory jumper header configuration, which has no fabricated jumper installed on jumper header P5 between pins 1 and 2.

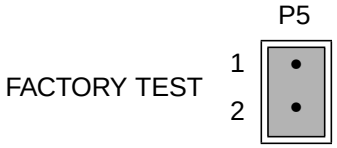


Figure 2-2. Jumper Header P5

2.4.3 Factory Test Select Header (P8)

Use jumper header P8 to select the power source for the MCU internal analog-to-digital (ADC) module

Install a jumper on jumper header P8 (factory default) when V_{DDAD} is not supplied from the target system. This allows use of the ADC module in the MC68HC908GP32 or MC68HC908GP20 MCUs when there is no target system V_{DDAD} power.

Remove the jumper on jumper header P8 when V_{DDAD} is provided by target system and an MC68HC908GP32 or MC68HC908GP20 MCU is being used.

Because V_{DD} and V_{DDAD} are connected internally in the MC68HC08JL3 MCU, the jumper on P8 must be installed when emulating JL3.

Alternately, remo

ve the jumper from P8 and connect an external power supply to P8 pin 1.

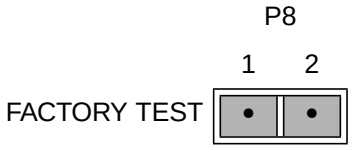


Figure 2-3. Jumper Header P8

2.5 Remaining System Installation

When all jumper headers are configured, follow these steps to complete the GP32EM installation:

- To install the GP32EM in an MMDS station module, remove the entire top half of the station-module enclosure. Fit together EM connectors P1 and P2 (on the bottom of the board) and control-board connectors P1 and P2. Snap the corners of the EM onto the plastic standoffs.
- To install the GP32EM on an MMEVS platform board, fit together EM connectors P1 and P2 (on the bottom of the board) and platform-board connectors P3 and P4. Snap the corners of the EM onto the plastic standoffs.
- Copy the personality files from the provided diskette to the directory that contains the debugging software. The personality files for the GP32EM are:
  - 00455Vxx.MEM — Personality file for MC68HC908GP32 MCU
  - 0GP20Vxx.MEM — Personality file for MC68HC908GP20 MCU
  - 0JL3Vxx.MEM — Personality file for MC68HC908JL3 MCU

At this point, make any system cable connections and restore power. For instructions, consult the MMDS or MMEVS operations manuals.

Configuration and Operation

Section 3. Connector Information

3.1 Contents

3.2 Introduction

This section consists of pin assignments and signal descriptions for M68EML08GP32 target and logic analyzer connectors.

3.3 Logic Analyzer Connector (P1)

Connector P1 is the GP32EM logic analyzer connector.

Figure 3-1 shows the pin assignments for connector P1. **Table 3-1** gives the signal descriptions.

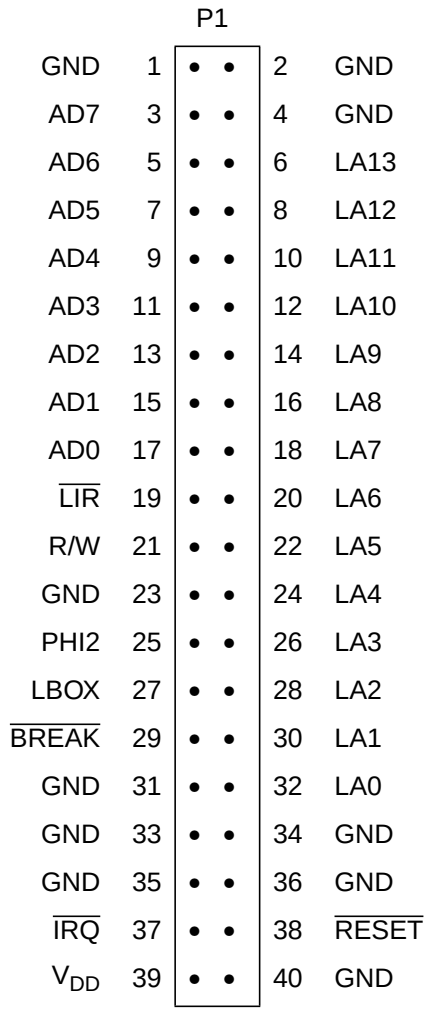


Figure 3-1. Logic Analyzer Connector P1 Pin Assignments

Table 3-1. Logic Analyzer Connector P1 Signal Descriptions

Pin	Mnemonic	Signal
1, 2	GND	GROUND
3	AD7	Data bus bit 7 — MCU bidirectional data bus
4	GND	GROUND
5	AD6	Data bus bit 6 — MCU bidirectional data bus
6	LA13	Address bus bit 13 — MCU output address bus
7	AD5	Data bus bit 5 — MCU bidirectional data bus
8	LA12	Address bus bit 12 — MCU output address bus
9	AD4	Data bus bit 4 — MCU bidirectional data bus
10	LA11	Address bus bit 11 — MCU output address bus
11	AD3	Data bus bit 3 — MCU bidirectional data bus
12	LA10	Address bus bit 10 — MCU output address bus
13	AD2	Data bus bit 2 — MCU bidirectional data bus
14	LA9	Address bus bit 9 — MCU output address bus
15	AD1	Data bus bit 1 — MCU bidirectional data bus
16	LA8	Address bus bit 8 — MCU output address bus
17	AD0	Data bus bit 0 — MCU bidirectional data bus
18	LA7	Address bus bit 7 — MCU output address bus
19	$\overline{\text{LIR}}$	Load instruction register — Active-low output signal, asserted when an instruction starts
20	LA6	Address bus bit 6 — MCU output address bus
21	R/W	Read/Write — Output signal that indicates the direction of data transfer
22	LA5	Address bus bit 5 — MCU output address bus
23	GND	GROUND
24	LA4	Address bus bit 4 — MCU output address bus
25	PHI2	PHI2 clock — Internally generated output clock signal used as a timing reference
26	LA3	Address bus bit 3 — MCU output address bus

Connector Information

Table 3-1. Logic Analyzer Connector P1
Signal Descriptions (Continued)

Pin	Mnemonic	Signal
27	LBOX	Last bus cycle — Input signal that the emulator asserts to indicate that the target system MCU is in the last bus cycle of an instruction
28	LA2	Address bus bit 2 — MCU output address bus
29	$\overline{\text{BREAK}}$	$\overline{\text{BREAK}}$ — Active low signal that the EM asserts to stop the target system MCU from running user code
30	LA1	Address bus bit 1 — MCU output address bus
31	GND	GROUND
32	LA0	Address bus bit 0 — MCU output address bus
38	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ — Active-low bidirectional signal for starting an EVS reset
37	GND	GROUND
39	V_{DD}	+5 Vdc power — Input voltage (+5 Vdc @ 1 A (max)) used by the EM logic circuits
40	GND	GROUND
31	GND	GROUND

3.4 Target Connectors (P6 and P7)

GP32EM has two target connectors: P6 and P7, each a 2-row by-20-pin connector.

Figure 3-1, **Table 3-2**, and **Table 3-3** give the pin assignments and signal descriptions for these connectors.

P6

V_{SS}	1	2	PTC1	
NC	3	4	V_{SS}	
V_{SS}	5	6	PTC4	
PTA7	7	8	RESERVED	
PTA6 (GP32)	9	10	NC	
PTA4	11	12	NC	
PTA2	13	14	NC	
PTA0	15	16	NC	
V_{DDAD}	17	18	NC	
V_{SS}	19	20	NC	
PTA6 (JL3)	21	22	PTB5	
NC	23	24	V_{SS}	
NC	25	26	PTB2	
NC	27	28	PTB0	
NC	29	30	PTD6 (GP32)	
NC	31	32	PTD5	
NC	33	34	V_{DD}	
PTE1	35	36	PTD3	
PTD0	37	38	V_{SS}	
PTD2	39	40	V_{SS}	

P7

$\overline{\text{RESET}}$	1	2	PTC0	
OSC1	3	4	PTC2	
NC	5	6	PTC3	
RESERVED	7	8	PTC5	
V_{SS}	9	10	PTC6	
PTA5	11	12	NC	
PTA3	13	14	V_{SS}	
PTA1	15	16	NC	
V_{SSAD}	17	18	NC	
PTB7	19	20	NC	
NC	21	22	PTB6	
NC	23	24	PTB4	
NC	25	26	PTB3	
V_{SS}	27	28	PTB1	
NC	29	30	PTD7 (GP32)	
PTD6 (JL3)	31	32	V_{SS}	
PTD7 (JL3)	33	34	PTD4	
PTE0	35	36	V_{SS}	
$\overline{\text{IRQ}}$	37	38	V_{SS}	
PTD1	39	40	V_{SS}	

Figure 3-2. Target Connectors P6 and P7 Pin Assignments

Connector Information

Table 3-2. Target Connectors P6 Signal Descriptions

Pin	Mnemonic	Signal
1	V_{SS}	EM GROUND — Ground signal of the EM board
2	PTC1	PORT C (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
3	NC	No connect
4, 5	V_{SS}	EM GROUND — Ground signal of the EM board
6	PTC4	PORT C (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
7	PTA7	PORT A (bit 7) — General-purpose I/O lines controlled by software via data direction and data registers
8	RESERVED	Reserved
9	PTA6 (GP32)	PORT A (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
10	NC	No connect
11	PTA4	PORT A (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
12	NC	No connect
13	PTA2	PORT A (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
14	NC	No connect
15	PTA0	PORT A (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
16	NC	No connect
17	V_{DDAD}	Analog-to-digital input voltage — ADC input voltage. Use the same voltage level as V_{DD}.
18	NC	No connect
19	V_{SS}	EM GROUND — Ground signal of the EM board
20	NC	No connect
21	PTA6 (JL3)	PORT A (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
22	PTB5	PORT B (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers
23	NC	No connect

Table 3-2. Target Connectors P6 Signal Descriptions (Continued)

Pin	Mnemonic	Signal
24	V_{SS}	EM GROUND – Ground signal of the EM board.
25	NC	No connect
26	PTB2	PORT B (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
27	NC	No connect
28	PTB0	PORT B (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
29	NC	No connect
30	PTD6 (GP32)	PORT D (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
31	NC	No connect
32	PTD5	PORT D (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers
33	NC	No connect
34	V_{DD}	MMDS +5 V — Used for factory testing
35	PTE1	PORT E (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
36	PTD3	PORT D (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
37	PTD0	PORT D (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
38	V_{SS}	EM GROUND — Ground signal of the EM board
39	PTD2	PORT D (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
40	V_{SS}	EM GROUND — Ground signal of the EM board

Connector Information

Table 3-3. Target Connectors P7 Signal Descriptions

Pin	Mnemonic	Signal
1	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ — Active-low bidirectional control line that initializes the MCU
2	PTC0	PORT C (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
3	OSC1	OSCILLATOR — Crystal oscillator amplifier input signal
4	PTC2	PORT C (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
5	NC	No connect
6	PTC3	PORT C (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
7	RESERVED	Reserved
8	PTC5	PORT C (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers
9	VSS	EM GROUND — Ground signal of the EM board
10	PTC6	PORT C (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
11	PTA5	PORT A (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers
12	NC	No connect
13	PTA3	PORT A (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
14	V_{SS}	EM GROUND — Ground signal of the EM board
15	PTA1	PORT A (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
16	NC	No connect
17	V_{SSAD}	ANALOG-TO-DIGITAL GROUND — ADC ground
18	NC	No connect
19	PTB7	PORT B (bit 7) — General-purpose I/O lines controlled by software via data direction and data registers
20, 21	NC	No connect
22	PTB6	PORT B (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers

Table 3-3. Target Connectors P7 Signal Descriptions (Continued)

Pin	Mnemonic	Signal
23	NC	No connect
24	PTB4	PORT B (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
25	NC	No connect
26	PTB3	PORT B (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
27	V_{SS}	EM GROUND — Ground signal of the EM board
28	PTB1	PORT B (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
29	NC	No connect
30	PTD7 (GP32)	PORT D (bit 7) — General-purpose I/O lines controlled by software via data direction and data registers
31	PTD6 (JL3)	PORT D (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
32	V_{SS}	EM GROUND — Ground signal of the EM board
33	PTD7 (JL3)	PORT D (bit 7) — General-purpose I/O lines controlled by software via data direction and data registers
34	PTD4 (JL3)	PORT D (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
35	PTE0	PORT E (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
36	V_{SS}	EM GROUND — Ground signal of the EM board
37	$\overline{IRQ}$	INTERRUPT REQUEST — Active-low input line for requesting MCU asynchronous non-maskable interrupt
38	V_{SS}	EM GROUND — Ground signal of the EM board
39	PTD1	PORT D (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
40	V_{SS}	EM GROUND — Ground signal of the EM board

3.5 Target Cable Assembly

To connect the GP32EM to a target system, a separately purchased target cable assembly is needed, plus the appropriate target head and target-head/adapter package.

Figure 3-3 shows how one end of the flex cable plugs into the GP32EM module, and it also shows how the target head connects into the target system.

If the GP32EM is installed in the MMDS station module, run the flex cable through the slit in the station-module enclosure.

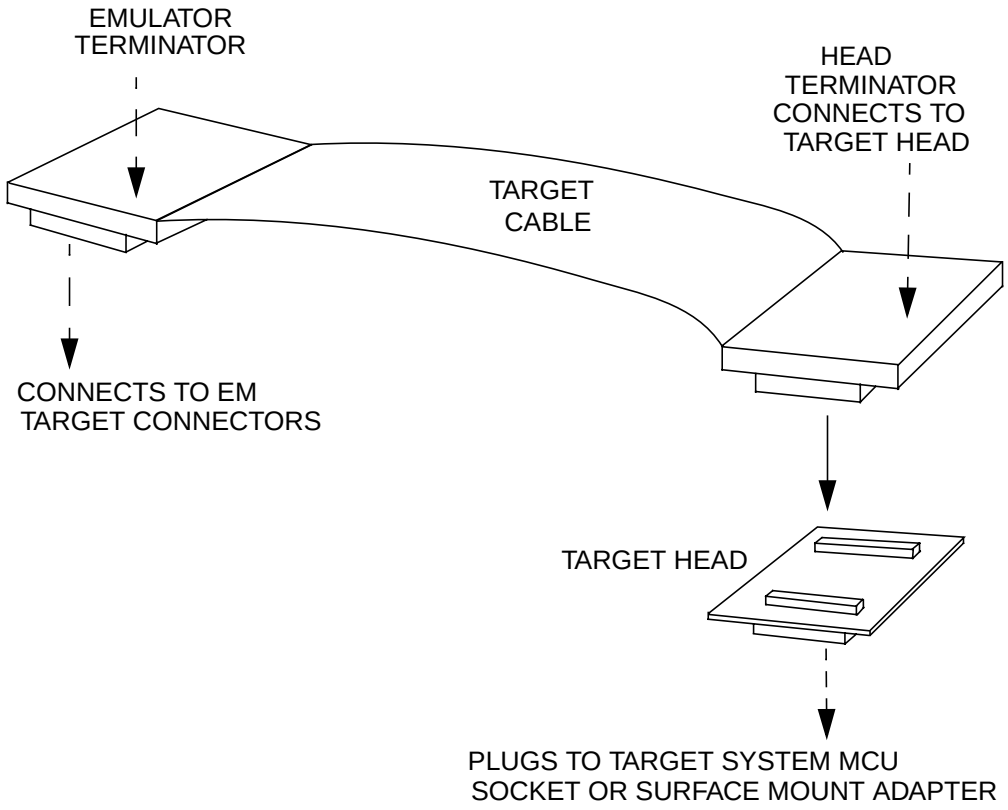
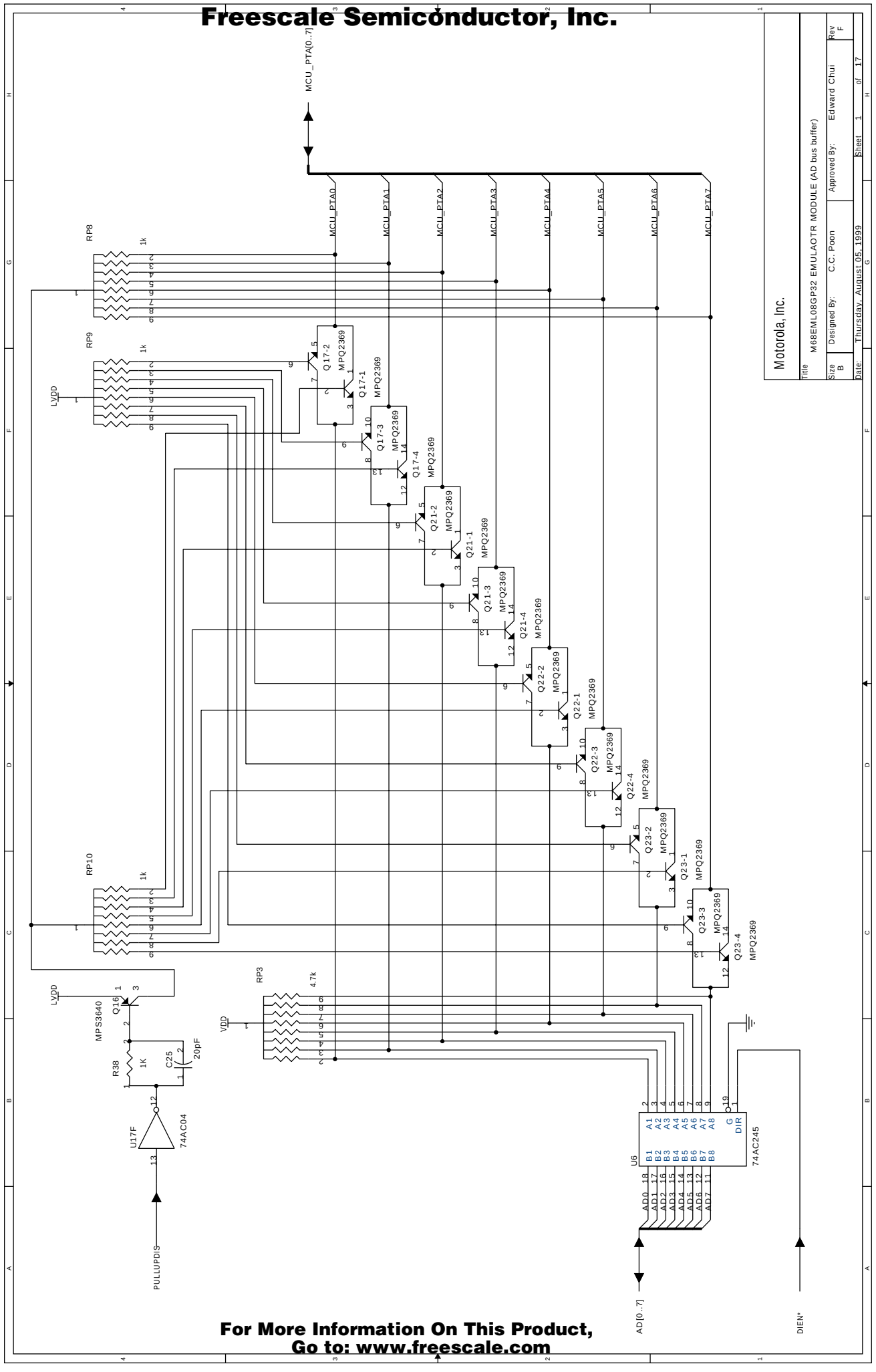


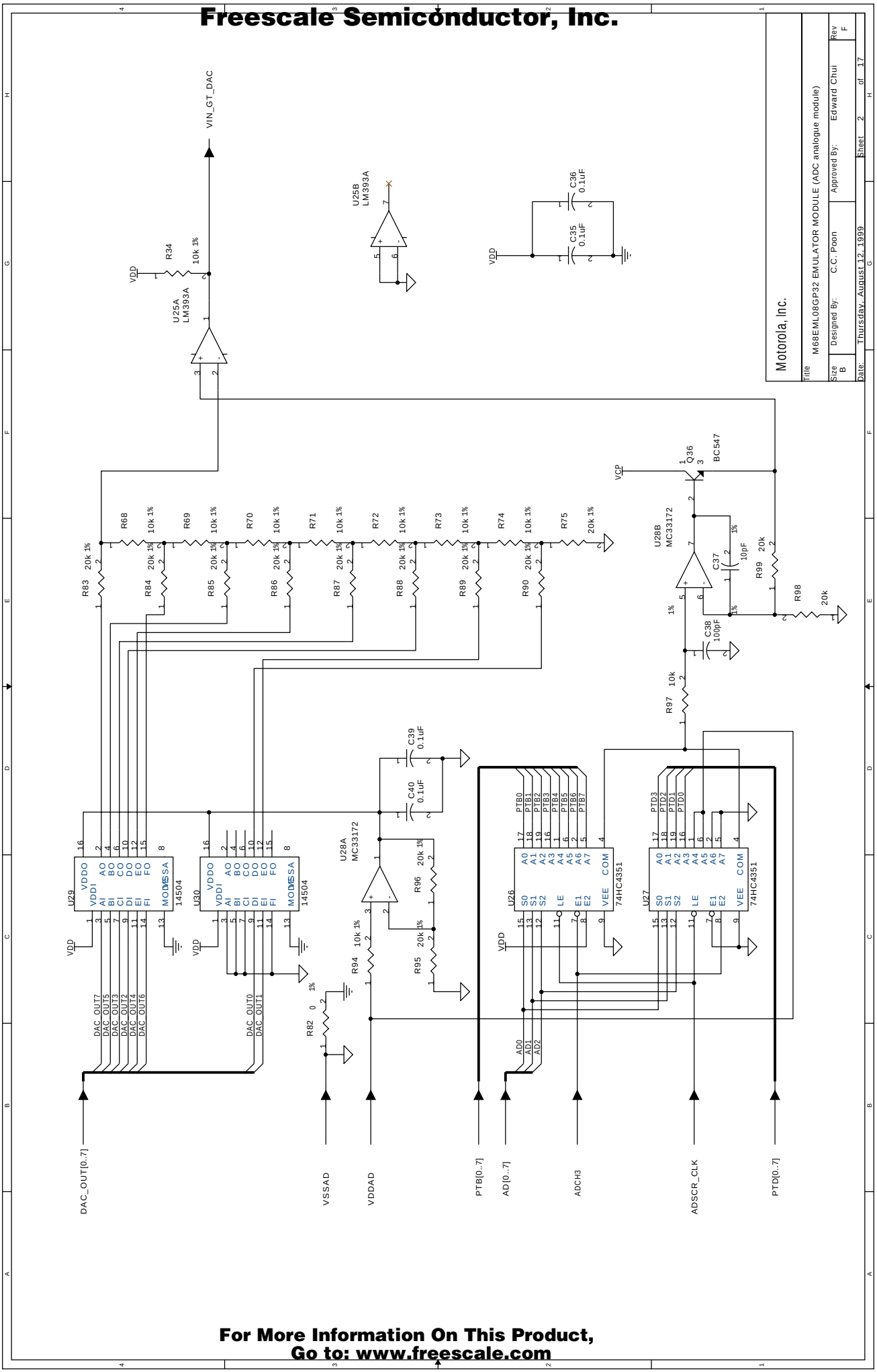
Figure 3-3. Target Cable Assembly

Section 4. Schematics

This chapter contains the M68EML08GP32 emulator module schematic diagrams.

These schematic diagrams are for reference only and may deviate slightly from the circuits on the GP32EM.





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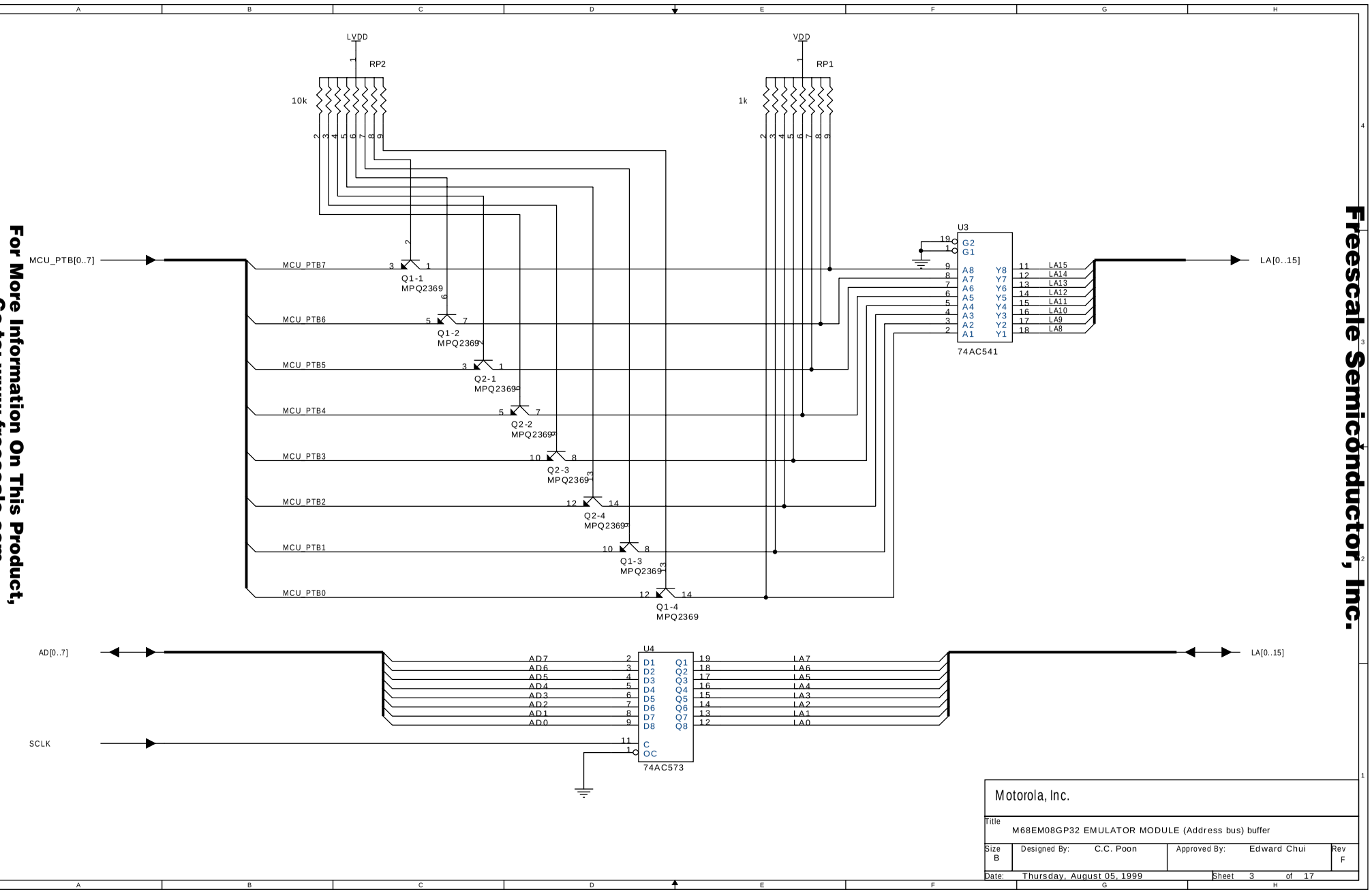
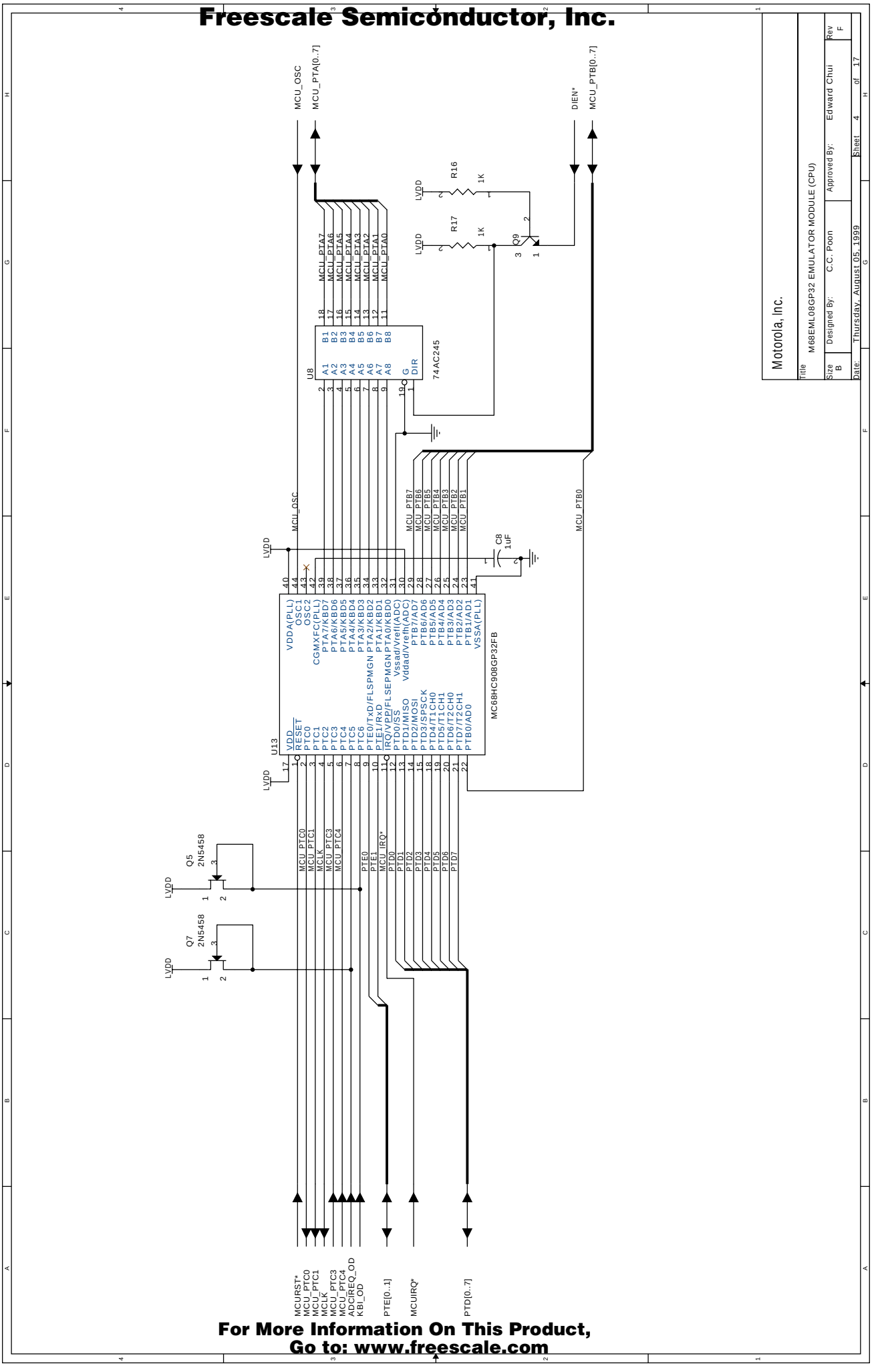
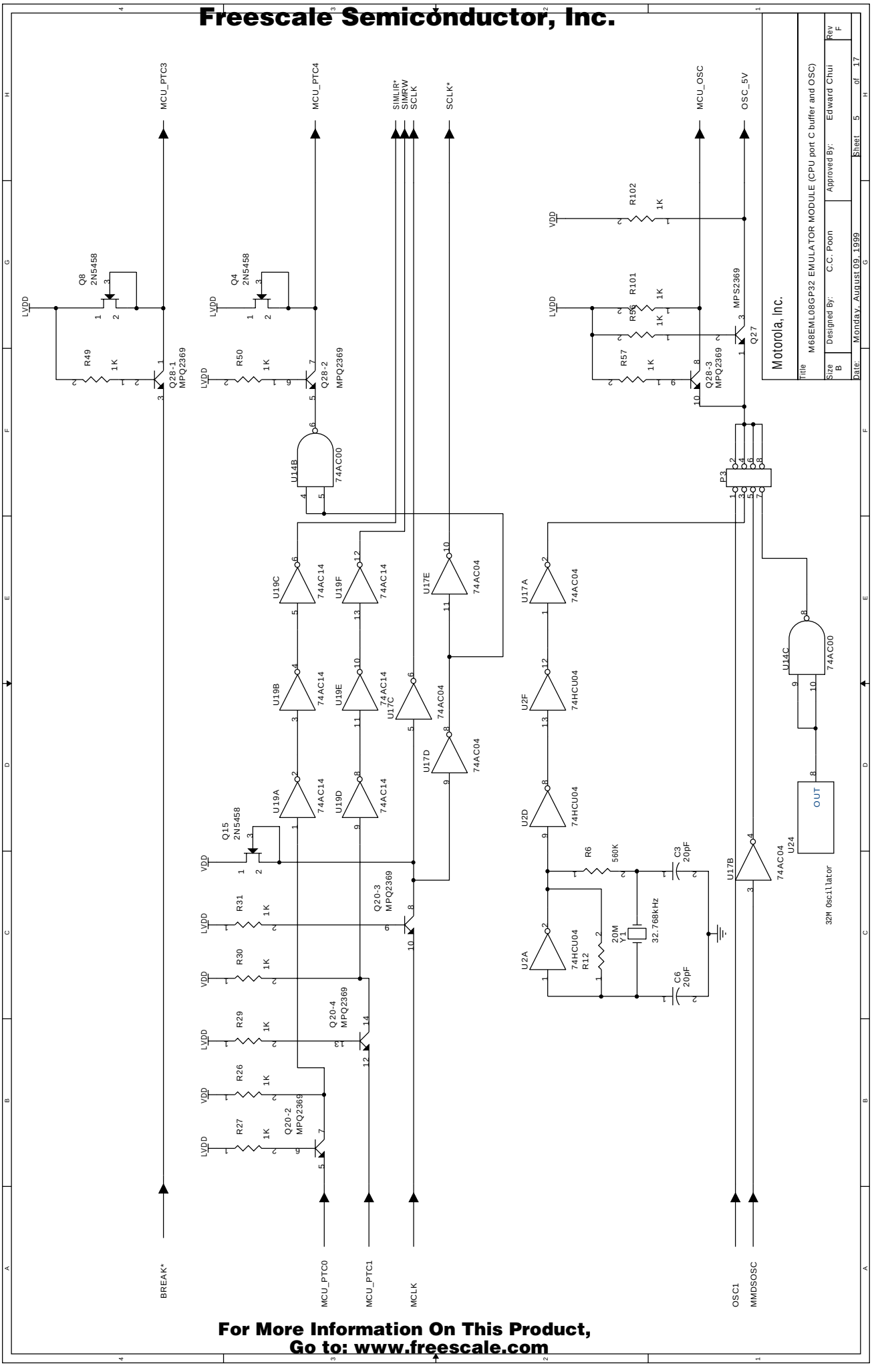
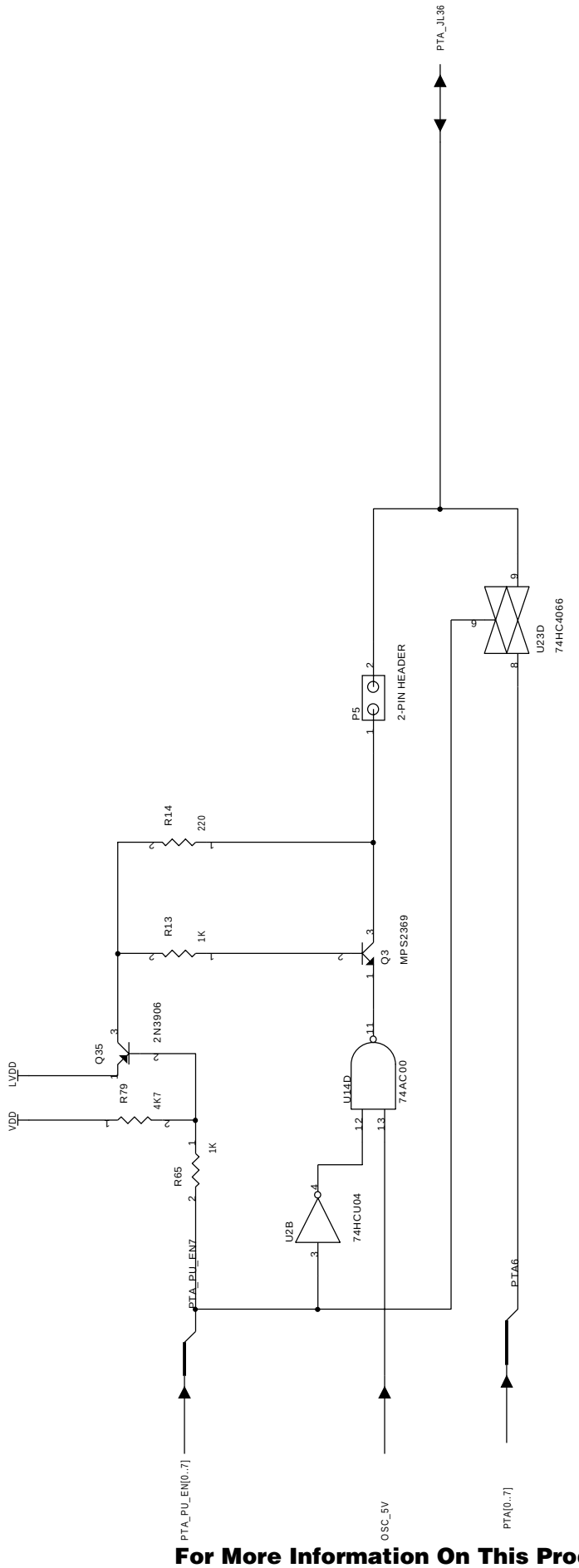


Motorola, Inc.			
Title: M68EM08GP32 EMULATOR MODULE (Address bus) buffer			
Size: B	Designed By: C.C. Poon	Approved By: Edward Chui	Rev: F
Date: Thursday, August 05, 1999	Sheet 3 of 17		





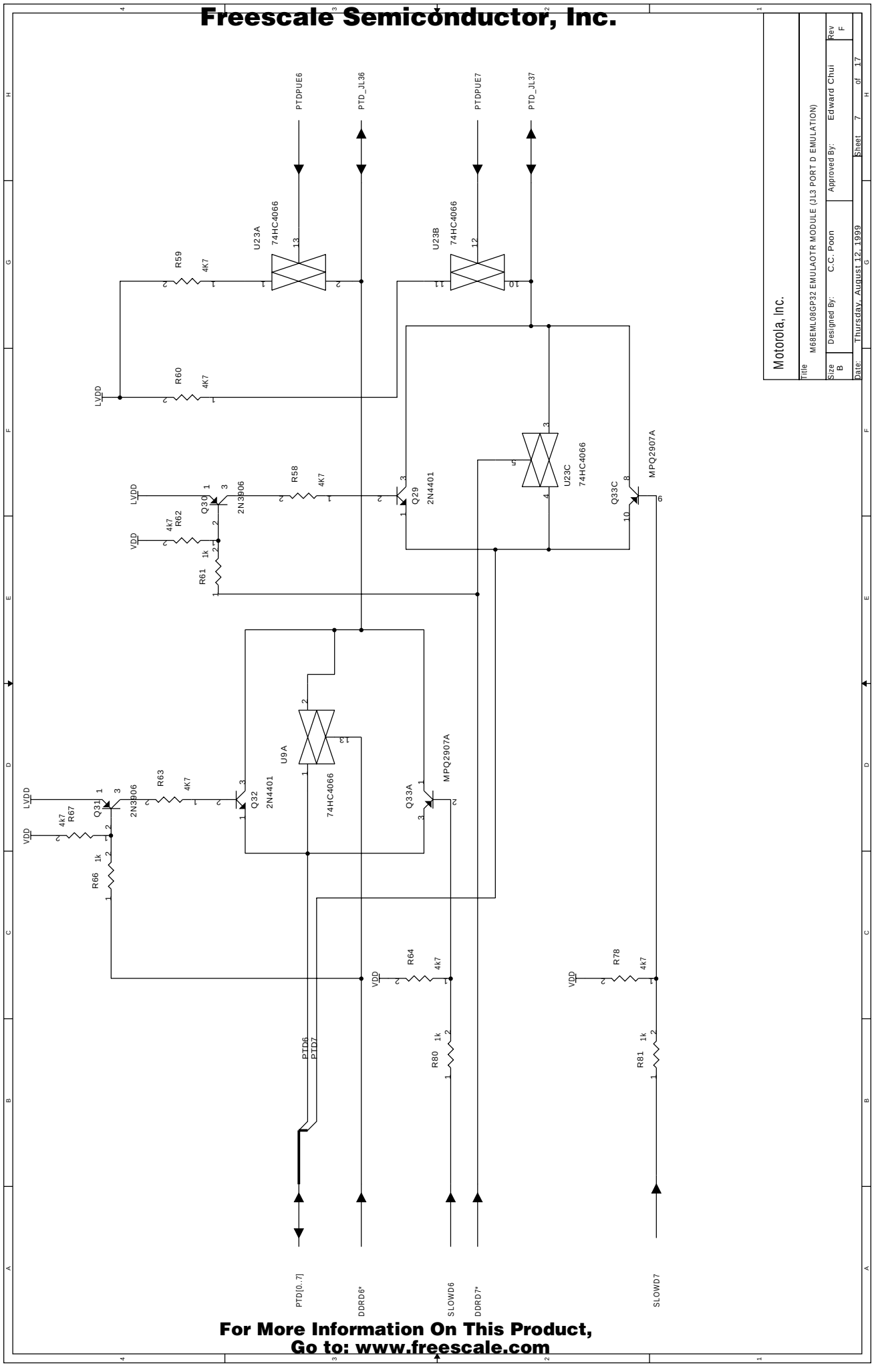


Motorola, Inc.

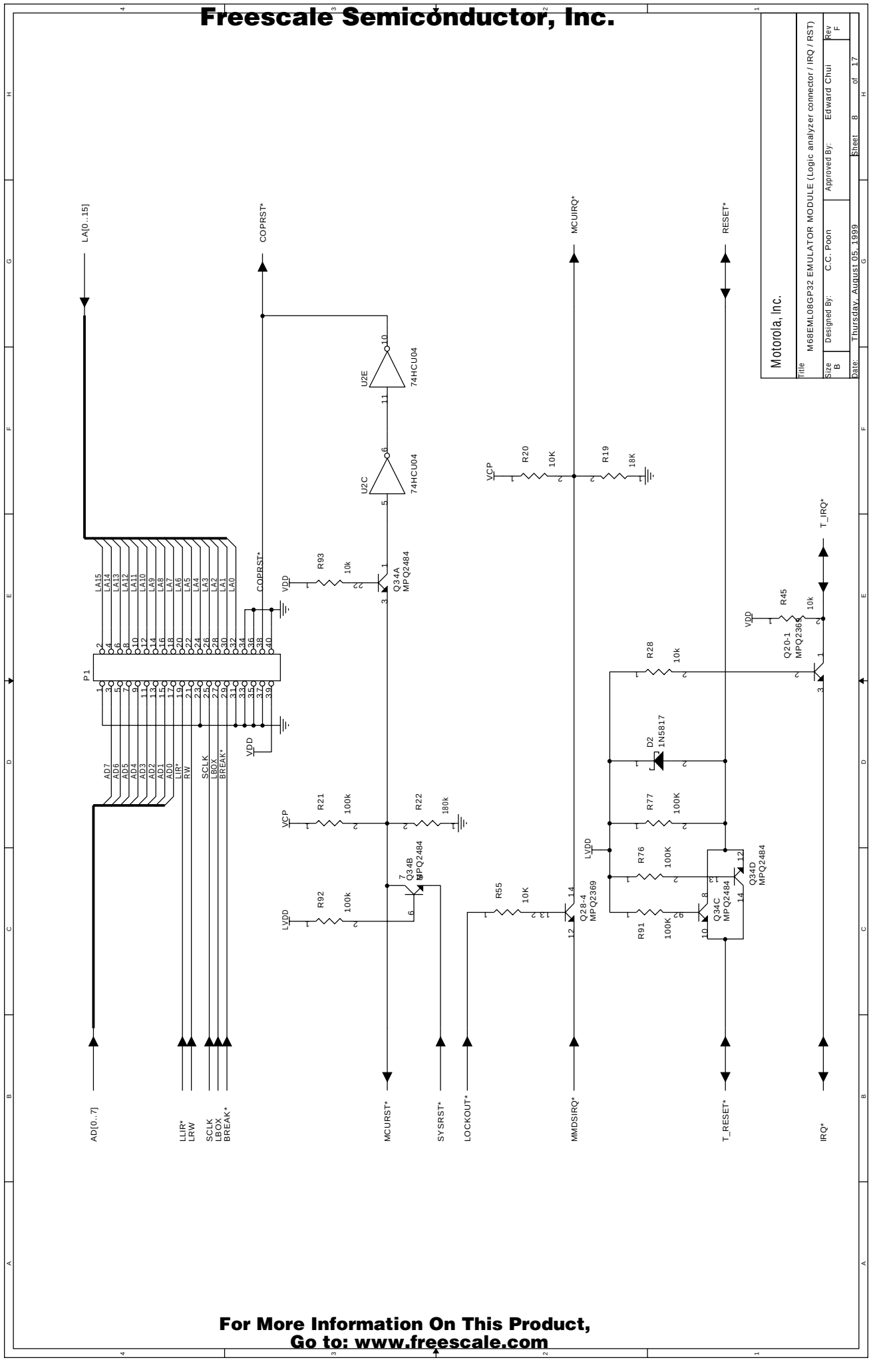
Title: M68EML08GP32 EMULAOTR MODULE (JL3 PORT A EMULATION)

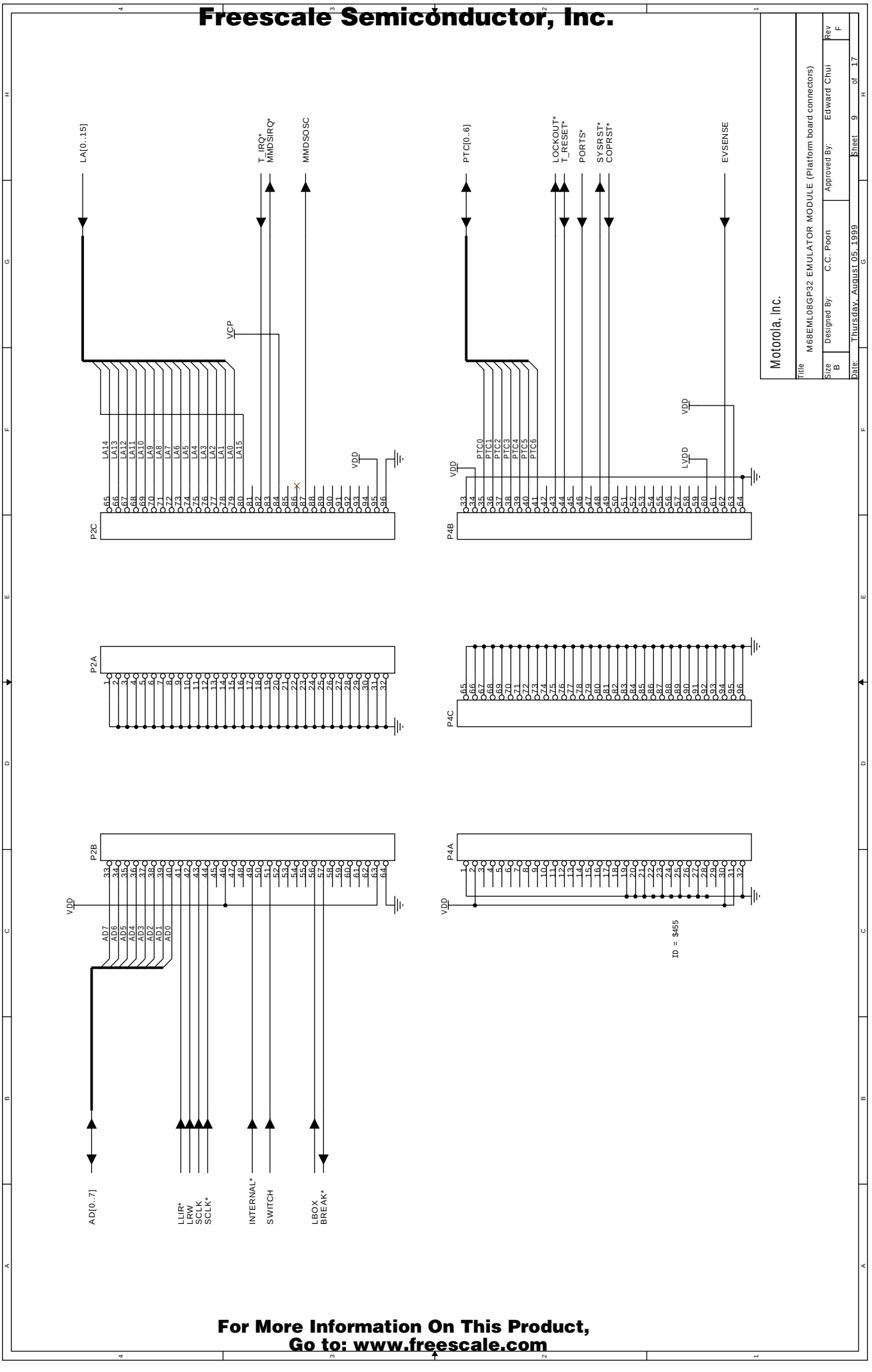
Size	Designed By:	Approved By:	Rev
B	C.C. Poon	Edward Chui	F

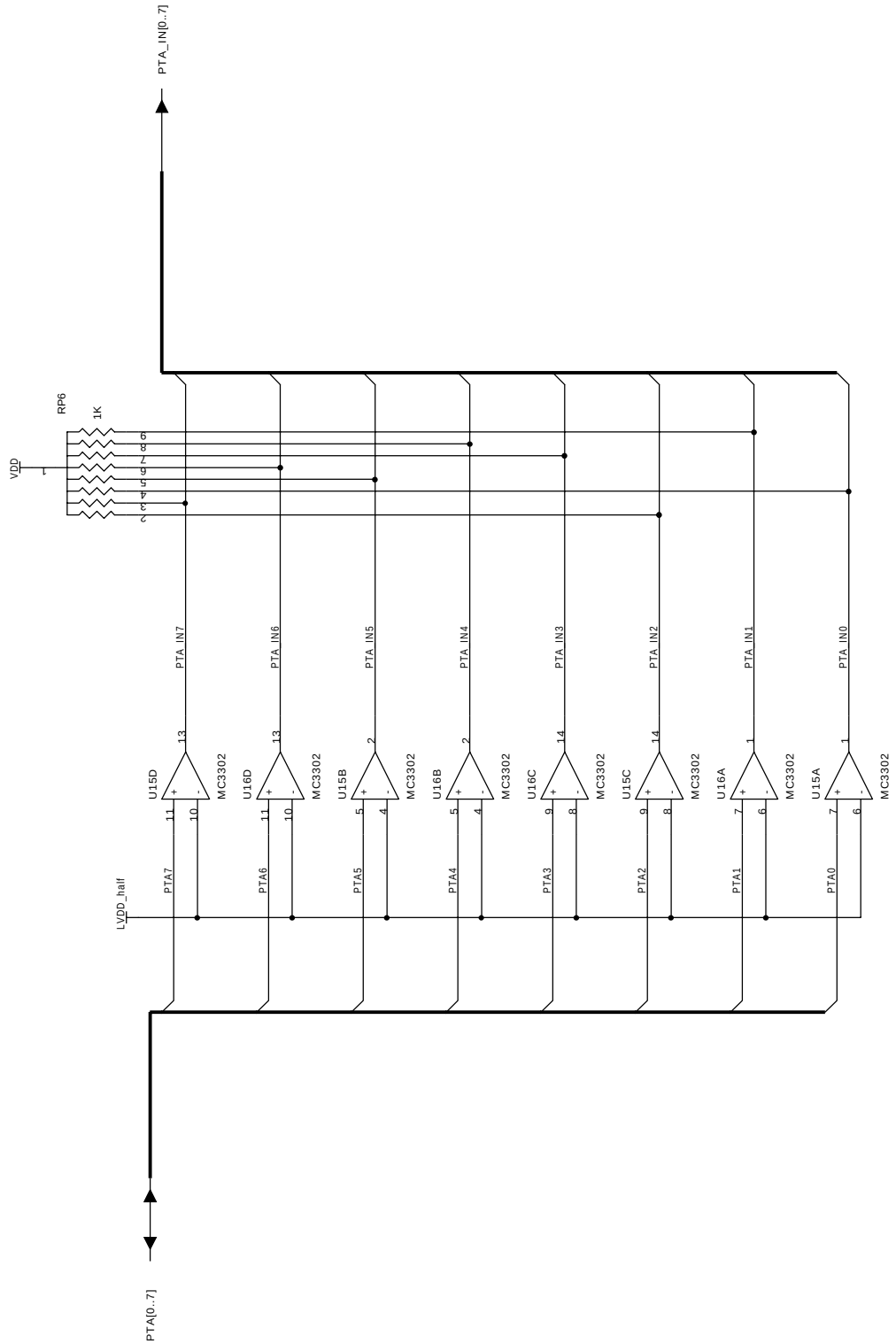
Date: Thursday, August 05, 1999 Sheet 6 of 17



Freescale Semiconductor, Inc.





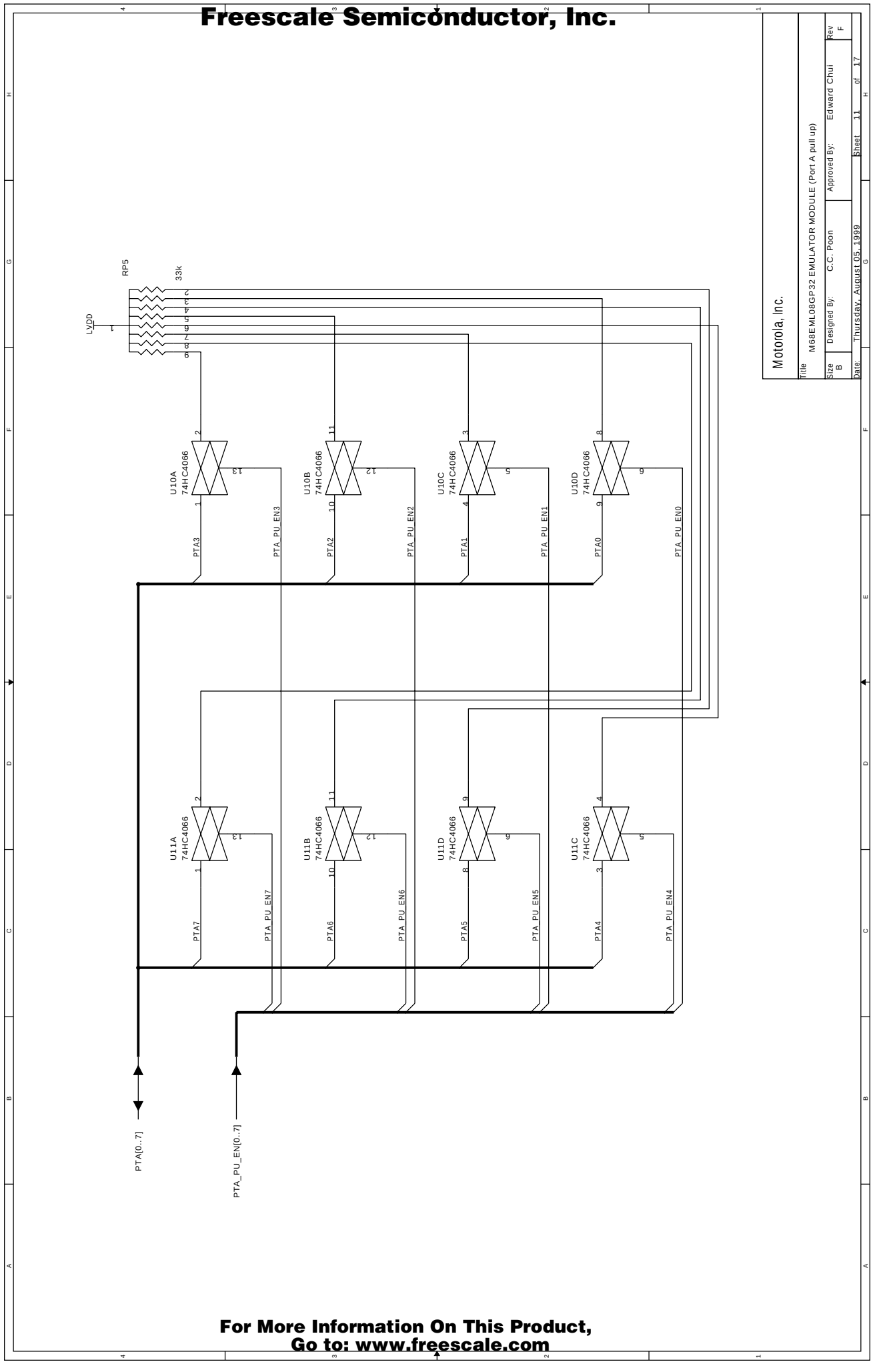


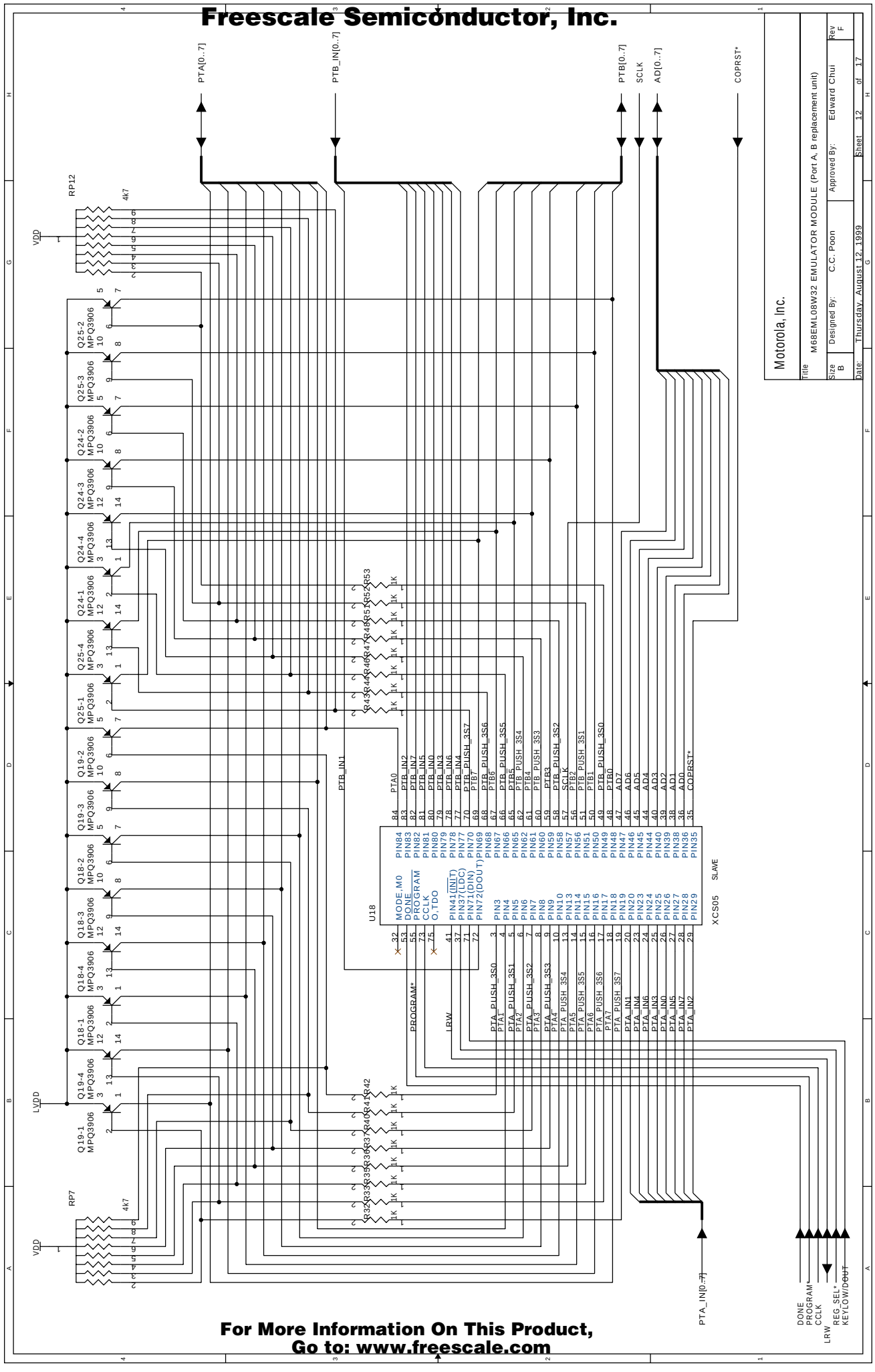
Motorola, Inc.

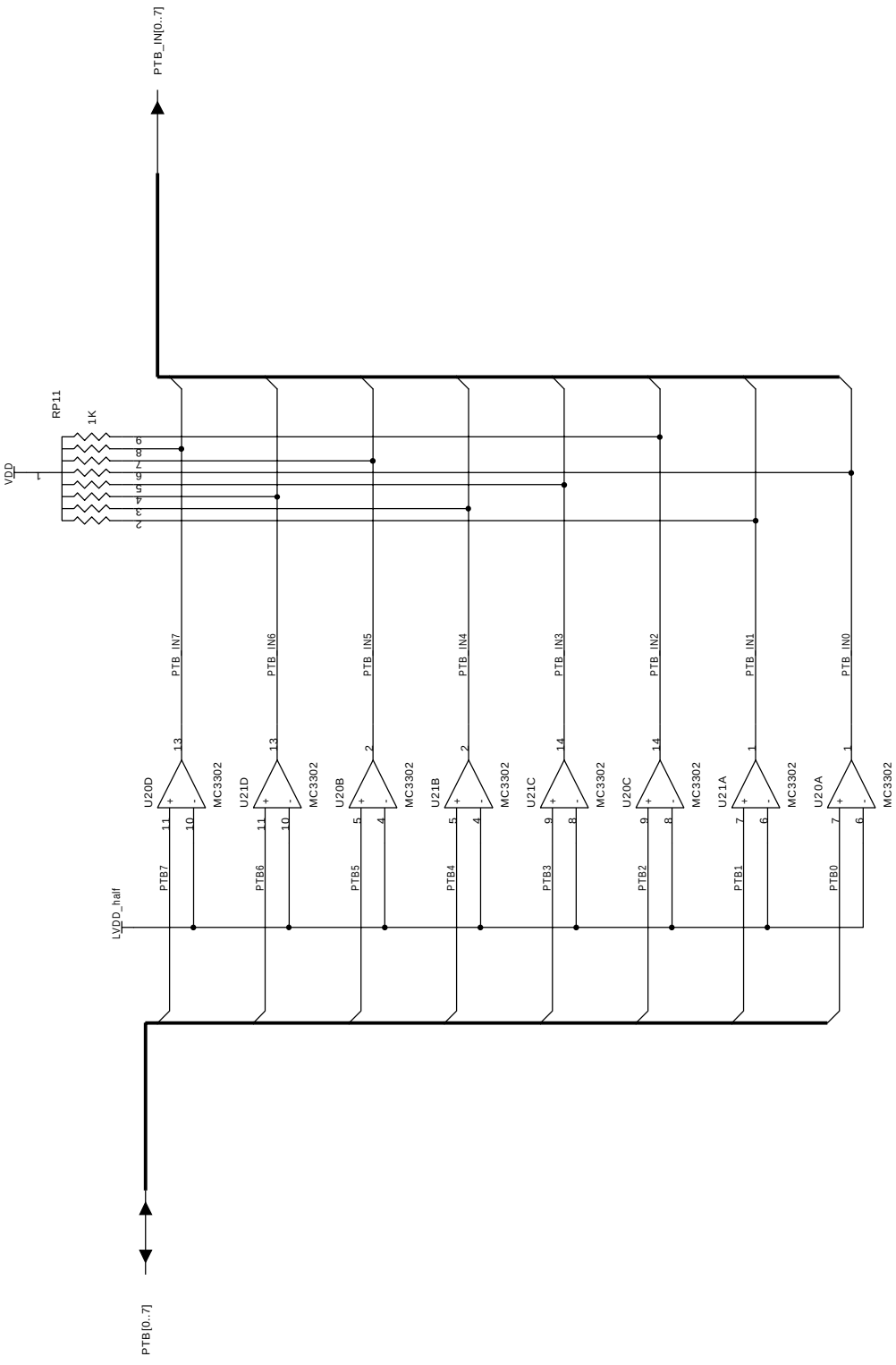
Title: M68EML08GP32 EMULATOR MODULE (Port A input comparator)

Size	Designed By:	Approved By:	Rev
B	C.C. Poon	Edward Chui	F

Date: Thursday, August 05, 1999 Sheet 10 of 17







Motorola, Inc.

Title: M68EML08GP32 EMULATOR MODULE (Port B input comparator)

Size	Designed By:	Approved By:	Rev
B	C.C. Poon	Edward Chui	F

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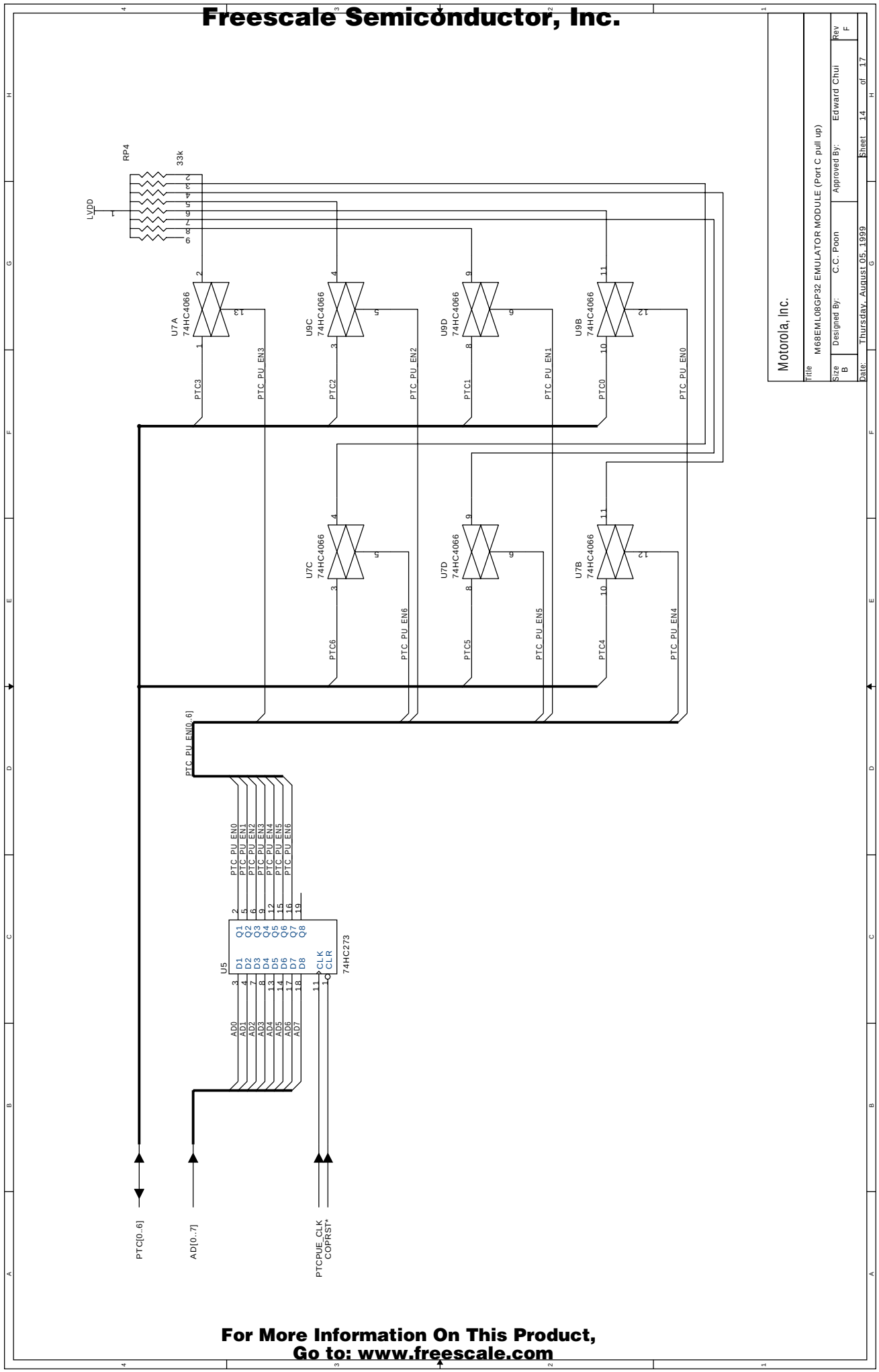

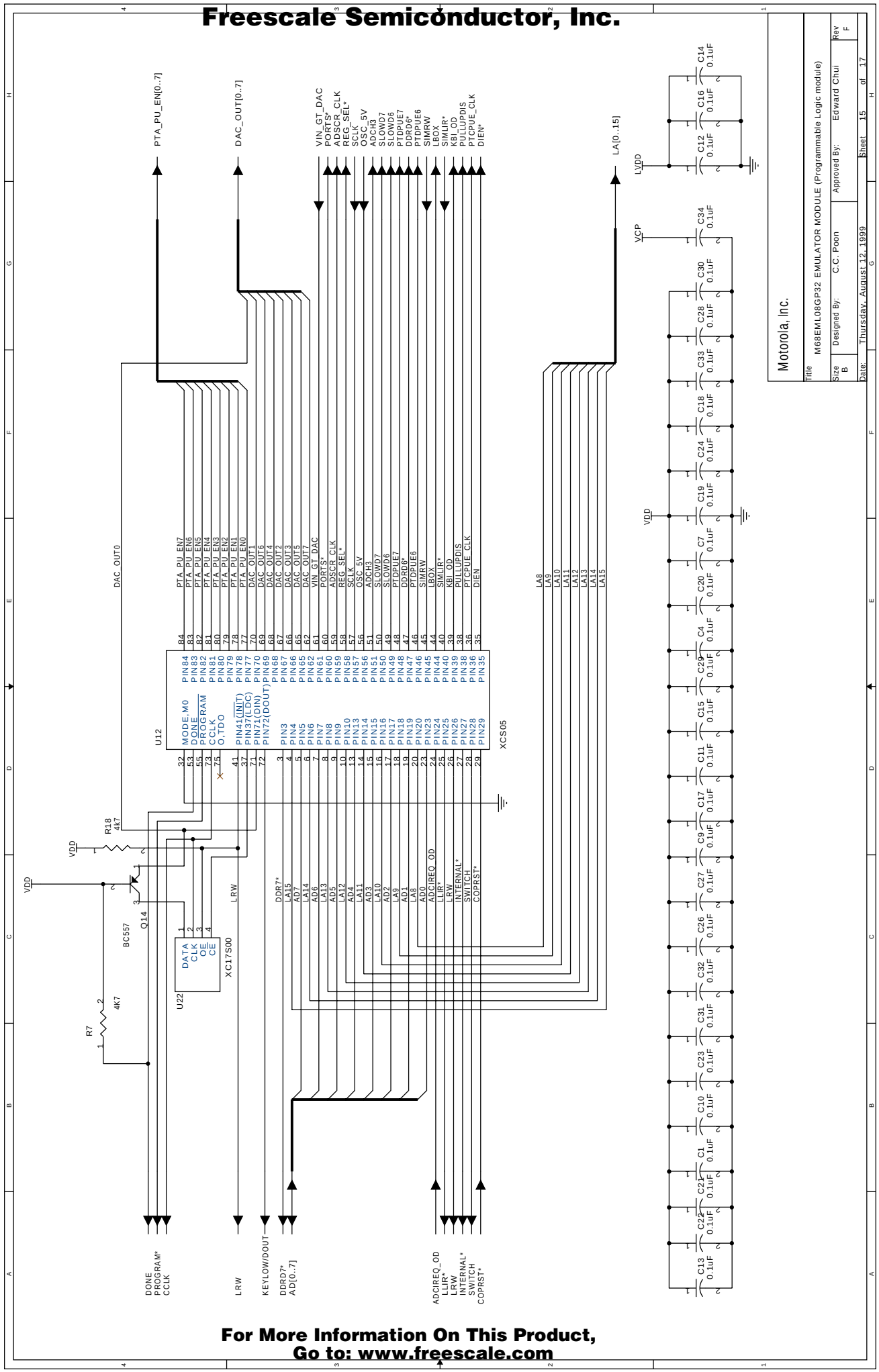

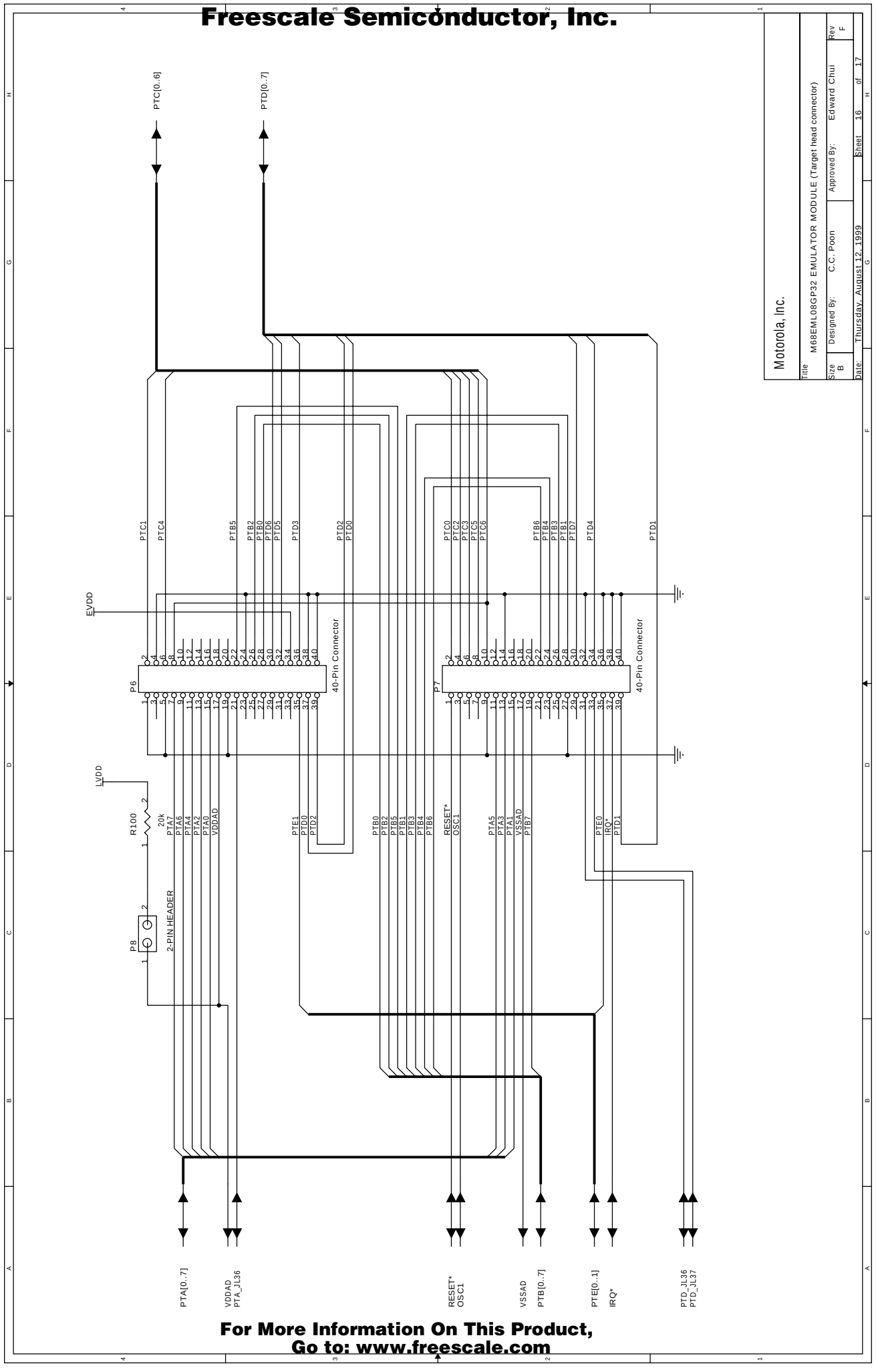

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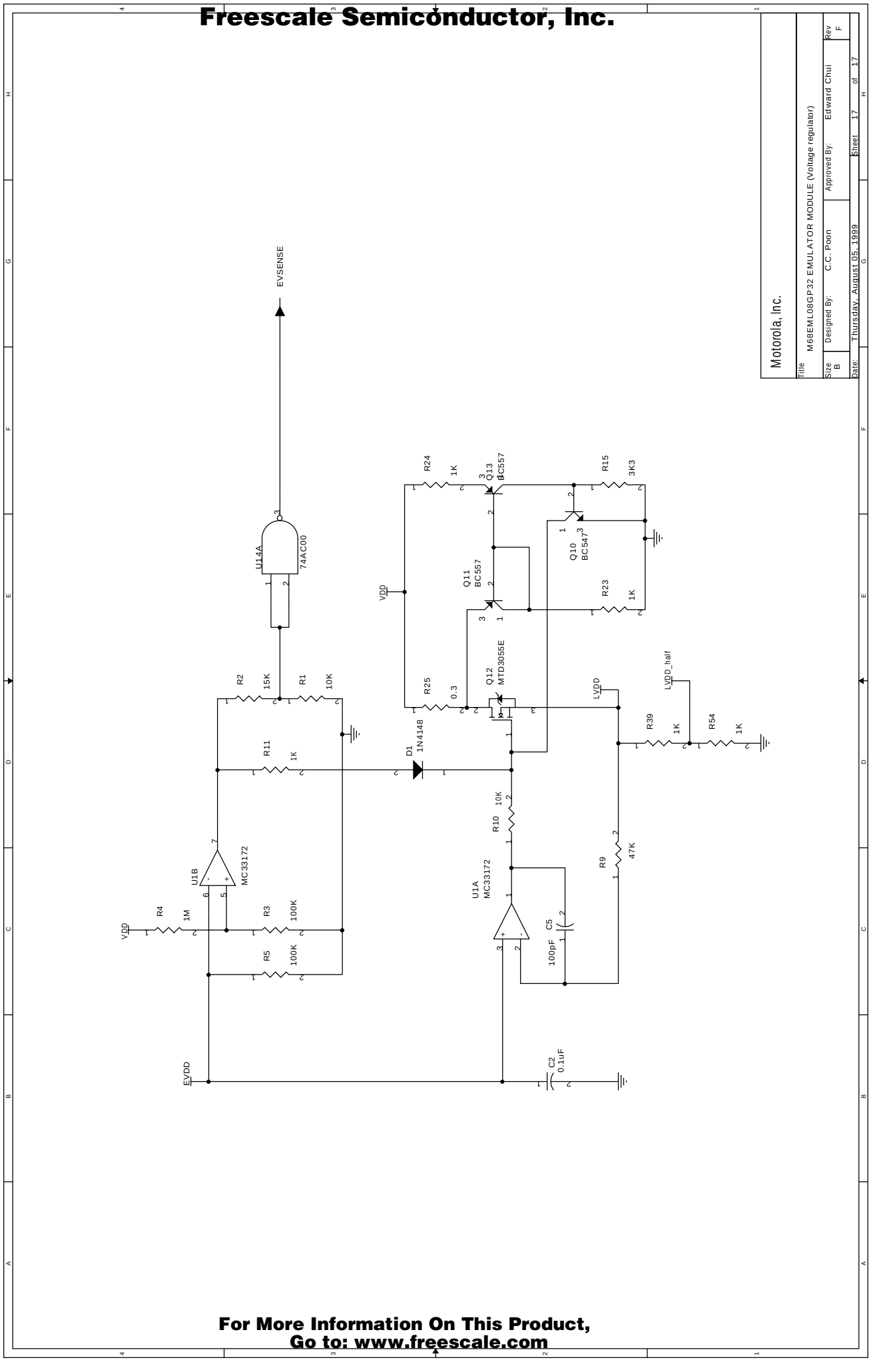

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