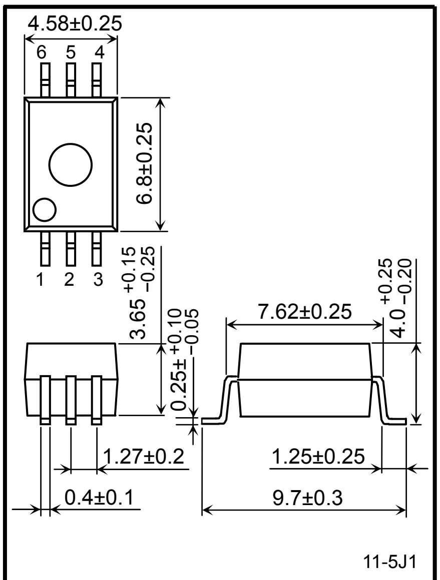
TOSHIBA Photocoupler GaAℓAs IRED + Photo IC

TLP700

Industrial inverters
Inverter for air conditioners
IGBT/Power MOS FET gate drive

Unit in mm



TOSHIBA 11-5J1

Weight: 0.26 g (typ.)

TLP700 consists of a GaAℓAs light-emitting diode and an integrated photodetector.

This unit is 6-lead SDIP package. The TLP700 is 50% smaller than the 8-pin DIP and meets the reinforced insulation class requirements of international safety standards. Therefore the mounting area can be reduced in equipment requiring safety standard certification.

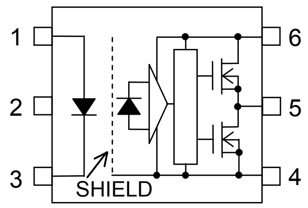
The TLP700 is suitable for gate driving circuits for IGBTs or power MOSFETs. In particular, the TLP700 is capable of “direct” gate driving of low-power IGBTs.

- Peak output current : ±2.0 A (max)
- Guaranteed performance over temperature : −40~100°C
- Supply current : 2 mA (max)
- Power supply voltage : 15~30 V
- Threshold input current : I_{FLH} = 5 mA (max)
- Switching time (t_{pLH} / t_{pHL}) : 500 ns (max)
- Common mode transient immunity : ±10 kV/μs (min)
- Isolation voltage : 5000 Vrms (min)
- Construction mechanical rating

	7.62-mm pitch standard type	10.16-mm pitch TLPXXXF type
Creepage Distance Clearance Insulation Thickness	7.0 mm (min) 7.0 mm (min) 0.4 mm (min)	8.0 mm (min) 8.0 mm (min) 0.4 mm (min)

- UL recognized : UL1577, File No. E67349
- Option (D4) type
  TÜV approval : EN60747-5-2 under plan

Pin Configuration (Top View)

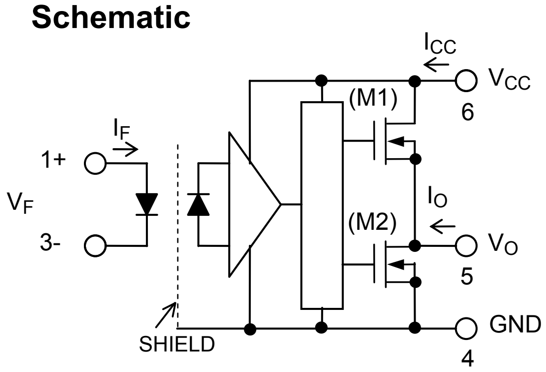


1: ANODE
2: N.C
3: CATHODE
4: GND
5: V_O (OUTPUT)
6: V_{CC}

Truth Table

Input	LED	M1	M2	Output
H	ON	ON	OFF	H
L	OFF	OFF	ON	L

Schematic



A 0.1-μF bypass capacitor must be connected between pins 6 and 4. (See Note 6.)

Absolute Maximum Ratings (Ta = 25 °C)

	Characteristics		Symbol	Rating	Unit
LED	Forward current		I_F	20	mA
	Forward current derating (Ta ≥ 85°C)		$\Delta I_F/\Delta Ta$	−0.54	mA/°C
	Peak transient forward current (Note 1)		I_{FP}	1	A
	Reverse voltage		V_R	6	V
	Junction temperature		T_j	125	°C
Detector	"H" peak output current	Ta=-40~100 °C (Note 2)	I_{OPH}	−2.0	A
	"L" peak output current		I_{OPL}	2.0	A
	Output voltage		V_O	35	V
	Supply voltage		V_{CC}	35	V
	Junction temperature		T_j	125	°C
Operating frequency (Note 3)			f	50	kHz
Operating temperature range			T_{opr}	−40~100	°C
Storage temperature range			T_{stg}	−55~125	°C
Lead soldering temperature (10 s) (Note 4)			T_{sol}	260	°C
Isolation voltage (AC, 1 minute, R.H. ≤ 60%) (Note 5)			BV_S	5000	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width P_W ≤ 1 μs, 300 pps

Note 2: Exponential waveform pulse width P_W ≤ 0.3 μs, f ≤15 kHz

Note 3: Exponential waveform I_{OPH} ≤−1.5 A (≤ 0.3 μs), I_{OPL} ≤+1.5 A (≤ 0.3 μs), Ta=100°C

Note 4: For the effective lead soldering area

Note 5: Device considered a two-terminal device: pins 1, 2 and 3 paired with pins 4, 5 and 6 respectively.

Note 6: A ceramic capacitor (0.1 μF) should be connected from pin 6 to pin 4 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property.
The total lead length between capacitor and coupler should not exceed 1 cm.

Recommended Operating Conditions

Characteristics	Symbol	Min	Typ.	Max	Unit
Input current, ON (Note 7)	$I_{F (ON)}$	7.5	—	10	mA
Input voltage, OFF	$V_{F (OFF)}$	0	—	0.8	V
Supply voltage * (Note 8)	V_{CC}	15	—	30	V
Peak output current	I_{OPH} / I_{OPL}	—	—	± 1.5	A
Operating temperature	T_{opr}	−40	—	100	°C

* This item denotes operating ranges, not meaning of recommended operating conditions.

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Note 7: Input signal rise time (fall time) ≤ 0.5 μs.

Note 8: If the Vcc rise slope is sharp, an internal circuit might not operate with stability. Please design the Vcc rise slope under 3.0 V/μs.

Electrical Characteristics (Ta = −40~100 °C, unless otherwise specified)

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.*	Max	Unit
Forward voltage		V_F	—	I_F = 10 mA, Ta = 25 °C		—	1.57	1.75	V
Temperature coefficient of forward voltage		$\Delta V_F/\Delta Ta$	—	I_F = 10 mA		—	−2.0	—	mV/°C
Input reverse current		I_R	—	V_R = 6 V, Ta = 25 °C		—	—	10	μA
Input capacitance		C_T	—	V =0 V, f = 1 MHz, Ta = 25 °C		—	100	—	pF
Output current (Note 9)	"H" Level	I_{OPH1}	1	V_{CC} = 15 V, I_F = 5 mA	$V_{6\text{-}5}$ = -3.5 V	−1.0	−1.4	—	A
		I_{OPH2}			$V_{6\text{-}5}$ = -7 V	−1.5	—	—	
	"L" Level	I_{OPL1}	2	V_{CC} = 15 V, I_F = 0 mA	$V_{5\text{-}4}$ = 2.5 V	1.0	1.4	—	
		I_{OPL2}			$V_{5\text{-}4}$ = 7 V	1.5	—	—	
Output voltage	"H" Level	V_{OH}	3	VCC1=+15V, VEE1=-15V R_L = 200Ω, I_F = 5 mA		11	13.7	—	V
	"L" Level	V_{OL}	4	VCC1=+15V, VEE1=-15V R_L = 200Ω,V_F = 0.8 V		—	-14.9	-12.5	
Supply current	"H" Level	I_{CCH}	5	V_{CC} = 30 V V_O=Open	I_F = 10 mA	—	1.3	2.0	mA
	"L" Level	I_{CCL}	6		I_F = 0 mA	—	1.3	2.0	
Threshold input current	L → H	I_{FLH}	—	V_{CC} = 15 V, V_O > 1 V		—	1.8	5	mA
Threshold input voltage	H → L	V_{FHL}	—	V_{CC} = 15 V, V_O < 1 V		0.8	—	—	V
Supply voltage		V_{CC}	—	—		15	—	30	V
UVLO thresh hold		V_{UVLO+}	—	V_O > 2.5V, IF = 5 mA		11.0	12.5	13.5	V
		V_{UVLO-}	—	V_O < 2.5V, IF = 5 mA		9.5	11.0	12.0	V
UVLO hysteresis		$UVLO_{HYS}$	—	—		—	1.5	—	V

(*): All typical values are at Ta = 25°C

Note 9: Duration of Io time ≤ 50 μs, 1 pulse

Note 10: This product is more sensitive than conventional products to electrostatic discharge (ESD) owing to its low power consumption design.
It is therefore all the more necessary to observe general precautions regarding ESD when handling this component.

Isolation Characteristics (Ta = 25 °C)

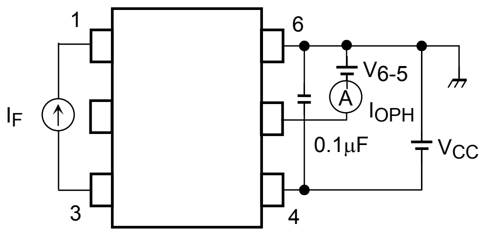
Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Capacitance input to output	C_S	Vs = 0 V , f = 1MHz (Note 5)	—	1.0	—	pF
Isolation resistance	R_S	R.H. ≤ 60 %, V_S = 500 V (Note 5)	1×10^{12}	10^{14}	—	Ω
Isolation voltage	BV_S	AC, 1 minute	5000	—	—	Vrms
		AC, 1 second, in oil	—	10000	—	
		DC, 1 minute, in oil	—	10000	—	Vdc

Switching Characteristics (Ta = −40~100 °C, unless otherwise specified)

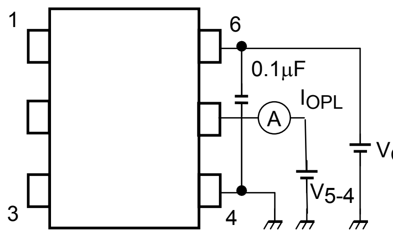
Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.*	Max	Unit
Propagation delay time	L → H	t_{pLH}	7	V_{CC} = 30 V R_g = 20 Ω C_g = 10 nF	I_F = 0 → 5 mA	50	—	500	ns
	H → L	t_{pHL}			I_F = 5 → 0 mA	50	—	500	
Output rise time (10–90 %)		t_r			I_F = 0 → 5 mA	—	50	—	
Output fall time (90–10 %)		t_f			I_F = 5 → 0 mA	—	50	—	
Switching time dispersion between ON and OFF		$\lvert t_{pHL}-t_{pLH} \rvert$			I_F = 0 ↔ 5 mA	—	—	250	
Common mode transient immunity at HIGH level output		CM_H	8	V_{CM} =1000 Vp-p Ta = 25 °C V_{CC} = 30 V	I_F = 5 mA $V_{O\ (min)}$ = 26 V	−10000	—	—	V/μs
Common mode transient immunity at LOW level output		CM_L			I_F = 0 mA $V_{O\ (max)}$ = 1 V	10000	—	—	

(*): All typical values are at Ta = 25 °C.

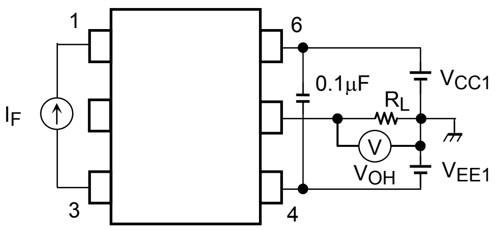
Test Circuit 1: I_{OPH}



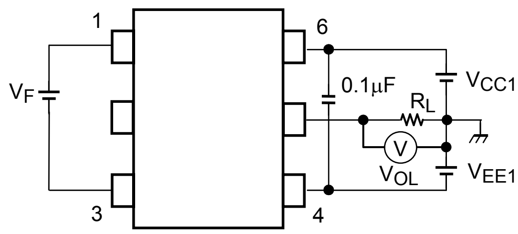
Test Circuit 2: I_{OPL}



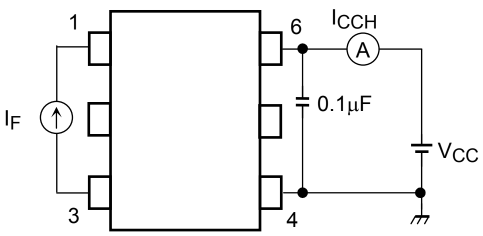
Test Circuit 3: V_{OH}



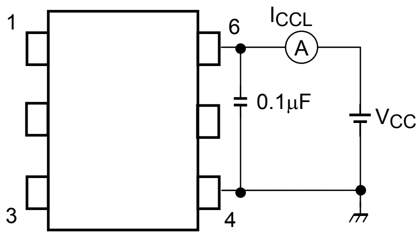
Test Circuit 4: V_{OL}



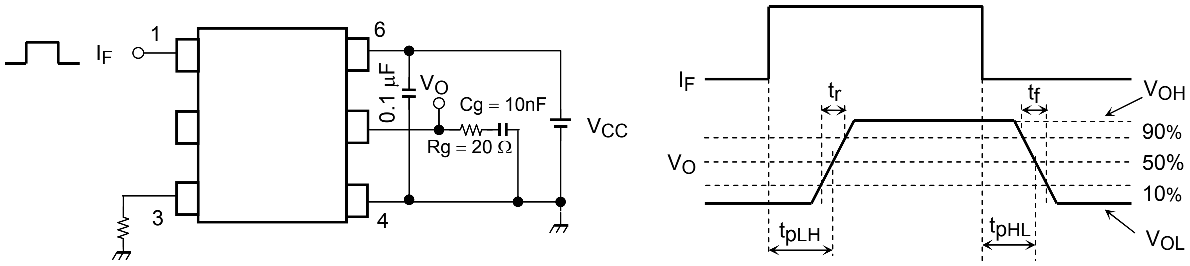
Test Circuit 5: I_{CCH}



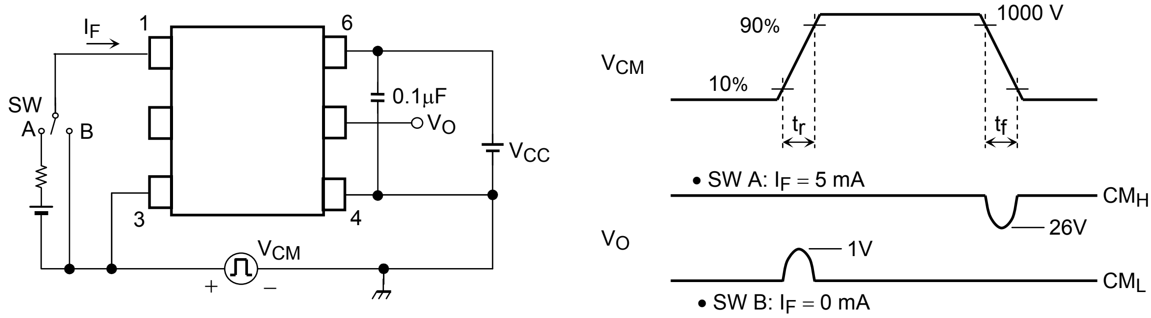
Test Circuit 6: I_{CCL}



Test Circuit 7: t_{pLH}, t_{pHL}, t_r, t_f, $| t_{pHL} - t_{pLH} |$



Test Circuit 8: CM_H, CM_L



$$CM_H = -\frac{800\text{ V}}{t_f\ (\mu s)}$$

$$CM_L = \frac{800\text{ V}}{t_r\ (\mu s)}$$

CM_L (CM_H) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the LOW (HIGH) state.

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20070701-EN

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