



# TLP552

GaAlAs IRED & PHOTO-IC

(TLP552)

ISOLATED LINE RECEIVER

SIMPLEX/MULTIPLEX DATA TRANSMISSION

COMPUTER-PERIPHERAL INTERFACE

MICROPROCESSOR SYSTEM INTERFACE

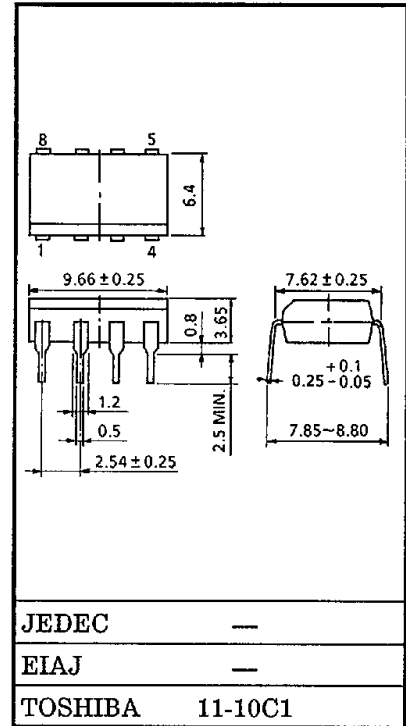
DIGITAL ISOLATION FOR A/D, D/A CONVERSION

The TOSHIBA TLP552 is a photocoupler which combines a GaAlAs IRED as the emitter and an integrated high gain, high speed photodetector. This unit is 8-lead DIP package.

The output of the detector circuit is an open collector, Schottky clamped transistor.

- TTL/LSTTL Compatible :  $V_{CC}=5V$
- Isolation Voltage :  $2500V_{rms}$  (Min.)
- Switching Speed :  $t_{pHL}, t_{pLH}=60ns$  (Typ.)  
(@ $R_L=350\Omega$ )
- Guaranteed Performance Over Temp. :  $0^\circ C \sim 70^\circ C$
- UL Recognized : UL1577, File No. E67349

Unit in mm



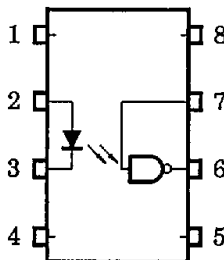
Weight : 0.54g

## TRUTH TABLE (Positive Logic)

INPUT	ENABLE	OUTPUT
H	H	L
L	H	H
H	L	H
L	L	H

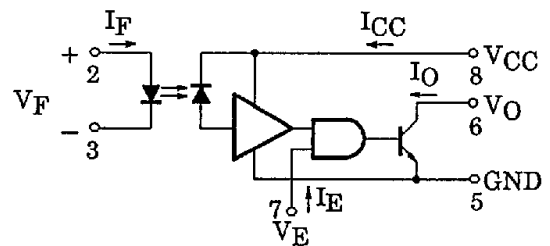
A  $0.1\mu F$  bypass capacitor must be connected between pins 8 and 5 (See Note 3).

## PIN CONFIGURATION (TOP VIEW)



- 1.: NC
- 2.: ANODE
- 3.: CATHODE
- 4.: NC
- 5.: GND
- 6.: OUTPUT (OPEN COLLECTOR)
- 7.: ENABLE
- 8.: VCC

## SCHEMATIC



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## RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input Current, Low Level	$I_{FL}$	0	—	250	$\mu A$
Input Current, High Level	$I_{FH}$	7	—	20	mA
Supply Voltage, Output	$V_{CC}$	4.5	—	5.5	V
High Level Enable Voltage	$V_{EH}$	2.0	—	$V_{CC}$	V
Low Level Enable Voltage	$V_{EL}$	0	—	0.8	V
Fan Out (TTL Load)	N	—	—	8	—
Operating Temperature	$T_{opr}$	0	—	70	$^{\circ}C$

MAXIMUM RATINGS ( $T_a = 25^{\circ}C$ )

CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current	$I_F$	20	mA
	Pulse Forward Current (Note 1)	$I_{FP}$	40	mA
	Peak Transient Forward Current (Note 2)	$I_{FPT}$	0.5	A
	Reverse Voltage	$V_R$	5	V
	Diode Power Dissipation	$P_D$	40	mW
DETECTOR	Output Current	$I_O$	50	mA
	Output Voltage	$V_O$	7	V
	Supply Voltage (1 Minute Maximum)	$V_{CC}$	7	V
	Enable Input Voltage (Not to exceed $V_{CC}$ by more than 500mV)	$V_E$	5.5	V
	Output Collector Power Dissipation	$P_O$	85	mW
Operating Temperature Range		$T_{opr}$	0~70	$^{\circ}C$
Storage Temperature Range		$T_{stg}$	-55~125	$^{\circ}C$
Lead Solder Temperature (10sec.)**		$T_{sold}$	260	$^{\circ}C$
Isolation Voltage (R.H. $\leq 60\%$ , AC / 1min., Note 4)		$BV_S$	2500	$V_{rms}$

\*\* Soldering portion of lead : up to 2mm from the body of the device.

Note 1 : 50% duty cycle, 1ms pulse width.

Note 2 : Pulse width  $\leq 1\mu s$ , 300pps.

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ELECTRICAL CHARACTERISTICS (For  $0^{\circ}\text{C} \leq T_a \leq 70^{\circ}\text{C}$ , unless otherwise specified.)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Forward Voltage	$V_F$	$I_F=10\text{mA}$ , $T_a=25^{\circ}\text{C}$	—	1.65	1.8	V
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_a$	$I_F=10\text{mA}$	—	-2.0	—	mV/ $^{\circ}\text{C}$
Input Reverse Current	$I_R$	$V_R=5\text{V}$ , $T_a=25^{\circ}\text{C}$	—	—	10	$\mu\text{A}$
Input Capacitance	$C_T$	$V_F=0$ , $f=1\text{MHz}$	—	45	—	pF
High Level Output Current	$I_{OH}$	$V_{CC}=5.5\text{V}$ , $V_O=5.5\text{V}$ $I_F=250\mu\text{A}$ , $V_E=2.0\text{V}$	—	10	250	$\mu\text{A}$
Low Level Output Voltage	$V_{OL}$	$V_{CC}=5.5\text{V}$ , $I_F=5\text{mA}$ $V_{EH}=2.0\text{V}$ $I_{OL}(\text{Sinking})=13\text{mA}$	—	0.4	0.6	V
Input Current Logic Low Output Level	$I_{FH}$	$I_{OL}=13\text{mA}$ (Sinking), $V_O=0.6\text{V}$ $V_{CC}=5.5\text{V}$ , $V_{EH}=2.0\text{V}$	—	—	5	mA
High Level Enable Current	$I_{EH}$	$V_{CC}=5.5\text{V}$ , $V_E=2.0\text{V}$	—	-0.1	—	mA
Low Level Enable Current	$I_{EL}$	$V_{CC}=5.5\text{V}$ , $V_E=0.5\text{V}$	—	-1.6	-2.0	mA
High Level Supply Current	$I_{CCH}$	$V_{CC}=5.5\text{V}$ , $I_F=0$ $V_E=0.5\text{V}$	—	7	15	mA
Low Level Supply Current	$I_{CCL}$	$V_{CC}=5.5\text{V}$ , $I_F=10\text{mA}$ $V_E=0.5\text{V}$	—	12	18	mA
Current Transfer Ratio	CTR	$I_F=5.0\text{mA}$ , $R_L=100\Omega$ $V_{CC}=5\text{V}$ , $T_a=25^{\circ}\text{C}$	—	1000	—	%
Resistance (Input-Output)	$R_S$	$V_S=500\text{V}$ , R.H. $\leq 60\%$ $T_a=25^{\circ}\text{C}$ (Note 4)	—	$10^{12}$	—	$\Omega$
Capacitance (Input-Output)	$C_S$	$f=1\text{MHz}$ , $V_S=0$ , $T_a=25^{\circ}\text{C}$ (Note 4)	—	0.6	—	pF

\* All typical values are at  $V_{CC}=5\text{V}$ ,  $T_a=25^{\circ}\text{C}$ .

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SWITCHING CHARACTERISTICS ( $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$ )

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time to High Output Level (L→H)	$t_{pLH}$	1	$R_L = 350\Omega$ , $C_L = 15\text{pF}$ $I_F = 7.5\text{mA}$	—	60	120	ns
Propagation Delay Time to Low Output Level (H→L)	$t_{pHL}$		$R_L = 350\Omega$ , $C_L = 15\text{pF}$ $I_F = 7.5\text{mA}$	—	60	120	ns
Output Rise Fall Time (10~90%)	$t_r$ , $t_f$		$R_L = 350\Omega$ , $C_L = 15\text{pF}$ $I_F = 7.5\text{mA}$	—	30	—	ns
Propagation Delay Time of Enable from $V_{EH}$ to $V_{EL}$	$t_{ELH}$	2	$R_L = 350\Omega$ , $C_L = 15\text{pF}$ $I_F = 7.5\text{mA}$ , $V_{EH} = 3.0\text{V}$	—	25	—	ns
Propagation Delay Time of Enable from $V_{EL}$ to $V_{EH}$	$t_{EHL}$		$R_L = 350\Omega$ , $C_L = 15\text{pF}$ $I_F = 7.5\text{mA}$ , $V_{EH} = 3.0\text{V}$	—	25	—	ns
Common Mode Transient Immunity at Logic High Output Level	$CM_H$	3	$V_{CM} = 200\text{V}$ , $R_L = 350\Omega$ $V_O(\text{min.}) = 2\text{V}$ , $I_F = 0\text{mA}$ (Note 6)	—	200	—	$\text{V} / \mu\text{s}$
Common Mode Transient Immunity at Logic Low Output Level	$CM_L$		$V_{CM} = 200\text{V}$ , $R_L = 350\Omega$ $V_O(\text{max.}) = 0.8\text{V}$ , $I_F = 5\text{mA}$ (Note 6)	—	-500	—	$\text{V} / \mu\text{s}$

Note 3 : A ceramic capacitor ( $0.1\mu\text{F}$ ) should be connected from pin 8 and pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching properties. The total lead length between capacitor and coupler should not exceed 1cm.

Note 4 : Device considered a two-terminal device : Pins 1, 2, 3 and 4 shorted together, and Pins 5, 6, 7 and 8 shorted together.

Note 5 : Enable Input : No pull up resistor required as the device has an internal pull up resistor.

Note 6 :  $CM_L$  : The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the low output state (i.e.,  $V_{OUT} < 0.8\text{V}$ ).

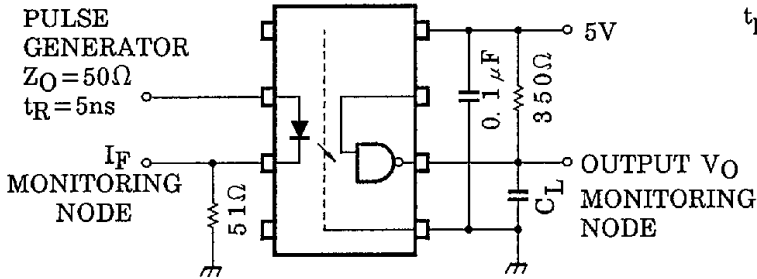
$CM_H$  : The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the high state (i.e.,  $V_{OUT} > 2.0\text{V}$ ).  
Measured in volts per microsecond ( $\text{V} / \mu\text{s}$ ).

Note 7 : Maximum electrostatic discharge voltage for any pins : 180V ( $C = 200\text{pF}$ ,  $R = 0$ )

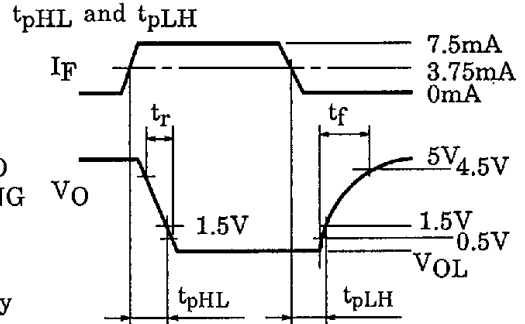
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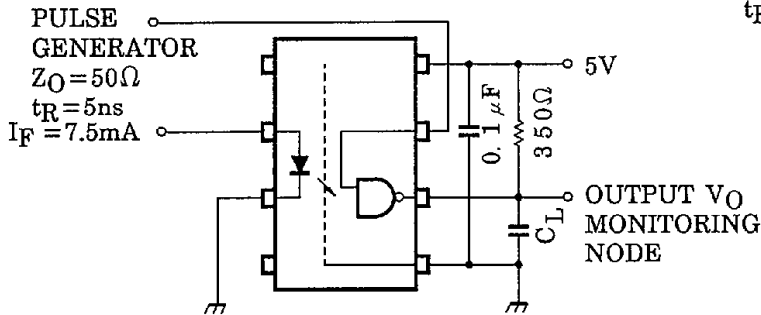
## TEST CIRCUIT 1



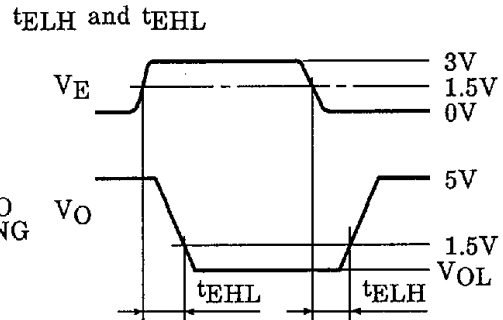
$C_L$  is approximately 15pF which includes probe and stray wiring capacitance.



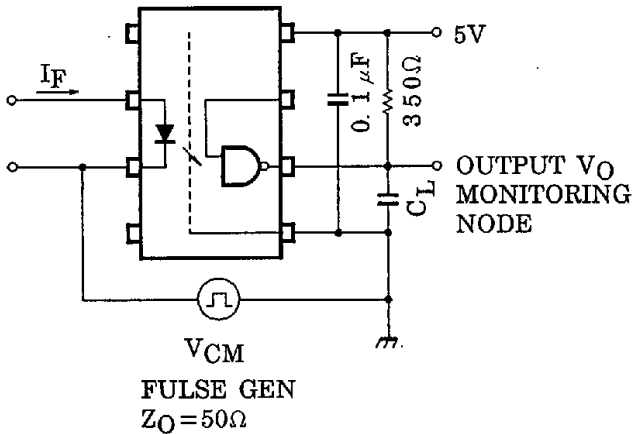
## TEST CIRCUIT 2



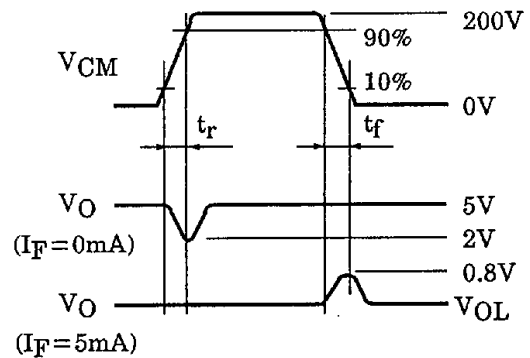
$C_L$  is approximately 15pF which includes probe and stray wiring capacitance.



## TEST CIRCUIT 3

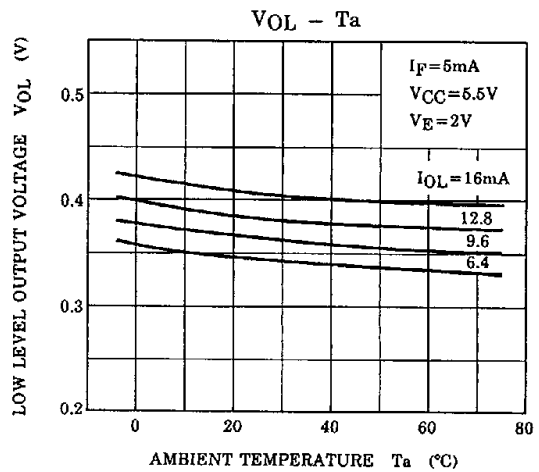
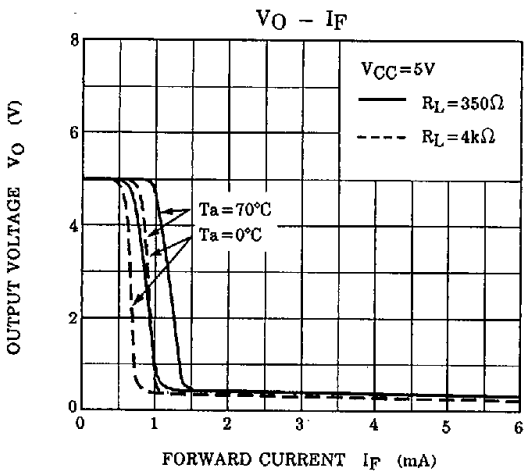
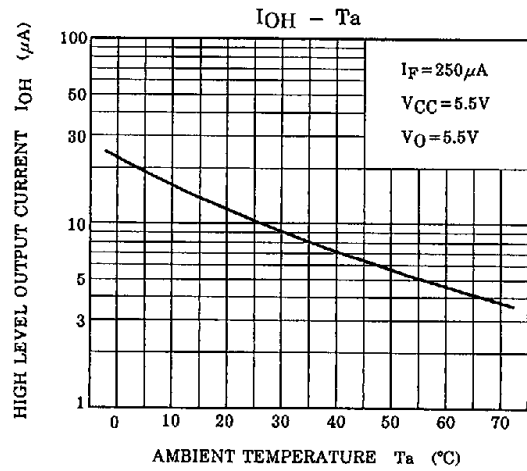
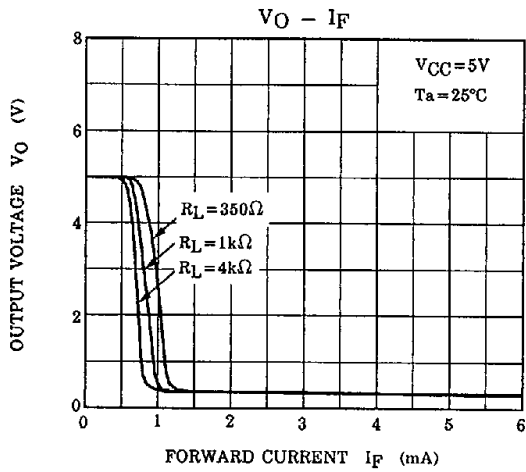
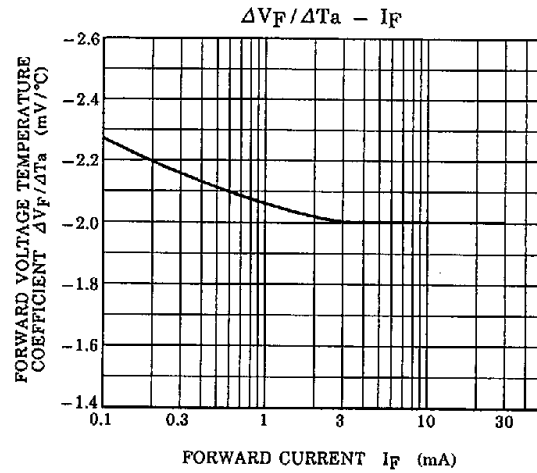
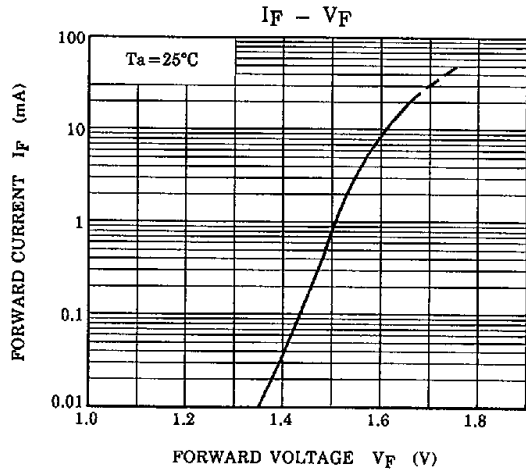


## Transient Immunity and Typical Waveform



$$CM_H = \frac{160(V)}{t_r(\mu s)}, \quad CM_L = \frac{160(V)}{t_f(\mu s)}$$

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