MC145705
MC145706
MC145707

Product Preview

5 Volt Only Driver/Receiver with an Integrated Standby Mode

EIA–232–E and CCITT V.28

The MC145705/06/07 are a series of silicon–gate CMOS transceiver ICs that fulfill the electrical specifications of EIA–232–E and CCITT V.28 while operating from a single + 5 V power supply. These transceiver series are high performance and low power consumption devices that are equipped with standby and output enable function.

A voltage doubler and inverter convert the + 5 V to ± 10 V. This is accomplished through an on–board 20 kHz oscillator and four inexpensive external electrolytic capacitors.

The MC145705 is composed of two drivers and three receivers, the MC145706 has three drivers and two receivers, and the MC145707 has three drivers and three receivers. These drivers and receivers are virtually identical to those of the MC145407.

Available Driver/Receiver Combinations

Device	Drivers	Receivers	No. of Pins
MC145705	2	3	20
MC145706	3	2	20
MC145707	3	3	24

Drivers:

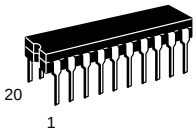
- ± 7.5 Output Swing
- 300 Ω Power–Off Impedance
- Output Current Limiting
- TTL and CMOS Compatible Inputs
- Three–State Outputs During Standby Mode
- Hold Output OFF (MARK) State by TxEN Pin

Receivers:

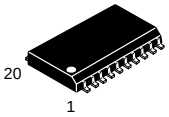
- ± 25 V Input Range
- 3 to 7 kΩ Input Impedance
- 0.8 V Hysteresis for Enhanced Noise Immunity
- Three–State Outputs During Standby Mode

Charge Pumps:

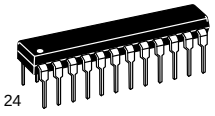
- + 5 to ± 10 V Dual Charge Pump Architecture
- Supply Outputs Capable of Driving Three Drivers on the MC145403/06 Simultaneously
- Requires Four Inexpensive Electrolytic Capacitors
- On–Chip 20 kHz Oscillators



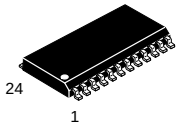
P SUFFIX
PLASTIC DIP
CASE 738



DW SUFFIX
SOG PACKAGE
CASE 751D



P SUFFIX
PLASTIC DIP
CASE 724



DW SUFFIX
SOG PACKAGE
CASE 751E

ORDERING INFORMATION

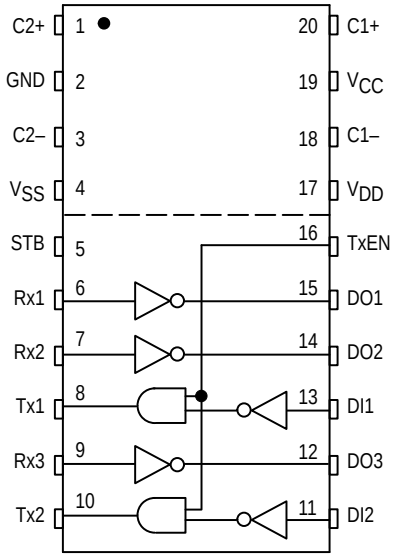
MC145705P	Plastic DIP
MC145706P	Plastic DIP
MC145707P	Plastic DIP
MC145705DW	SOG Package
MC145706DW	SOG Package
MC145707DW	SOG Package

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

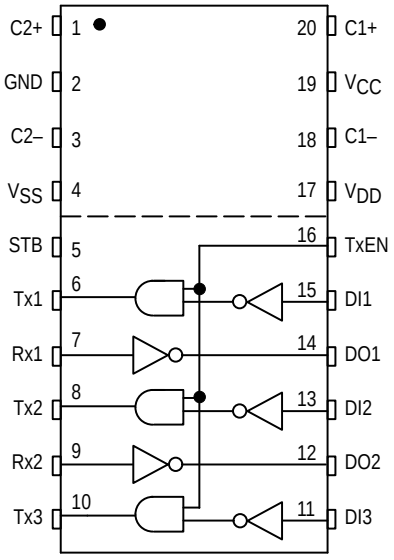
REV 1
8/95

PIN ASSIGNMENTS

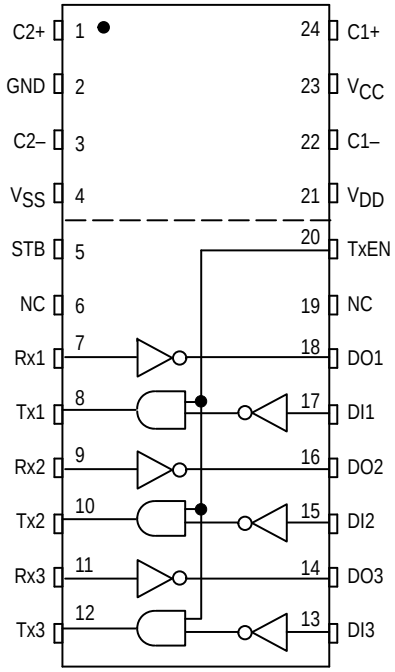
MC145705
2 DRIVERS/3 RECEIVERS



MC145706
3 DRIVERS/2 RECEIVERS



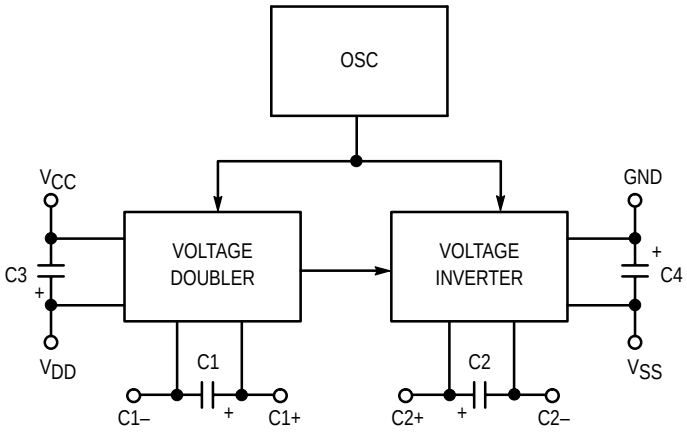
MC145707
3 DRIVERS/3 RECEIVERS



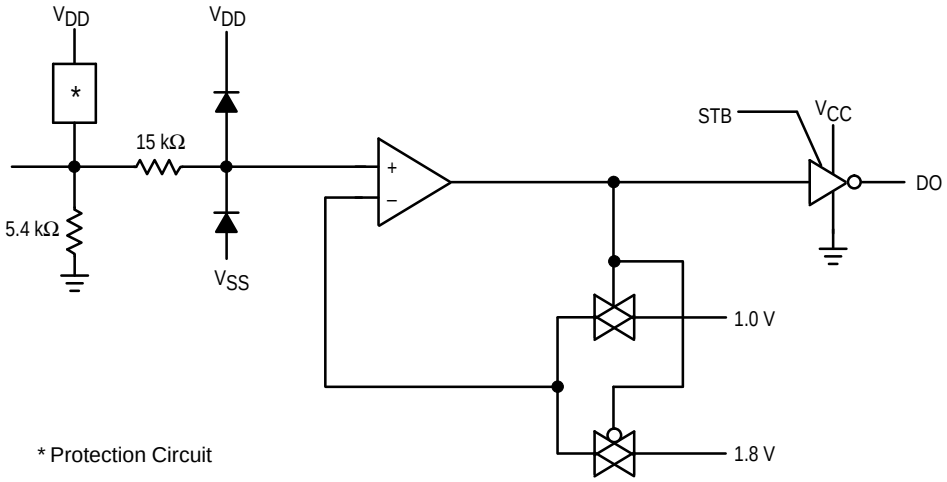
NC = NO CONNECTION

FUNCTION DIAGRAM

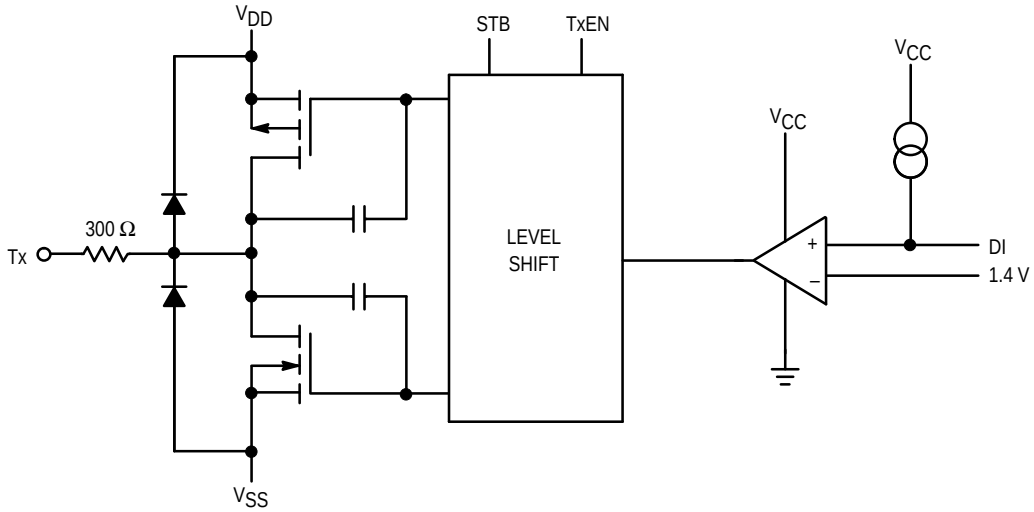
CHARGE PUMPS



RECEIVER



DRIVER



MAXIMUM RATINGS (Voltage Polarities Referenced to GND)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	– 0.5 to + 6.0	V
Input Voltage Rx1 – Rx3 Inputs DI1 – DI3 Inputs	V_{IR}	V_{SS} – 15 to V_{DD} + 15 0.5 to V_{CC} + 15	V
DC Current per Pin	I	± 100	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 85 to + 150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, it is recommended that the voltage at the DI and DO pins be constrained to the range $GND \le V_{DI} \le V_{DD}$ and $GND \le V_{DO} \le V_{CC}$. Also, the voltage at the Rx pin should be constrained to $(V_{SS} – 15\ V) \le V_{Rx1 – Rx3} \le (V_{DD} + 15\ V)$, and Tx should be constrained to $V_{SS} \le V_{Tx1 – Tx3} \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., GND or V_{CC} for DI, and GND for Rx).

RECOMMENDED OPERATING LIMITS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	V_{CC}	4.5	5	5.5	V
Operating Temperature Range	T_A	– 40	—	85	°C

DC ELECTRICAL CHARACTERISTICS (Voltage polarities referenced to GND = 0 V; C1 – C4 = 10 µF; T_A = – 40 to + 85°C)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supply		V_{CC}	4.5	5	5.5	V
Quiescent Supply Current (Output Unloaded, Input Low)		I_{CC}	—	1.7	3.5	mA
Quiescent Supply Current (Standby Mode) (Output Unloaded, Input Open)		$I_{CC(STB)}$	—	< 10	20	µA
Control Signal Input Voltage (STB, TxEN)	Logic Low Logic High	V_{IL} V_{IH}	— V_{CC} – 0.5	— —	0.5 —	V
Control Signal Input Current	Logic Low (TxEN) Logic High (STB)	I_{IL} I_{IH}	— —	— —	– 10 10	µA
Charge Pumps Output Voltage (C1, C2, C3, C4 = 10 µF)						V
Output Voltage (V_{DD})	I_{load} = 0 mA I_{load} = 5 mA I_{load} = 10 mA	V_{DD}	8.5 7.5 6.0	10.0 9.5 9.0	11 — —	
Output Voltage (V_{SS})	I_{load} = 0 mA I_{load} = 5 mA I_{load} = 10 mA	V_{SS}	– 8.5 – 7.5 – 6.0	– 10.0 – 9.2 – 8.6	– 11 — —	

RECEIVER ELECTRICAL SPECIFICATIONS

(Voltage polarities referenced to GND = 0 V; V_{CC} = + 5 V ± 10%; C1 – C4 = 10 µF; T_A = – 40 to + 85°C)

Parameter		Symbol	Min	Typ	Max	Unit
Input Turn–On Threshold ($V_{DO1 – DO3} = V_{OL}$)	Rx1 – Rx3	V_{on}	1.35	1.8	2.35	V
Input Turn–Off Threshold ($V_{DO1 – DO3} = V_{OH}$)	Rx1 – Rx3	V_{off}	0.75	1	1.25	V
Input Threshold Hysteresis ($V_{on} = V_{off}$)	Rx1 – Rx3	V_{hys}	0.6	0.8	—	V
Input Resistance		R_{in}	3	5.4	7	kΩ
High–Level Output Voltage (DO1 – DO3) $V_{Rx1 – Rx3}$ = – 3 to – 25 V	I_{out} = – 20 µA I_{out} = – 1 mA	V_{OH}	V_{CC} – 0.1 V_{CC} – 0.7	— 4.3	— —	V
Low–Level Output Voltage (DO1 – DO3) $V_{Rx1 – Rx3}$ = + 3 to + 25 V	I_{out} = + 20 µA I_{out} = + 1.6 mA	V_{OL}	— —	0.01 0.5	0.1 0.7	V

DRIVER ELECTRICAL SPECIFICATIONS

(Voltage polarities referenced to GND = 0 V; V_{CC} = + 5 V ± 10%; C1 – C4 = 10 µF; T_A = – 40 to + 85°C)

Parameter		Symbol	Min	Typ	Max	Unit
Digital Input Voltage	DI1 – DI3					V
Logic Low		V_{IL}	—	—	0.8	
Logic High		V_{IH}	2	—	—	
Input Current	DI1 – DI3					µA
V_{DI} = GND		I_{IL}	—	7	—	
V_{DI} = V_{CC}		I_{IH}	—	—	± 1.0	
Output High Voltage	Tx1 – Tx3	V_{OH}	6	7.5	—	V
($V_{DI1 – DI3}$ = Logic Low, R_L = 3 kΩ)	Tx1 – Tx6*		5	6.5	—	
Output Low Voltage	Tx1 – Tx3	V_{OL}	– 6	– 7.5	—	V
($V_{DI1 – DI3}$ = Logic High, R_L = 3 kΩ)	Tx1 – Tx6*		– 5	– 6.5	—	
Off Source Impedance	Tx1 – Tx3	Z_{off}	300	—	—	Ω
Output Short Circuit Current (V_{CC} = 5.5 V)		I_{SC}				mA
Tx1 – Tx3 Shorted to GND**			—	—	± 60	
Tx1 – Tx3 Shorted to ± 15 V***			—	—	± 100	

* Specifications for a MC14570X powering a MC145406 or MC145403 with three additional drivers/receivers.

** Specification is for one Tx output to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits could be exceeded.

*** This condition could exceed package limitations.

SWITCHING CHARACTERISTICS (V_{CC} = + 5 V, ± 10%; C1 – C4 = 10 µF; T_A = – 40 to + 85°C)

Parameter		Symbol	Min	Typ	Max	Unit
Drivers						
Propagation Delay Time	Tx1 – Tx3	t_{PLH}				µs
Low–to–High (R_L = 3 kΩ, C_L = 50 pF or 2500 pF)			—	0.5	1	
High–to–Low (R_L = 3 kΩ, C_L = 50 pF or 2500 pF)		t_{PHL}	—	0.5	1	
Output Slew Rate	Tx1 – Tx3	SR				V/µs
Minimum Load (R_L = 7 kΩ, C_L = 0 pF)			—	± 6	± 30	
Maximum Load (R_L = 3 kΩ, C_L = 2500 pF)			—	± 5	—	
Output Disable Time		t_{DAZ}	—	4	10	µs
Output Enable Time		t_{DZA}	—	25	50	ms
Receivers						
Propagation Delay Time	DO1 – DO3	t_{PLH}				µs
Low–to–High			—	—	1	
High–to–Low		t_{PHL}	—	—	1	
Output Rise Time	DO1 – DO3	t_r	—	250	400	ns
Output Fall Time	DO1 – DO3	t_f	—	40	100	ns
Output Disable Time		t_{RAZ}	—	4	10	µs
Output Enable Time		t_{RZA}	—	25	50	ms

TRUTH TABLE

Drivers

DI	TxEN	STB	Tx
X	X	H	Z*
X	L	L	L
H	H	L	L
L	H	L	H

* $V_{SS} \le V_{Tx} \le V_{DD}$ X = Don't Care

Receivers

Rx	STB	DO
X	H	Z*
H	L	L
L	L	H

* GND ≤ V_{DO} ≤ V_{CC} X = Don't Care

PIN DESCRIPTIONS

V_{CC}
Digital Power Supply

This digital supply pin is connected to the logic power supply. This pin should have a 0.33 μF capacitor to ground.

GND
Ground

Ground return pin is typically connected to the signal ground pin of the EIA–232–D connector (Pin 7) as well as to the logic power supply ground.

V_{DD}
Positive Power Supply

This is the positive output of the on–chip voltage doubler and the positive power supply input of the driver/receiver sections of the device. This pin requires an external storage capacitor to filter the 50% duty cycle voltage generated by the charge pump.

V_{SS}
Negative Power Supply

This is the negative output of the on–chip voltage doubler/inverter and the negative power supply input of the driver/receiver sections of the device. This pin requires an external storage capacitor to filter the 50% duty cycle voltage generated by the charge pump.

TxEN
Output Enable

This is the driver output enable pin. When this pin is in logic low level, the condition of the driver outputs (Tx1 – Tx3) are in keep OFF (mark) state.

STB
Standby

The device enters the standby mode while this pin is connected to the logic high level. During the standby mode, driver and receiver output pins become high impedance state. In this condition, supply current I_{CC} is below 10 μA (Typ) and can be operated with low current consumption.

C2+, C2–, C1+, C1–
Voltage Doubler and Inverter

These are the connections to the internal voltage doubler and inverter, which generate the V_{DD} and V_{SS} voltages.

Rx1, Rx2 (Rx3)
Receive Data Input

These are the EIA–232–E receive signal inputs. A voltage between + 3 and + 25 V is decoded as a space, and causes the corresponding DO pin to swing to ground (0 V). A voltage between – 3 and – 25 V is decoded as a mark, and causes the DO pin to swing up to V_{CC}.

DO1, DO2 (DO3)
Data Output

These are the receiver digital output pins, which swing from V_{CC} to GND. Each output pin is capable of driving one LSTTL input load.

Output level of these pins is high impedance while in standby mode.

DI1, DI2 (DI3)
Data Input

These are the high impedance digital input pins to the drivers. Input voltage levels on these pins must be between V_{CC} and GND.

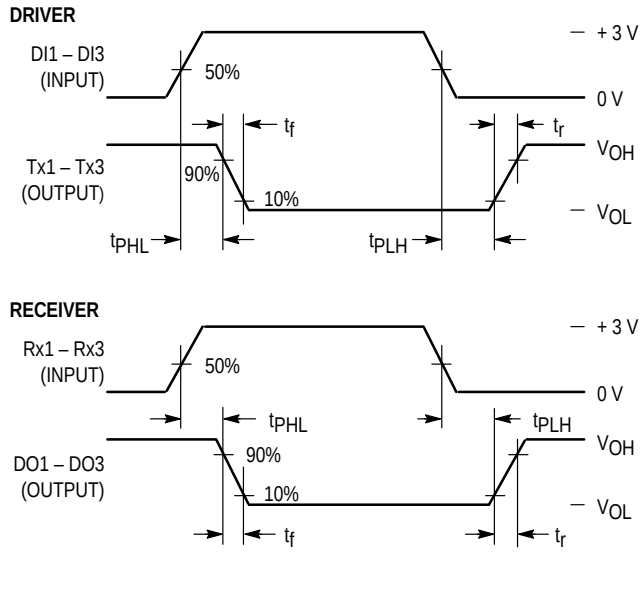
The level of these input pins are TTL/CMOS compatible.

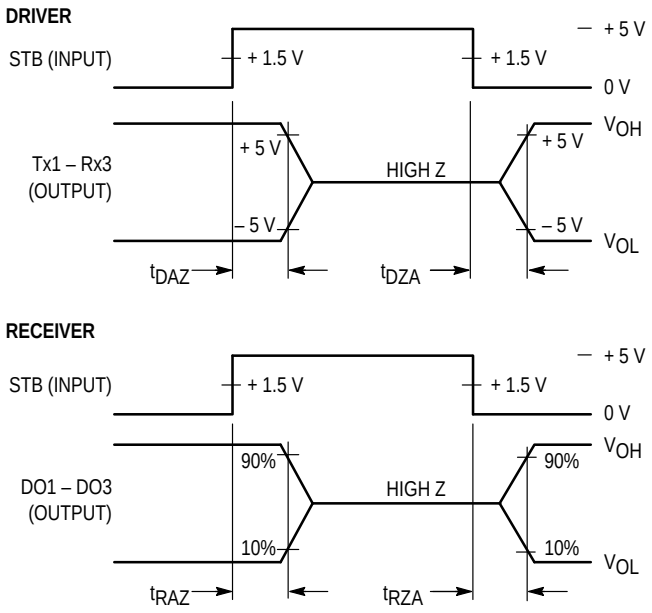
Tx1, Tx2 (Tx3)
Transmit Data Output

These are the EIA–232–E transmit signal output pins, which swing toward V_{DD} and V_{SS}. A logic 1 at a DI input causes the corresponding Tx output to swing toward V_{SS}. The actual levels and slew rate achieved will depend on the output loading (RL/CL).

The minimum output impedance is 300 Ω when turned off.

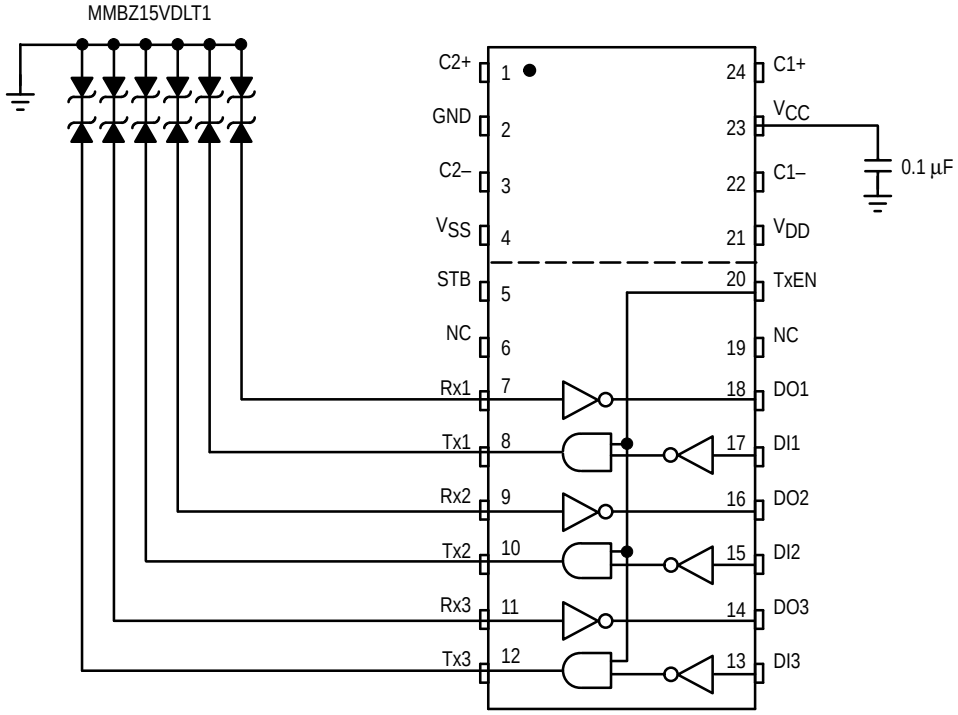
SWITCHING CHARACTERISTICS





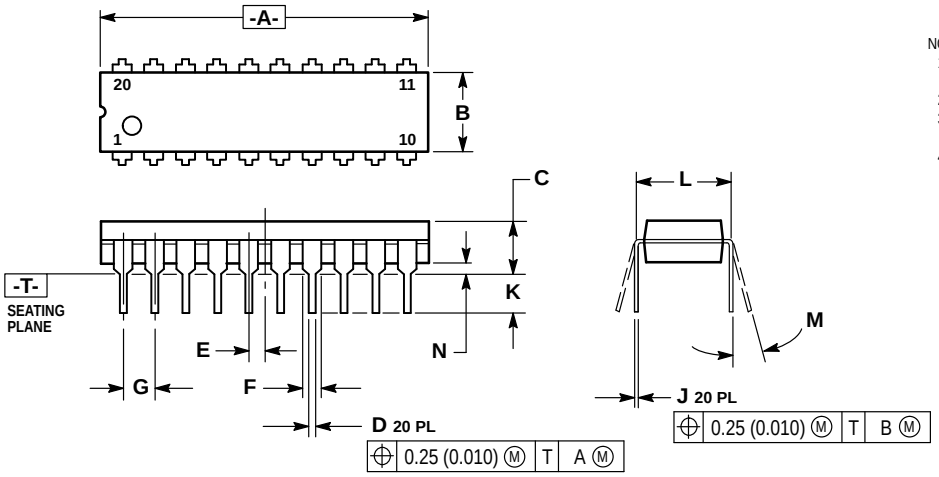
ESD PROTECTION

ESD protection on IC devices that have their pins accessible to the outside world is essential. High static voltages applied to the pins when someone touches them either directly or indirectly can cause damage to gate oxides and transistor junctions by coupling a portion of the energy from the I/O pin to the power supply buses of the IC. This coupling will usually occur through the internal ESD protection diodes which are designed to do just that. The key to protecting the IC is to shunt as much of the energy to ground as possible before it enters the IC. The figure below shows a technique which will clamp the ESD voltage at approximately ± 15 V using the MMBZ15VDLT1. Any residual voltage which appears on the supply pins is shunted to ground through the capacitors C1 and C2.



PACKAGE DIMENSIONS

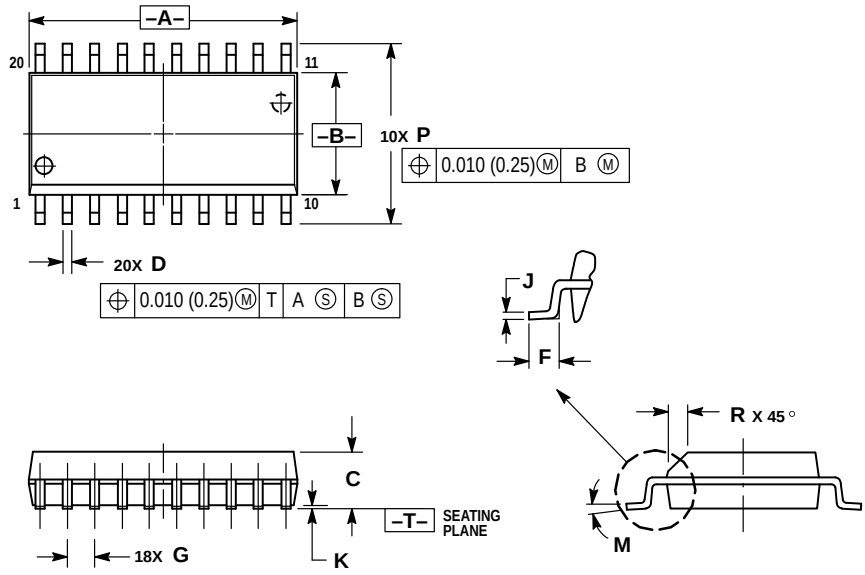
P SUFFIX
PLASTIC DIP
CASE 738–03



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

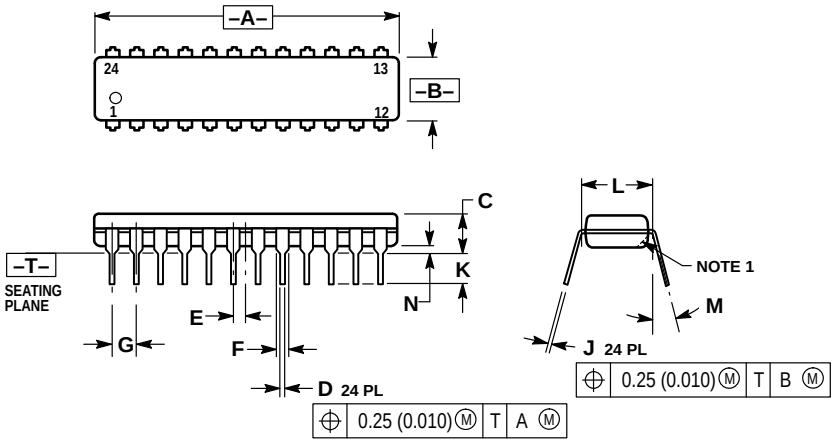
DW SUFFIX
SOG PACKAGE
CASE 751D–04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

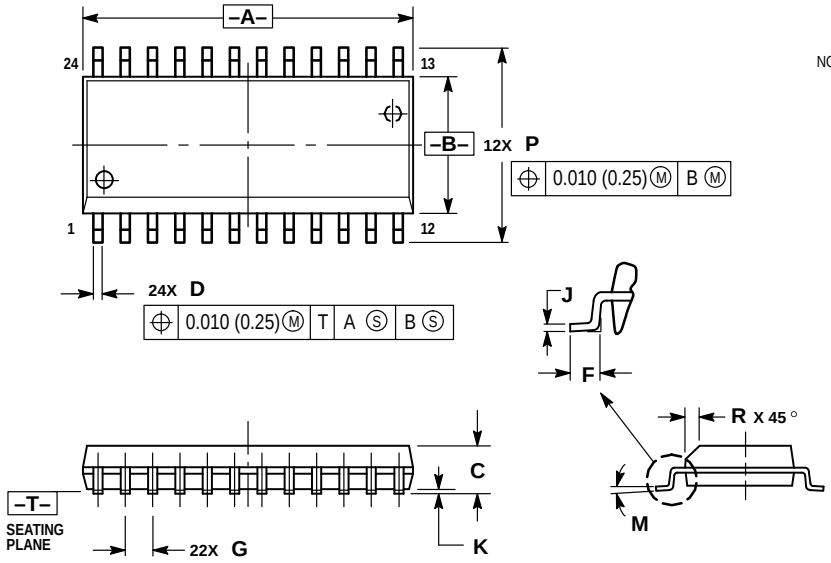
P SUFFIX
PLASTIC DIP
CASE 724–03



NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.230	1.265	31.25	32.13
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.020	0.38	0.51
E	0.050 BSC		1.27 BSC	
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
J	0.007	0.012	0.18	0.30
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

DW SUFFIX
SOG PACKAGE
CASE 751E–04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

This page intentionally left blank.

This page intentionally left blank.

How to reach us:
USA/EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298