Highly-Integrated Green-Mode PWM Controller **SG6842**

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FEATURES

- Linearly decreasing PWM frequency
- Burst-mode at light load and zero load
- Low start-up current (20uA)
- Low operating current (4mA)
- Internal latch circuit for OTP, OVP
- Leading-edge blanking
- Built-in synchronized slope compensation
- Totem pole output with soft driving
- Improved EMI
- Constant power limit over a universal AC input range
- Current mode operation
- Cycle-by-cycle current limiting
- Under Voltage Lockout (UVLO)
- Programmable PWM frequency
- GATE output maximum voltage clamped at 18V
- VDD Over Voltage Protection (OVP)
- Programmable Over Temperature Protection (OTP)
- Very few external components are required

APPLICATIONS

General-purpose switch mode power supplies and flyback power converters, including:

- Power adapters
- Open-frame SMPS
- Battery Charger Adapter

DESCRIPTION

The highly integrated SG6842 series of PWM controllers provides several features to enhance the performance of flyback converters. To minimize standby power consumption, a proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency under light-load conditions. Under zero-load conditions, the power supply enters burst-mode. This completely shuts off PWM output. Then, the output restarts just before the supply voltage, VDD, drops below the UVLO voltage. This green-mode function enables the power supply to easily meet international power conservation requirements.

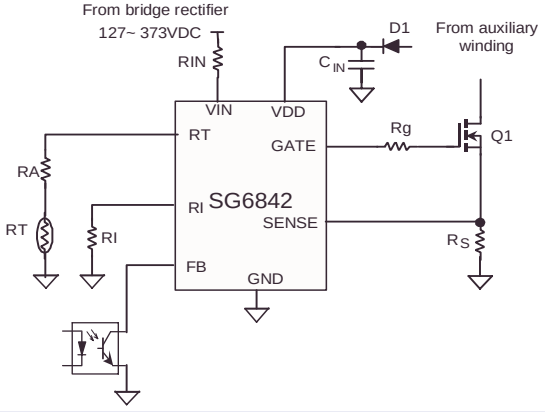
For improved power conversion efficiency, the SG6842 series is manufactured using the BiCMOS process. This allows the start-up current to be reduced to 20uA, and the operating current to be reduced to 4mA. For even higher power conversion efficiency, a large start-up resistance can be used.

Built-in synchronized slope compensation ensures the stability of peak current mode control. Proprietary internal compensation ensures constant output power limiting over a universal range of AC input voltages, from 90VAC to 264VAC.

SG6842 controllers provide many protection functions. Pulse-by-pulse current limiting ensures a constant output current, even when short circuits occur. Should an open circuit failure occur in the feedback loop, the internal protection circuit will disable PWM output. PWM output will be disabled as long as VDD remains higher than 26V. The gate output is clamped at 18V to protect the power MOS from over-voltage damage. An external NTC thermistor can be applied to sense the ambient temperature for over temperature protection. When either over temperature conditions or VDD over voltage faults are detected, an internal latch circuit is used to latch-off the controller. The latch will reset when the temperature cools off sufficiently, or when the VDD power supply is disabled.

SG6842 series controllers are available in both 8-pin DIP and SO packages.

TYPICAL APPLICATION



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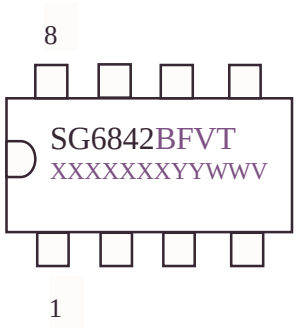
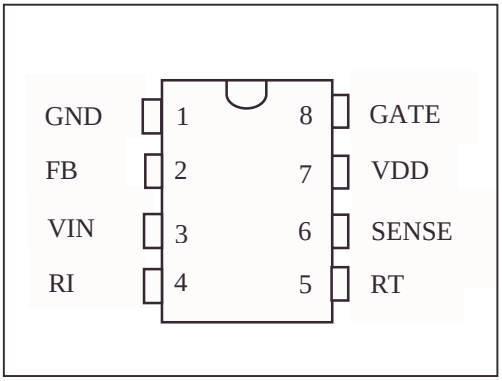
MARKING DIAGRAMS



B: B = Linearly Decreasing Frequency + Burst-Mode: Null = Linear
F: L = OTP Latch: The pin is reset when AC is disconnected.
C = Hysteresis OTP : The pin is reset when the temperature cools down.
V: V = OVP Latch
T: D = DIP, S = SOP
XXXXXXX: Wafer Lot
YY: Year; WW: Week
V: Assembly Location

PIN CONFIGURATION



ORDERING INFORMATION

The SG6842 family of controllers is distinguished for its protection features and burst-mode functionality.

Part Number	Green-Mode Function: Linearly Decreasing Frequency and Burst-Mode			Package
	OTP Latch: Reset when AC is unplugged (L).	Hysteresis OTP: Reset when the temperature cools down (C).	OVP Latch: Reset when AC is unplugged (V).	
SG6842BS				8-Pin SOP
SG6842BD				8-Pin DIP
SG6842BLS	✔			8-Pin SOP
SG6842BLD	✔			8-Pin DIP
SG6842BCS		✔		8-Pin SOP
SG6842BCD		✔		8-Pin DIP
SG6842BLVS	✔		✔	8-Pin SOP
SG6842BLVD	✔		✔	8-Pin DIP
SG6842BCVS		✔	✔	8-Pin SOP
SG6842BCVD		✔	✔	8-Pin DIP

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Part Number	Green Mode Function: Linearly Decreasing Frequency			Package
	OTP Latch: Reset when AC is unplugged (L).	Hysteresis OTP: Reset when the temperature cools down (C).	OVP Latch: Reset when AC is unplugged (V).	
SG6842S				8-Pin SOP
SG6842D				8-Pin DIP
SG6842LS	✔			8-Pin SOP
SG6842LD				8-Pin DIP
SG6842CS		✔		8-Pin SOP
SG6842CD				8-Pin DIP
SG6842LVS	✔		✔	8-Pin SOP
SG6842LVD				8-Pin DIP
SG6842CVS		✔	✔	8-Pin SOP
SG6842CVD				8-Pin DIP

Note 1: All part numbers have the following default protection functions:

a. OTP. PWM output is turned off when an over-temperature condition is detected.
b. OVP. PWM output is turned off when an over-voltage condition is detected.

Note 2: Green-Mode:

a. Linear-Mode: The PWM frequency linearly decreases from the maximum frequency of 65kHz to around 12kHz. This happens when the output load goes from a high-load state to low-load/zero-load state.
b. Linear-Mode with Burst-Mode: After the PWM frequency linearly decreases from the maximum frequency of 65kHz to around 22kHz, the controller can enter into burst-mode. In burst-mode, PWM completely stops, and the V_{DD} voltage begins dropping. When V_{DD} drops to 11.75V (1.25V higher than the UVLO threshold), the SG6842 will start to send out PWM signals at a frequency of 27kHZ.

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PIN DESCRIPTIONS

Pin No.	Symbol	Function	Description
1	GND	Ground	Ground.
2	FB	Feedback	The signal from the external compensation circuit is fed into this pin. This FB pin and the current-sense signal from Pin 6 determine the PWM duty cycle.
3	VIN	Start-Up Input	For start-up, this pin is pulled high to the rectified line input. This pin is pulled via a resistor. Since the start-up current requirement of the SG6842 is very small, a large start-up resistance can be used to minimize power loss. Under normal operation, this pin is also used to detect the line voltage. The line voltage is detected to compensate the output power limit, so that it can be kept constant over a universal AC input range
4	RI	Reference Setting	A resistor from the RI pin to ground will generate a constant current source for the SG6842. This current charges an internal capacitor. This determines the switching frequency. Increasing the resistance will decrease the amplitude of the current from the current source, and thereby reduce the switching frequency. Using a 26kΩ resistor Ri results in a 50uA constant current Ii and a 65kHz switching frequency.
5	RT	Temperature Detection	For over-temperature protection. An external NTC thermistor is connected from this pin to ground. The impedance of the NTC will decrease at high temperatures. Once the voltage of the RT pin drops below a fixed limit of 1.05V, PWM output will be disabled.
6	SENSE	Current Sense	Current sense. The sensed voltage is used for current-mode control and pulse-by-pulse current limiting. To protect against short circuits across the current-sense resistor, the controller continuously checks the SENSE pin. If a low voltage is detected, the controller will immediately shut down.
7	VDD	Power Supply	Power Supply. If an open circuit failure occurs in the feedback loop, the internal protection circuit will disable PWM output as long as VDD remains higher than 26V.
8	GATE	Driver Output	The totem-pole output driver for the power MOSFET. A soft driving waveform is implemented for improved EMI.

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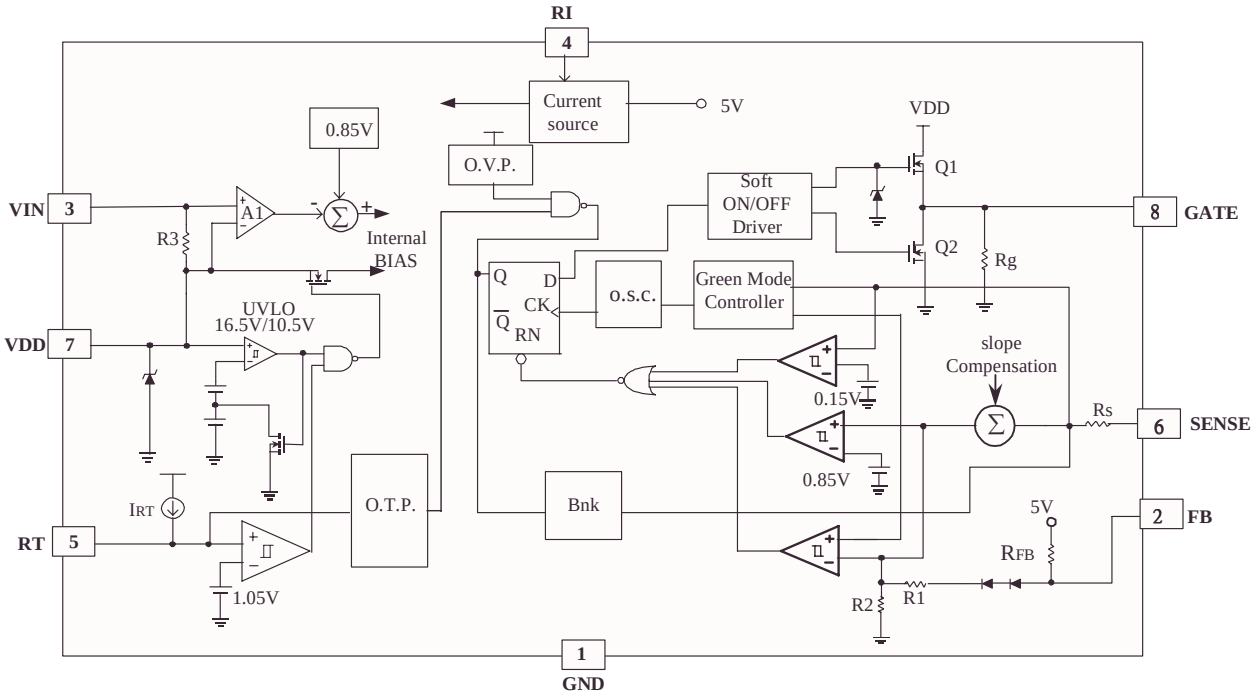
BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Condition	Value	Unit
VDD	Supply Voltage	Low Impedance Source, Zener Clamp	28 30	V V
Iz	Zener Current	-	10	mA
VIN	FB/SENSE Terminal Input Voltage	FB, SENSE	-0.3 to 5.5V	V
ISINK	Error Amplifier Sink Current	-	10	mA
IOUT	Gate Output Current	-	TBD	mA
VFB	Input Voltage to FB Pin	-	-0.3 to 7V	V
VSense	Input Voltage to SENSE Pin	-	-0.3 to 7V	V
VRT	Input Voltage to RT Pin	-	-0.3 to 7V	V
VRI	Input Voltage to RI Pin	-	-0.3 to 7V	V
Pd	Power Dissipation	at Ta < 50°C DIP SOP	800 400	mW
RΘ j-a	Thermal Resistance	Junction-Air DIP SOP	82.5 141	°C/W
TJ	Operating Junction Temperature	-	150	°C
Ta	Operating Ambient Temperature	-	-40 to 125	°C
TSTG	Storage Temperature Range	-	-65 to +150	°C
TL	Lead Temperature (Soldering)	10 sec DIP 10 sec SOP	260 230	°C
	ESD Capability, HBM Model	-	2.0	kV
	ESD Capability, Machine Model	-	200	V

OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
Vcc	Supply Voltage	-	20	V
Ta	Operating Ambient Temperature	-30	85	°C

ELECTRICAL CHARACTERISTICS

Feedback Input Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Av	Input-Voltage to Current-Sense Attenuation		1/3.5	1/4	1/4.5	V/V
Zfb	Input Impedance		3	4.5	6	kΩ
Ifb	Bias Current				2	mA
Voz	Zero Duty-Cycle Input Voltage		1.2			V

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Current Sense Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Zcs	Input Impedance		8	12	16	kΩ
T_{PD}	Delay to Output			100	200	nsec
Vth	Current Limit Threshold Voltage		0.8	0.85	0.9	V
ΔVth @ IIN	Threshold Voltage Change versus the Input Current of the VIN Pin	IIN = 220 uA	-0.09	-0.15	-0.21	V
Tdelay-Ips	The Delay Time for Limited Power Control.	VFB=5V Ri=26KΩ		32		msec
Sense-VF	The Delay Time for VDD Over Voltage Protection.	VDD=25V~27V Ri=26KΩ		32		msec

Oscillator Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Fosc	Normal Mode Frequency	Ri=26KΩ	60	65	70	KHz
Fosc-green	Green-ON Mode Frequency	Ri=26KΩ	20	22.5	25	KHz
Fosc-goff	Green-OFF Mode Frequency (Burst-Mode Version)	Ri=26KΩ			0	KHz
Vg	Green-OFF Mode Voltage at FB pin	VDD=15V		1.6		V
Vn	FB Pin Threshold for Beginning the Reduction of Frequency	VDD=15V		2.3		V
Sg	Slope for Green-Mode Modulation	Ri=26KΩ		60		Hz/mV
Fdv	Frequency Variation Versus VDD Deviation	VDD=11 to 20V			5	%
Fdt	Frequency Variation Versus Temp. Deviation	Ta=-30 to 85℃		1.5	5	%
VDD-th-g	VDD Low-Threshold Voltage to Exit Green-OFF Mode		VTH(OFF) + 0.8	VTH(OFF) + 1.25	VTH(OFF) + 1.7	V

PWM Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DCY (MAX)	Maximum Duty Cycle		80	85	90	%
DCY (MIN)	Minimum Duty Cycle (= Bnk)		-	1		%
Bnk	Leading Edge Blanking Time		260	360	460	nsec

Output Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Vol	Output Voltage Low	VDD= 12V, Io = 50mA			1.5	V
Voh	Output Voltage High	VDD= 12V, Io = 50mA	8V			V
Tr	Rising Time	VDD=15V, CL=1nF	150	250	350	nsec
Tf	Falling Time	VDD=15V, CL=1nF	30	50	90	nsec
Vclamp	Gate Output Clamping Voltage	VDD=25V		18		V

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Over Temperature Protection Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Irt	Output Current of RT Pin	Ri=26KΩ	64	70	76	uA
VOTP-LATCH-OFF	Threshold Voltage for Over Temperature Protection. Turn-Off and Latch-Off.		1.015	1.05	1.085	V
TDOTP-LATCH	Over-Temperature Latch-Off Debounce.		2	8	16	msec
VOTPRESET-ON	Threshold Voltage (Hysteresis) for Over Temperature Latch-Off Reset. At this Threshold, the Latch is Reset and PWM is Turned On.		1.05	1.15	1.25	V

VDD Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
VTH(ON)	On Threshold Voltage		15.5	16.5	17.5	V
VTH(OFF)	Off Threshold Voltage		9.5	10.5	11.5	V
IDD ST	Start-Up Current (VDD = 15.5V)			8	20	uA
IDD OP	Operating Supply Current (FB=SENSE=0V, VDD =15V, GATE Open)	-		3.7	5	mA
VDD-OVP	VDD Over Voltage Protection (Disable PWM Output). For Protection Against Open Feedback Loops.		23.5	25.5	28	V
Td-VDD-OVP	VDD Over Voltage Protection Debounce (Disable PWM Output)			200		n sec
VDD-ZENER	VDD ZENER Crowbar	IDD = 10mA	27	30	33	V

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TYPICAL CHARACTERISTICS

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OPERATION DESCRIPTION

Start-Up Current

The typical start-up current is only 20uA. This allows a high resistance, low-wattage start-up resistor to be used, to minimize power loss. A 1.5 MΩ, 0.25W, start-up resistor and a 10uF/25V VDD hold-up capacitor would be sufficient for an AC/DC adapter with a universal input range.

Operating Current

The required operating current has been reduced to 4mA. This enables higher efficiency and reduces the VDD hold-up capacitance requirement.

Green Mode Operation

The proprietary Green-mode function provides off-time modulation to linearly decrease the switching frequency under light-load conditions. On-time is limited to provide protection against abnormal conditions and brownouts. To further reduce power consumption under zero-load conditions, the PWM output will be completely turned off, and the power supply will enter burst-mode. After the PWM oscillator is turned off, the IC's supply voltage VDD will drop gradually. Before the VDD voltage drops below the UVLO voltage, the PWM oscillator will be turned on again. This Green-mode function dramatically reduces power consumption under light-load and zero-load conditions. Power supplies using a SG6842 controller can easily meet even the most restrictive international regulations regarding standby power consumption.

Oscillator Operation

A resistor connected from the RI pin to ground generates a constant current source for a SG6842 controller. This current is used to charge an internal capacitor. The charge of the capacitor determines the internal clock and the switching frequency. Increasing the resistance will decrease the amplitude of the current source and reduce the switching frequency. Using a 26kΩ resistor R_i results in a 50uA constant current I_i, and a corresponding 65kHz switching frequency. The relationship between R_i and the switching frequency is:

$$f_{PWM} = \frac{1690}{R_I\ (k\Omega)}(kHz) \quad \text{---------- (1)}$$

SG6842 controllers are designed to operate at a PWM oscillation frequencies ranging from 50kHz to 100kHz.

Leading Edge Blanking

Each time the power MOSFET is switched on, a turn-on spike will inevitably occur at the sense-resistor. To avoid premature termination of the switching pulse, a 360nsec leading-edge blanking time is built in. Conventional RC filtering is not necessary. During this blanking period, the current-limit comparator is disabled, and it cannot switch off the gate drive.

Under-Voltage Lockout (UVLO)

The turn-on/turn-off thresholds are fixed internally at 16.5V/10.5V. To enable a SG6842 controller during start-up, the hold-up capacitor must first be charged to 16.5V, through the start-up resistor.

The hold-up capacitor will continue to supply VDD before energy can be delivered from the auxiliary winding of the main transformer. VDD must not drop below 10.5V during this start-up process. This UVLO hysteresis window ensures that the hold-up capacitor can adequately supply VDD during start-up.

Gate Output / Soft Driving

The BiCMOS output stage of a SG6842 is a fast totem pole gate driver. Cross-conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 18V Zener diode in order to protect the power MOSFET transistors against any harmful over-voltage gate signals. A soft driving waveform is implemented to minimize EMI.

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Slope Compensation

The sensed voltage across the current sense resistor is used for current mode control and pulse-by-pulse current limiting. The built-in slope compensation function improves power supply stability and prevents peak current-mode control from causing sub-harmonic oscillations. With every switching cycle, a positively sloped, synchronized ramp is activated by SG6842 controllers.

Constant Output Power Limit

When the SENSE voltage across the sense resistor RS reaches the threshold voltage (around 0.85V), the output GATE drive will be turned off following a small propagation delay tD. This propagation delay will introduce an additional current proportional to tD*VIN/LP. The propagation delay is nearly constant regardless of the input line voltage VIN. Higher input line voltages will result in larger additional currents. Thus, under high input-line voltages the output power limit will be higher than under low input-line voltages.

Over a wide range of AC input voltages, the variation can be significant. To compensate for this, the threshold voltage is adjusted by the VIN current. Since the VIN pin is connected to the rectified input line voltage through the start-up resistor, a higher line voltage will generate a higher VIN current through the VIN pin.

The threshold voltage decreases if the VIN current increases. A small threshold voltage will force the output GATE drive to terminate earlier, thus reducing total PWM turn-on time, and making the output power equal to that of low line input. This proprietary internal compensation feature ensures a constant output power limit over a wide range of AC input voltages (90VAC to 264VAC).

VDD Over-Voltage Protection

VDD over-voltage protection has been built in to prevent any over voltage destruction. When VDD voltage is abnormally over 25.5V, the PWM output will be turned off. The over-voltage condition is usually caused by feedback open loop.

Thermal Protection

An external NTC thermistor can be connected from the RT pin to ground. The impedance of the NTC will decrease at high temperatures. When the voltage of the RT pin drops below 1.05V, the PWM output will be latched off. After the latch is reset and cleared, the PWM will be turned on again.

Limited Power Control

The FB voltage will increase every time the output of the power supply is shorted or over-loaded. If the FB voltage remains higher than a built-in threshold (4.2V) for longer than 32msec, PWM output will then be turned off. As the PWM output is turned off, the supply voltage VDD will also begin decreasing.

When VDD goes below the turn-off threshold (eg, 10.5V) the controller will be totally shut down. VDD will be charged up to the turn-on threshold voltage of 16.5V through the start-up resistor until PWM output is restarted. This protection feature will continue to be activated as long as the over-loading condition persists. This will prevent the power supply from overheating due to over loading conditions.

Protection Latch Circuit

In some applications, latch operation for OVP or OTP may be necessary. For the SG6842 family, the optional built in latch function provides a versatile protection feature that does not require external components. See ordering information for a detailed description. To reset the latch circuit, it is necessary to disconnect the AC line voltage of the power supply.

Noise immunity

Noise from the current sense or the control signal may cause significant pulse width jitter, particularly in continuous-conduction mode. Slope compensation helps alleviate this problem. Good placement and layout practices should be followed. The designer should avoiding long PCB traces and component leads. Compensation and filter components should be located near the SG6842. Finally, increasing the power-MOS gate resistance is advised.

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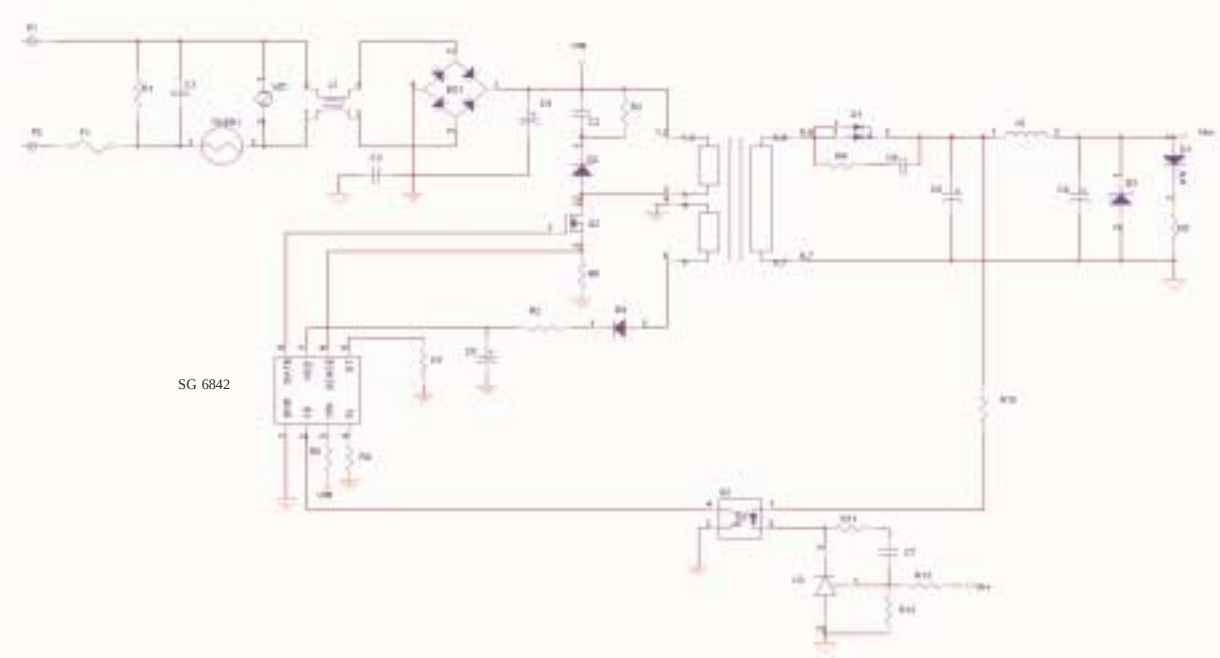
REFERENCE CIRCUIT

Circuit



BOM

Reference	Component	Reference	Component
BD1	BD 1A/600V	Q2	MOS 2A/600V
C1	XC 0.22u	R1,R2	R 470KΩ 1/4W
C2	EC 0.1u 250V	R3	R 47Ω 1/4W
C3,C6,C7	YC 222p	R4	R 22Ω 1/4W
C4	EC 68u/400V	R5	R 4.7KΩ 1/4W
C5	CC 102p/1KV	R6	R 0.5Ω 1W
C8	EC 1200u/16V	R8,R12	R 510KΩ 1/4W
C9	EC 680u/16V	R9	R 20KΩ 1/8W 1%
C10	EC 10u/25V	R10	R 100Ω 1/8W
D1	LED	THER1	Thermistor SCK054
D3	ZD 12V	T1	Transformer EI28
F1	FUSE 2A/250V	U1	IC SG6842
L1	UU10.5	U2	IC 4N35D
L2	L04	U3	IC TL431
Q1	DIODE	VZ1	VZ 9G

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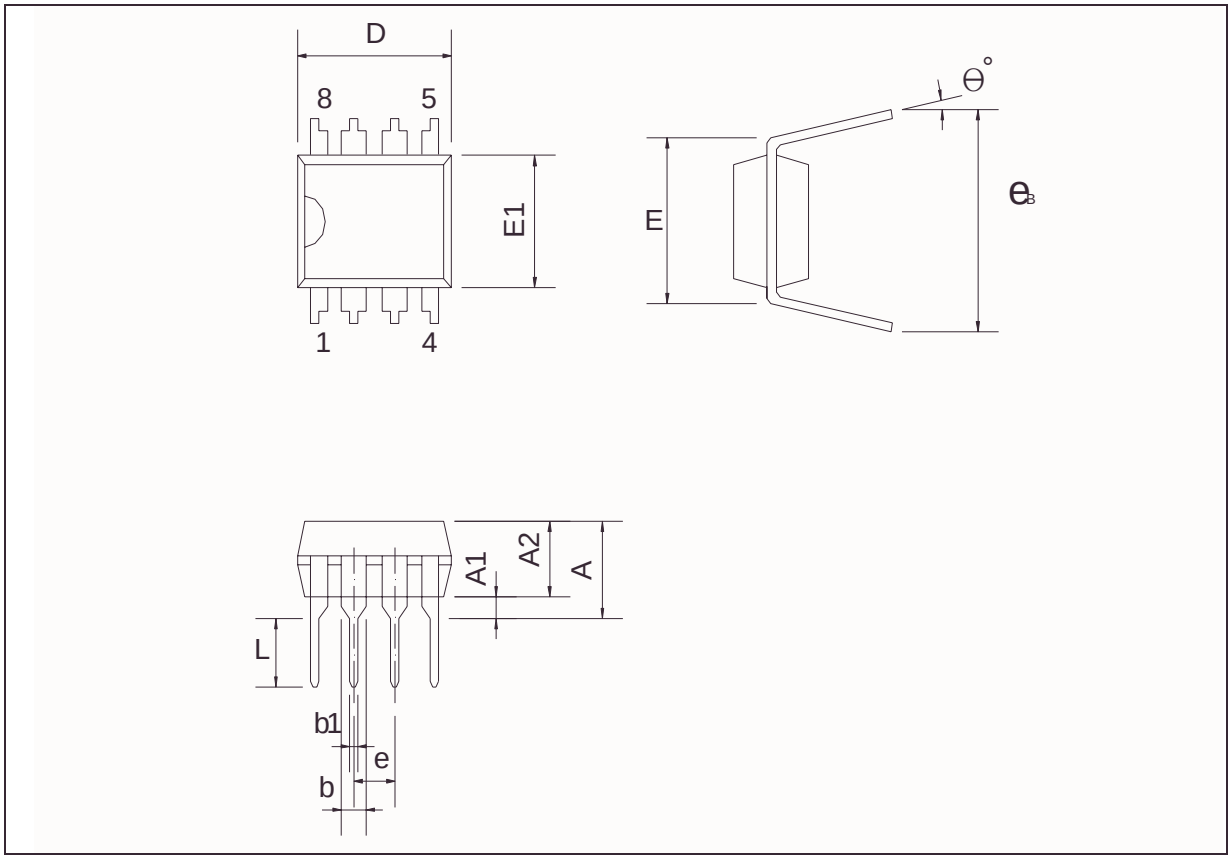
PACKAGE INFORMATION

DIP-8 Outline Dimensions



Dimensions

Symbol	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.334			0.210
A1	0.381			0.015		
A2	3.175	3.302	3.429	0.125	0.130	0.135
b		1.524			0.060	
b1		0.457			0.018	
D	9.017	9.271	10.160	0.355	0.365	0.400
E		7.620			0.300	
E1	6.223	6.350	6.477	0.245	0.250	0.255
e		2.540			0.100	
L	2.921	3.302	3.810	0.115	0.130	0.150
eB	8.509	9.017	9.525	0.335	0.355	0.375
θ°	0°	7°	15°	0°	7°	15°

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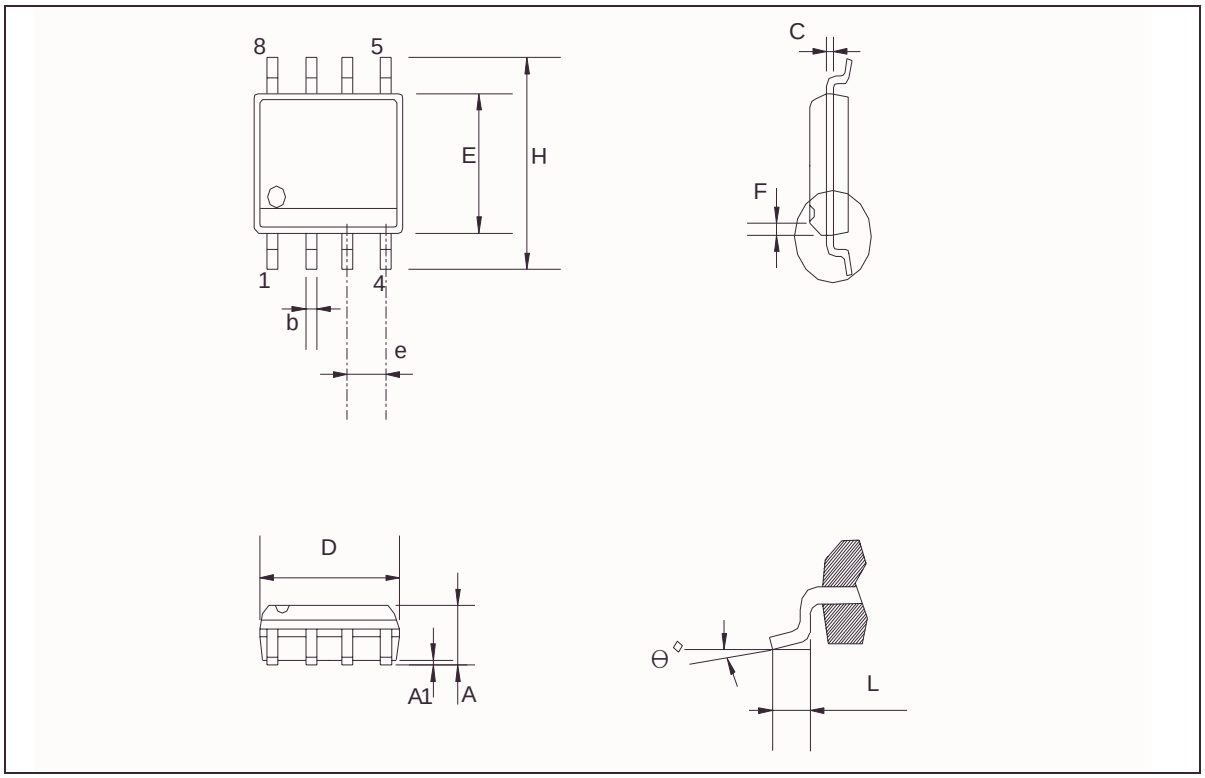
SOP-8 Outline Dimensions



Dimensions

Symbol	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.346		1.752	0.053		0.069
A1	0.101		0.254	0.004		0.010
b		0.406			0.016	
c		0.203			0.008	
D	4.648		4.978	0.183		0.196
E	0.381		3.987	0.150		0.157
e		1.270			0.050	
F		0.381X45°			0.015X45°	
H	5.791		6.197	0.228		0.244
L	0.406		1.270	0.016		0.050
θ°	0°		8°	0°		8°

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